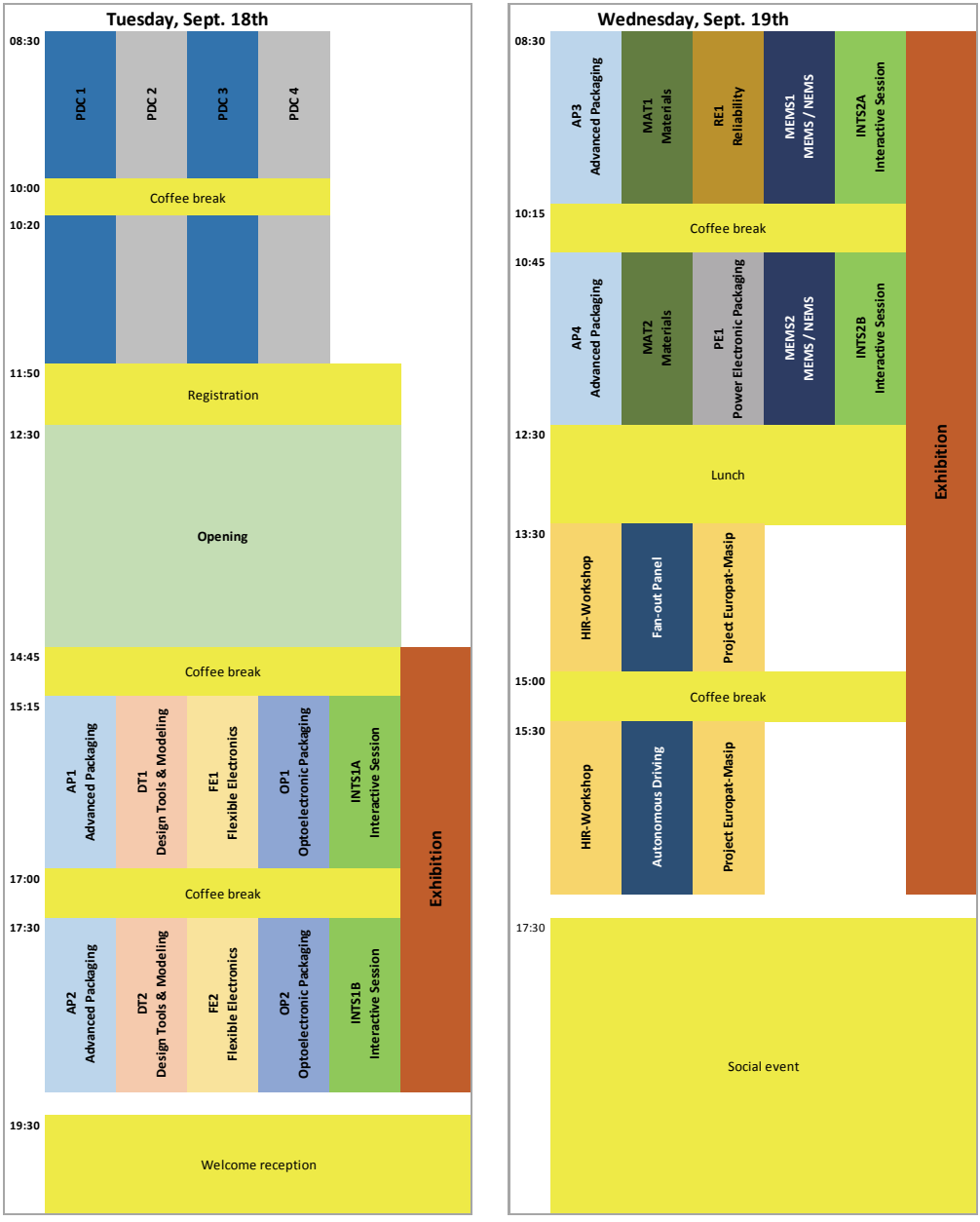
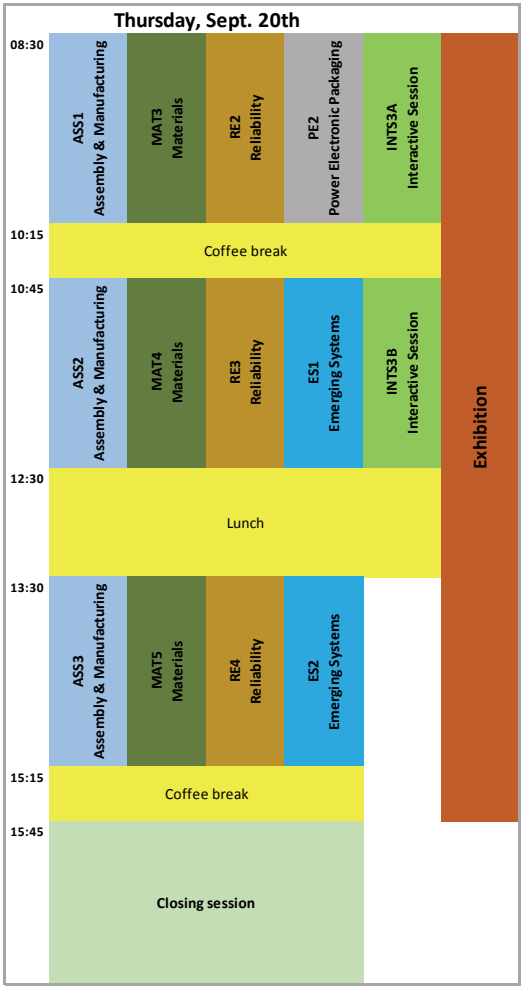
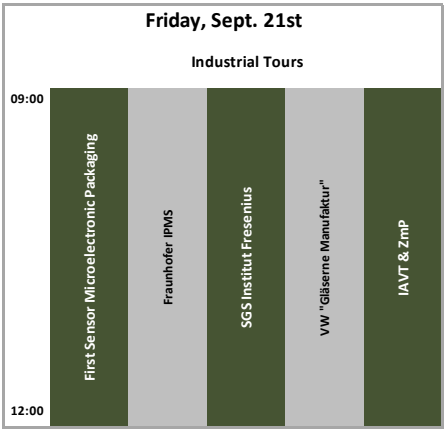
Schedule Overview

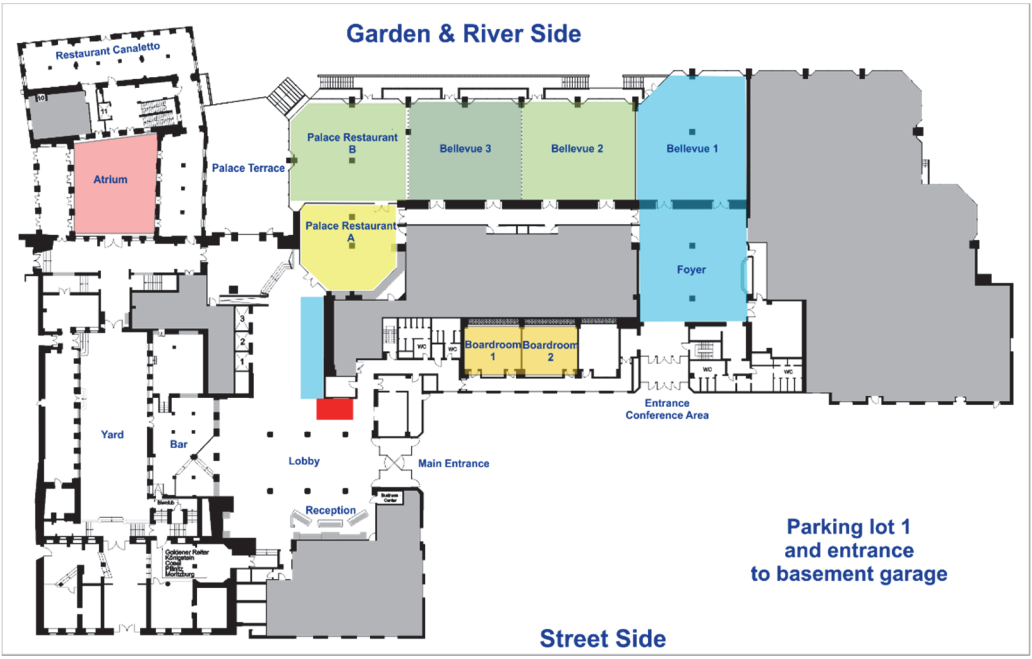


Schedule Overview





Conference Area Map



What?	Where?	
Registration	Lobby	
Opening, Closing, Keynotes	Bellevue 2, Bellevue 3, Palace Restaurant B	
Oral Presentations	Bellevue 2, Bellevue 3, Palace Restaurant B, Boardroom 1/2	
Interactive Presentations	Palace Restaurant A	
Industrial Exhibition	Bellevue 1, Foyer, Lobby	
Special Workshops	Bellevue 2, Bellevue 3, Boardroom 1/2	
Coffee and Lunch Breaks	Bellevue 1, Foyer, Atrium, Palace Restaurant A,	

Room	Bellevue 2	Bellevue 3
Session	AP1	DT1
Chairs	Rolf Aschenbrenner Fraunhofer IZM, Germany Hannes Stahr AT&S, Austria	Laurent Bechou IMS Bordeaux, France Christian Goetze Global Foundries, Germany
15:15	**Laser Assisted Bonding Technology Enabling Fine Bump Pitch in Flip Chip Package Assembly** Chi-Yuan Chen[1], Ian Hsu[1], Stanley Lin[1], DongSam Park[2], Ming-Che Hsieh[3] *1: MediaTek, Inc., Taiwan; 2: STATS ChipPAC Korea; 3: STATS ChipPAC Pte. Ltd Singapore*	**Chip/Package/Board Co-Simulation Methodology for Crosstalk between DC/DC Converter and ADC Input Channels** Francesco Setting[1,2], T. Brandtner[1], V. Subotskaya[1], A. Levanto[1], M. Faricelli[1], F. Praemassing[1], L. Della Ricca[1], H. Koffler[1], P. Palestri[3], F. Crupi[2] / *1: Infineon Technologies Austria AG; 2: University of Calabria, Italy; 3: University of Udine, Italy*
15:45	**Surface Treatment of Gold Bumps for Thermocompression Bonding with Low Temperature and Low Pressure** Juliane Fröhlich[1], Lothar Dietrich[1], Hermann Oppermann[1], Klaus-Dieter Lang[2] *1: Fraunhofer IZM, Germany; 2: Technische Universität Berlin, Germany*	**Electrical Modeling Approach and Manufacturing of a new Adjustable Capacitor for Medical Applications** Zaineb Jebri[1,2], Isabelle Bord Majek[1], Celine Delafosse[2], Yves Ousten[1] *1: IMS, France; 2: Exxelia Temex, France*
16:10	**Cu-In Fine-Pitch-Interconnects: Influence of Processing Conditions on the Interconnection Quality** Steffen Bickel[1], Shawon Sen[1], Jörg Meyer[1], Iuliana Panchenko[1,2], M. Jürgen Wolf[2] *1: Technische Universität Dresden, Germany; 2: Fraunhofer Institute for Reliability and Microintegration - ASSID, Germany*	**High Precision Numerical and Experimental Thermal Studies of Microelectronic Packages in Still Air Chamber Tests** Papa Momar Souare[1], Mamadou Kabirou Toure[1], Stephanie Allard[2], Benoit Foisy[2], Bijan Borzou[1], Eric Duchesne[2], Julien Sylvestre[1] *1: University of Sherbrooke, Canada; 2: IBM Bromont, Canada*
16:35	**Curved Full-Frame CMOS Sensor: Impact on Electro-Optical Performances** Bertrand Chambion[1], Stéphane Caplet[1], Jan Martin Kopfer[2], Aurélie Vandeneynde[1], Wim Diels[2], Alexandre de Kerckhove[2], Patrick Peray[1], David Henry[1] *1: University Grenoble Alpes, CEA, LETI, MINATEC campus, France; 2: AMS Sensors, Belgium*	**Can Bond Wires really be used as Antennas?** Ivan Ndip[1], Karl-Friedrich Becker[1], Flynn Brandenburger[1], Thi Huyen Le[1], Max Huhn[2], Jörg Bauer[1], Mathias Koch[1], Martin Hempel[1], Martin Schneider-Ramelow[1,3], Klaus-Dieter Lang[1,3] *1: Fraunhofer IZM, Germany; 2: Biotronik SE & Co. KG, Germany; 3: Technische Universität Berlin, Germany*

17:00	**Coffee break** Coffee and snacks will be served in the exhibition area located in **Foyer** and in **Bellevue 1** as well as in **Palace Restaurant A** and **Atrium**.

Palace Restaurant B	Boardroom 1/2	Room
FE1	**OP1**	Session
Karlheinz Bock TU Dresden, Germany Matti Mäntysalo Tampere University of Technology, Finland	Stéphane Bernabé CEA-LETI, France Giovanni Delrosso VTT Technical Research Centre, Finland	Chairs
Integration with Light Gari Arutinov[1], Merijn Giesbers[1], Rob Hendriks[2], Nikhil Pillai[2], Roel Kusters[1], Jeroen van den Brand[1] *1: Holst Centre/TNO, The Netherlands; NovaCentrix, USA*	On-board Optical Fiber and Embedded Waveguide Interconnects Lars Brusberg[1], Ulrich Neukirch[1], Alan F. Evans[1], Michael DeJong[2], Michael Yadlowsky[2], Andreas Matiss[3], Changsung Sean Kim[1] *1: Corning Research & Development Corporation, USA; 2: Corning Optical Communications LCC, USA; 3: Corning Optical Communications GmbH & Co.KG, Germany*	15:15
Roll-to-roll Functional Testing of Printed Conductors and Organic Light Emitting Devices Tuomas Happonen[1], Markus Tuomikoski[1], Tuomas Kokko[1], Kari Rönkä[1] *1: VTT Technical Research Centre of Finland*	Single Mode Polymer Optical Waveguides and Out-of-Plane Coupling Structure on a Glass Substrate Jean-Marc Boucaud[1,2,3], Q. Hivin[2], C. Durand[1], F. Gianesello[1], D. Bucci[3], J.-F. Robillard[2], F. Vaurette[2], J.-E. Broquin[3], E. Dubois[2] *1: STMicroelectronics, France; 2: Univ. Lille, France; 3: IMEP-LaHC, Université de Grenoble Alpes, France*	15:45
Hybrid Lightweight and Flexible Circuit Boards for Satellites Nenad Marjanovic[1], Jérémy Disser[1], Frédéric Zanella[1], Jürg Schleuniger[1], Alessandro Mustaccio[1], Rolando Ferrini[1], Marc Schnieper[1], Eyad Assaf[2] *1: CSEM Center Muttenz, CSEM SA, Switzerland; 2: HIGHTEC MC AG, CSEM SA, Switzerland*	Two-Stage Simulation for Coupling Schemes in the Device Communication using Ray Tracing and Beam Propagation Method Lukas Lorenz[1], Krzysztof Nieweglowski[1], Klaus-Jürgen Wolter[1], Karlheinz Bock[1] *1: Technische Universität Dresden, Germany*	16:10
Conductors and transistors for biodegradable devices Michael Hoffmann[1], Falk Schütze[1], Christian May[1], Claudia Keibler-Willner[1] *1: Fraunhofer FEP, Germany*	Reliability Considerations in Discrete Optics External Cavity Tunable Laser Assemblies Maria Chiara Ubaldi[1] *1: Fondazione CIFE, Italy*	16:35

Note about Boardroom 1/2: Presentations will be given in Boardroom 1. As an addition to capacity there will be a real-time video and audio broadcast to Boardroom 2.

Please visit the Industrial Exhibition. More details on page 48.

Room	Palace Restaurant A	
Session	**Interactive Session 1A**	
Chairs	Hiroshi Nishikawa Osaka University, Japan Toni Mattila Business Finland, Finland	
15:15	Investigating the Fine Microstructure of Mn-doped SnAgCu Solder Alloys by Selective Electrochemical Etching Oliver Krammer[1], Tamás Hurtony[1] *1: Budapest University of Technology and Economics, Hungary*	Anisotropic Conductive Film (ACF) Bonding: Effect of Interfaces on Contact Resistance Giang Minh Nghiem[1], Knut E. Aasmundtveit[1], Helge Kristiansen[2], Molly Bazilchuk[2] *1: University of South-Eastern Norway; 2: Conpart AS, Norway*
	PCM-based Thermal Buffer Coating for High Temperature Applications Jacob Maxa[1], Andrej Novikov[1], Mathias Nowottnick[1], Matthias Heimann[2], Kay Jarchoff[2] *1: University of Rostock, Germany; 2: Siemens AG, Germany*	Morphology Variations of Primary Cu_6Sn_5 Intermetallics in Lead-Free Solder Balls Maik Müller[1], Iuliana Panchenko[1], Steffen Wiese[2], Klaus-Jürgen Wolter[1] *1: Technische Universität Dresden, Germany; 2: Saarland University, Germany*
	Electrodeposition of Gold Electrode on Silicon Wafers for Submillimeter-wave Devices Mikiko Saito[1], Hiroyuki Seto[2], Yoshiyuki Inoue[2], Jiro Hirokawa[3] *1: Waseda University, Japan; 2: Kyoto University, Japan; 3: Tokyo Institute of Technology, Japan*	In-situ Characterization of Thin Polyimide Films Used for Microelectronic Packaging Frank Windrich[1], Mikhail Malanin[2], Eva Bittrich[2], Alexander Schwarz[1], Klaus-Jochen Eichhorn[2], Brigitte Voit[2] *1: Fraunhofer IZM, Germany; 2: Leibniz-Institut für Polymerforschung Dresden e. V., Germany*
	Cold-rolled Copper Trace Performance in PCB's and the Influence of Thermal Ageing Adam Yuile[1], Steffen Wiese[1] *1: Saarland University, Germany*	Light-weight Compressible and Highly Thermal Conductive Graphene-based Thermal Interface Material Nan Wang[1], Shujing Chen[2], Amos Nkansah[1], Lilei Ye[1], Johan Liu[2,3] *1: SHT Smart High Tech AB, Sweden; 2: Shanghai University, China; 3: Chalmers University of Technology, Sweden*

17:00	**Coffee break** Coffee and snacks will be served in the exhibition area located in **Foyer** and in **Bellevue 1** as well as in **Palace Restaurant A** and **Atrium**.

Palace Restaurant A

INTS1A

Interactive Session is based on a poster exhibition, where audience and speaker can discuss the presented results during the whole session. Posters are shown during both session parts A and B. In addition speakers give a short introduction to their posters topic scheduled as follows.

Characterization of Moisture Uptake in Microelectronics Packaging Materials
Fabian Huber[1,2], Harald Etschmaier[1], Archim Wolfberger[1], Anderson Singulani[1], Peter Hadley[2]
1: ams AG, Austria; 2: Graz University of Technology, Austria

Ultra-thin Actives for Embedded Components: Halfway Between Thin Film Technology and Embedded Surface Mounted Device
Mickael Balmont[1], Isabelle Bord Majek[1], Yves Ousten[1]
1: University of Bordeaux, France

Copper-based Graphene Nanoplatelet Composites as Interconnect for Power Electronics Pacakging
Jing Wang[1], Zhaoxia Zhou[1], Wen-Feng Lin[1], Changqing Liu[1], Behzad Ahmadi[2], Lee Empringham[2]
1: Loughborough University, UK; 2: University of Nottingham, UK

Investigating the Fine Microstructure of Mn-doped SnAgCu Solder Alloys by Selective Electrochemical Etching	15:15
PCM-based Thermal Buffer Coating for High Temperature Applications	15:23
Electrodeposition of Gold Electrode on Silicon Wafers for Submillimeter-wave Devices	15:31
Cold-rolled Copper Trace Performance in PCB's and the Influence of Thermal Ageing	15:38
Anisotropic Conductive Film (ACF) Bonding: Effect of Interfaces on Contact Resistance	15:46
Morphology Variations of Primary Cu_6Sn_5 Intermetallics in Lead-Free Solder Balls	15:54
In-situ Characterization of Thin Polyimide Films Used for Microelectronic Packaging	16:02
Light-weight Compressible and Highly Thermal Conductive Graphene-based Thermal Interface Material	16:10
Characterization of Moisture Uptake in Microelectronics Packaging Materials	16:18
Ultra-thin Actives for Embedded Components: Halfway Between Thin Film Technology and Embedded Surface Mounted Device	16:26
Copper-based Graphene Nanoplatelet Composites as Interconnect for Power Electronics Packaging	16:34

Please visit the Industrial Exhibition. More details on page 48.

Room	Bellevue 2	Bellevue 3
Session	AP2	DT2
Chairs	Beth Keser Intel Germany Steffen Kröhnert Amkor Technology, Germany	Chris Bailey University of Greenwich, UK Rainer Dudek Fraunhofer ENAS, Germany
17:30	Characterization of Electromigration Effects in RDL of Wafer Level Fan-In and Fan-Out Packaging Using a Novel Analysis Approach André Cardoso[1], Sofia Martins[1], Andrea Gouvea[1] *1: R&D Department ATEP – Amkor Technologies Portugal*	Utilizing Thermo-Mechanical CPI Simulation to Define a 7 nm Package Envelope Thiagarajan Raman[1], Scott Pozder[1], Carole Graas[1], Himani Suhag Kamineni[1] *1: GLOBALFOUNDRIES, Malta, USA*
18:00	Compact LTCC Packaging and Printing Technologies for Sub-THz Modules Martin Ihle[1], Steffen Ziesche[1], Christian Zech[2], Benjamin Baumann[2] *1: Fraunhofer Institute for Ceramic Technologies and Systems IKTS, Dresden, Germany; 2: Fraunhofer Institute for Applied Solid State Physics, Freiburg*	Experimental and Numerical Study of Uniaxial-Stress Effects on DC Characteristics of pMOSFETs Masaaki Koganemaru[1], Kazuya Hidaka[1], Toru Ikeda[1], Noriyuki Miyazaki[2] *1: Kagoshima University, Japan; 2: Green Electronics Research Institute, Japan*
18:25	Embedding and Interconnecting of Ultra-Thin RF Chip in Combination with Flexible Wireless Hub in Polymer Foil Golzar Alavi[1], S. Özbek[2], M. Rasteh[3], M. Grözing[2], M. Berroth[2], J. Hesselbarth[3], J. N. Burghartz[1] *1: Inst. for Nano-and Microelectrical System, 2: Inst. of Electrical and Optical Communications Engineering, 3: Inst. of Radio Frequency Technology – University of Stuttgart, Germany*	An Approximate Numerical Method for the Prediction of Plastic Strain in Layered Structures Kenneth C. Nwanoro[1], Hua Lu[1], Chuyan Yin[1], Chris Bailey[1] *1: University of Greenwich London, UK*
18:50	Process Technology and Integration of an LED Driver using Chip-embedding Technology Andreas Munding[1], Martin Gruber[1], Klaus Pressel[1], Boris Plikat[1], Michael Vogt[2], Peter Fruehauf[3] *1: Infineon Technologies AG Regensburg, Germany; 2: OSRAM GmbH Garching, Germany; 3: Siemens AG Berlin, Germany*	Predictive Modeling of Competing Failure Mechanisms using a Dedicated Constitutive Relation for Solder Alloy Michiel van Soestbergen[1], Jeroen J.M. Zaal[1] *1: NXP Semiconductors Nijmegen, the Netherlands*

19:30	**Welcome Reception** All conference attendees, exhibitors, officials and sponsors are invited to join the Welcome Reception. Time to network, relax and enjoy food and drinks. Detailed information will be given in time during sessions.

Palace Restaurant B	Boardroom 1/2	Room
FE2	**OP2**	Session
Nenad Marjanovic CSEM, Switzerland James Watkins University of Massachusetts, USA	Ulrich Fischer-Hirchert Univ. of Applied Science Wernigerode, Germany Maria Chiara Ubaldi Fondazione CIFE, Italy	Chairs
Multi-Chip Patch in Low Stress Polymer Foils based on an Adaptive Layout for Flexible Sensor Systems Björn Albrecht[1], Golzar Alavi[2], Mourad Elsobky[1], Saleh Ferwana[1], Ulrike Passlack[1] , Christine Harendt[1], Joachim N. Burghartz[1] *1: IMS CHIPS, Germany; 2: University of Stuttgart, Germany*	Wafer Level Through Polymer Optical Vias (TPOV) Enabling High Throughput of Optical Windows Manufacturing Zigiao Huang[1], R.H. Poelma[1], S. Vollebregt[1], M.H. Koelink[2], E. Boschman[2], R. Kropf[3], M. Gallouch[3], G.Q. Zhang[1] *1: Delft University of Technology, The Netherlands; 2: Advanced Packaging Center Duiven, The Netherlands; 3: iC-Haus Bodenheim, Germany*	17:30
Lifetime and Reliability of Flexible Aqueous Supercapacitors: Constant Voltage Floating and Bending Experiments Jari Keskinen[1], Suvi Lehtimäki[1], Anna Railanmaa[1], Thomas Kraft[1], Manu Kujala[1], Terho Kololuoma[2], Matti Mäntysalo[1], Donald Lupo[1] *1: Tampere University of Technology, Finland; 2: VTT Technical Research Centre of Finland Ltd*	Hermetic Wafer Level Packaging of LED Modules with Phosphor Ceramic Converter for White Light Applications based on TSV Technology Kai Zoschke[1], Yann Eichhammer[1], Hermann Oppermann[1], Charles-Alix Manier[1], Marius van Dijk[1], Constanze Weber[1], Matthias Hutter[1] *1: Fraunhofer IZM, Germany*	18:00
High Performance Microbatteries for Integrated Power via Nanoimprinting of 3-D Electrodes Wenhao Li[1], Troels Christiansen[2], Bo Iversen[2], James J. Watkins[1] *1: University of Massachusetts Amherst, USA; 2: Aarhus University, Denmark*	Presentation of Different Fine Pitch Interconnection Technologies Developed for Optic Applications Gilles Lasfargues[1], Bertrand Chambion[1], Marion Volpert[1], Frederic Berger[1], Divya Taneja[1], David Henry[1] *1: CEA LETI, France*	18:25
Thermosonic-Adhesive (TS-A) Integration of Flexible Integrated Circuits on Flexible Plastic Substrates Guangbin Dou[1], Andrew S. Holmes[1], Brian Cobb[2], Stephen Devenport[2], Anna Jeziorska-Chapman[2], Jake Meeth[2], Richard Price[2] *1: Imperial College London, UK; 2: PragmatIC Printing Limited, UK*	Femtosecond Pulsed Laser for Advanced Photonic Packaging Quentin Hivin[1], Jean Marc Boucaud[1,2], Flavie Braud[1], Cédric Durand[2], Frédéric Gianesello[2], Davide Bucci[3], Jean François Robillard[1], Jean Emmanuel Broquin[3], Christophe Gaquière[1], Emmanuel Dubois[1] *1: Université Lille, France; 2: STMicroelectronics, France; 3: Université de Grenoble Alpes, France*	18:50

Note about Boardroom 1/2: Presentations will be given in Boardroom 1. As an addition to capacity there will be a real-time video and audio broadcast to Boardroom 2.

Please visit the Industrial Exhibition. More details on page 48

Room	Palace Restaurant A	
Session	**Interactive Session 1B**	
Chairs	Derek Braden Aptiv Services UK Ltd, UK Ricky Lee Hong Kong University of Science and Technology	
17:30	Development of a Time Efficient Method to Enhance the Process of Parallel Lapping Sze Yee Tan[1], Chiu Soon Wong[1], Chea Wee Lo[1] *1: Infineon Technologies, Malaysia*	Influence of Environmental Factors like Temperature and Humidity on MEMS Packaging Materials Mahesh Yalagach[1], P. F. Fuchs[1], I. Mitev[1], T. Antretter[2], M. Feuchter[2], A. Wolfberger[3], T. Qi[4] *1: Polymer Competence Center Leoben GmbH, Austria; 2: Montanuniversitaet Leoben, Austria; 3: ams AG, Austria; 4: AT&S AG, Austria*
	Delamination Detection in an Electronic Package by Means of a Newly Developed Delamination Chip Based on Thermal Pixel (Thixel) Array A. Kumar[1], M. Schulz[1], S. Sheva[1], Jürgen Keller[1], V. Bader[2], M. Wöhrmann[2], J. Bauer[2], D. May[3], B. Wunderle[3] *1: AMIC GmbH, Germany; 2: Fraunhofer IZM, Germany; 3: Chemnitz University of Technology, Germany*	Accelerated Vibrational Fatigue Testing of Thin Aluminum and Copper Films at Different Temperatures Valentina Osipova[1], Bernhard Wunderle[1], Jörg Arnold[1], Jens Heilmann[1], Trideep Mahanta[1] *1: Chemnitz University of Technology, Germany*
	Silver Sintering in Power Electronics: The State of the Art in Material Characterization and Reliability Testing Marco Schaal[1], Markus Klingler[1], Bernhard Wunderle[2] *1: Robert Bosch GmbH, Germany; 2: Technische Universität Chemnitz, Germany*	Reliability of 3D Additive Manufactured Packages Sebastian Lüngen[1], Tobias Tiedje[1], Karsten Meier[1], Krzysztof Nieweglowski[1], Karlheinz Bock[1] *1: Technische Universität Dresden, Germany*
	Corrosion Mechanism in Metallization Systems for Printed Circuit Boards Sandy Klengel[1], Tino Stephan[1], Bolko Mühs-Portius[1], Robert Klengel[1] *1: Fraunhofer IMWS, Germany*	Non-destructive Evaluation and Life Monitoring of Solder Joints in Area Array Packaging Adeniyi A. Olumide[1], Kangkana Baishya[1], Guang-Ming Zhang[1], Derek R. Braden[1], David M. Harvey[1] *1: Liverpool John Moores University, UK*

19:30	**Welcome Reception** All conference attendees, exhibitors, officials and sponsors are invited to join the Welcome Reception. Time to network, relax and enjoy food and drinks. Detailed information will be given in time during sessions.

Palace Restaurant A

INTS1B

Interactive Session is based on a poster exhibition, where audience and speaker can discuss the presented results during the whole session. Posters are shown during both session parts A and B. In addition speakers give a short introduction to their posters topic scheduled as follows.

Fatigue Crack Growth Analysis of Interface Between Lead Frame and Molding Compound
Erkan Bektas[1], Katrin Broermann[1], Sascha P. Brumm[1], Goran Pecanac[1], Sven Rzepka[2], Christian Silber[1], Bernhard Wunderle[3]
1: Robert Bosch GmbH, Germany; 2: Fraunhofer ENAS, Germany; 3: Technical University of Chemnitz, Germany

Influences of SMD Package and Substrate Warpage on Quality and Reliability – Measurement, Effects and Counteractions
Heinz Wohlrabe[1], Karsten Meier[1], Oliver Albrecht[1]
1: Technische Universität Dresden, Germany

Thermo-Mechanical Measurement Approach of Ag-sintered Joints for Power Electronics
René Metasch[1], Karsten Meier[2], Mike Röllig[1]
1: Fraunhofer IKTS, Germany; 2: Technische Universität Dresden, Germany

Development of a Time Efficient Method to Enhance the Process of Parallel Lapping	17:30
Delamination Detection in an Electronic Package by Means of a Newly Developed Delamination Chip Based on Thermal Pixel Array	17:38
Silver Sintering in Power Electronics: The State of the Art in Material Characterization and Reliability Testing	17:46
Corrosion Mechanism in Metallization Systems for Printed Circuit Boards	17:54
Influence of Environmental Factors like Temperature and Humidity on MEMS Packaging Materials	18:02
Accelerated Vibrational Fatigue Testing of Thin Aluminum and Copper Films at Different Temperatures	18:10
Reliability of 3D Additive Manufactured Packages	18:18
Non-destructive Evaluation and Life Monitoring of Solder Joints in Area Array Packaging	18:26
Fatigue Crack Growth Analysis of Interface Between Lead Frame and Molding Compound	18:34
Influences of SMD Package and Substrate Warpage on Quality and Reliability – Measurement, Effects and Counteractions	18:42
Thermo-Mechanical Measurement Approach of Ag-sintered Joints for Power Electronics	18:50

19:30	**Welcome Reception** All conference attendees, exhibitors, officials and sponsors are invited to join the Welcome Reception. Time to network, relax and enjoy food and drinks. Detailed information will be given in time during sessions.

Room	Bellevue 2	Bellevue 3
Session	**AP3**	**MAT1**
Chairs	Björn Böhme Global Foundries, Germany Jürgen Wilde IMTEK, University Freiburg, Germany	Mike Röllig Fraunhofer IKTS, Germany Nihal Sinnadurai IMAPS Europe
8:30	Thermomechanical Reliability of Large Wafer Level Chip Scale Packages (LWLCSP) under Thermal Cycling Qualification Test Balaji Nandhivaram Muthuraman[1], Baltazar Canete[1] *1: Dialog Semiconductor GmbH, Germany*	Control for Au-Ag Nanoporous Structure by Electrodeposition and Dealloying Mikiko Saito[1], Jun Mizuno[1], Shunichi Koga[2], Hiroshi Nishikawa[2] *1: Waseda University, Japan; 2: Osaka University, Japan*
9:00	High Density Interconnect Processes for Panel Level Packaging Andreas Ostmann[1], Friedrich-Leonhard Schein[2], Michael Dietterle[3], Marc Kunz[4], Klaus-Dieter Lang[1] *1: Fraunhofer IZM, Germany; 2: Technical University of Berlin, Germany; 3: Dr.-Ing. Max Schlötter GmbH & Co. KG, Germany; 4: Schmoll Maschinen GmbH, Germany*	Novel Pre-applied Under-fill Material Specialized for Multiple Die Bonding Process Masashi Okaniwa[1], Takenori Takiguchi[1], Kohei Higashiguchi[1], Takahito Sekido[1], Katsutoshi Ihara[1], Tsuyoshi Kida[1], Shu Yoshida[1], Toyoji Oshima[1] *1: Mitsubishi Gas Chemical Company, Inc., Japan*
9:25	Development of a Wafer Level Packaging Technology for High Voltage Applications Marion Volpert[1], A. Aitmani[1], A. Gasse[1], B. Soulier[1], P. Peray[1], A. Vandeneynde[1], B. Chambion[1], D. Henry[1], F. Levy[1], F. Mercier[2], P. Rueda[2], V. Beix[2], T. Lacave[2] *1: Université Grenoble Alpes, CEA, LETI, MINATEC Campus, France; 2: ALEDIA SAS, France*	Thermal Characterization of Thermal Interface Materials using the Three-Omega Method Corinna Grosse[1], M. Abo Ras[1], A. Varpula[2], K. Grigoras[2], D. May[3], M. Prunnila[2], B. Wunderle[3] *1: Berliner Nanotest und Design GmbH, Germany; 2: VTT Technical Research Centre of Finland Ltd, Finland; 3: Technische Universität Chemnitz, Germany*
9:50	Roles and Requirements of Electronic Packaging in 5G Ivan Ndip[1], Klaus-Dieter Lang[1,2] *1: Fraunhofer IZM, Germany; 2: Technische Universität Berlin, Germany*	3D-Printed Eco-Friendly and Cost-Effective Wireless Platforms Xiaochen Chen[1], Han He[1], Leena Ukkonen[1], Johanna Virkki[1] *1: Tampere University of Technology, Finland*

10:15	**Coffee break** Coffee and snacks will be served in the exhibition area located in **Foyer** and in **Bellevue 1** as well as in **Palace Restaurant A** and **Atrium**.

Palace Restaurant B	Boardroom 1/2	Room
RE1	**MEMS1**	Session
Bernhard Wunderle TU Chemnitz, Germany Vesa Vuorinen Aalto University, Finland	Markku Tilli Okmetic, Finland Christophe Zinck ASE Group, France	Chairs
Spatially Resolved, Non-destructive in-situ Detection of Interface Degradation by Remote Electrical Readout of an On-chip Thermal Pixel (Thixel) Matrix B. Wunderle[1], D. May[1], M. Abo Ras[2], C. Grosse[2], M. Wöhrmann[3], V. Bader[3], J. Keller[4] *1: TU Chemnitz, Germany; 2: Berliner Nanotest & Design GmbH, Germany; 3: Fraunhofer IZM, Germany; 4: AMIC GmbH, Germany*	Flip-chip Die Attachment for High-temperature Pressure Sensor Packages up to 500 °C Nilavazhagan Subbiah[1], Qingming Feng[1], Kevin Ali Beltran Ramirez[1], Niclas Feil[1], Jürgen Wilde[1], Gudrun Bruckner[2] *1: University of Freiburg, Germany; 2: CTR AG, HIT, Austria*	8:30
Importance of Creep Fatigue Interaction in Reliability of Solder Joints Stéphane Zanella[1], Aurélien Lecavelier des Etangs-Levallois[1], Eric Charkaluk[2], Wilson Carlos Maia Filho[1], Andrei Constantinescu[2] *1: Thales Global Services SAS, France; 2: Ecole Polytechnique Palaiseau, France*	Micro Heat Pipe Design and Fabrication on LTCC Malika Tlili[1], Maïna Sinou[1], Camilla Kärnfelt[1], Daniel Bourreau[1], Alain Peden[1] *1: IMT Atlantique, France*	9:00
Effect of PCB stack-up on Temperature Cycling Reliability of WLCSP Romuald Roucou[1], J.J.M Zaal[1], R.T.H. Rongen[1], P.J. van der Wel[1] *1: NXP Semiconductors Nijmegen, The Netherlands*	Fabrication and Testing of MEMS Technology Based Thermoelectric Generator Alexander Korotkov[1], Vera Loboda[1], Sergey Dzyubanenko[2], Evgeniy Bakulin[2] *1: St.Petersburg Polytechnic University, Russia; 2: JSC "Avangard Saint-Petersburg, Russia*	9:25
Flex Cracking of Multilayer Ceramic Capacitors: Experiments on Fracture Propagation Joseph Al Ahmar[1], Erik Wiss[1], Steffen Wiese[1] *1: Saarland University, Germany*	Critical Issues in Tunable Mirror Assembly and Manufacturing Aldo Righetti[1], Maria Chiara Ubaldi[1], Lucia Ferrario[1], Giorgio Grasso[1] *1: Fondazione CIFE, Italy*	9:50

Note about Boardroom 1/2: Presentations will be given in Boardroom 1. As an addition to capacity there will be a real-time video and audio broadcast to Boardroom 2.

Please visit the Industrial Exhibition. More details on page 48.

Room	Palace Restaurant A	
Session	**Interactive Session 2A**	
Chairs	André Cardoso Amkor, Portugal Jean Charles Soriau CEA LETI, France	
8:30	Non-destructive Characterisation of Flexible Type Material using a White Light Interferometer Chiu Soon Wong[1], Sze Yee Tan[1], Chang Hui Tan[1] *1: Infineon Technologies, Malaysia*	Intelligent Power Module Featuring Optimised Active Gate Driver and IGBT Module Integration for Electric Vehicle Application Mingliang Jiao[1], Yaqing Ma[1], Jun Yu[1], Jia Xie[2], Pin Zeng[1], Zhenlong Zhao[1] *1: Zhuzhou CRRC Times Electric UK Innovation Center, UK; 2: Hunan CRRC Times Electric Vehicle Co., Ltd, China*
	Investigations of BGA Components' Balls Remanufacturing Techniques for Circular Economy Applications Janusz Sitek[1], Marek Koscielski[1], Aneta Arazna[1], Kamil Janeczek[1], Wojciech Steplewski[1] *1: Tele and Radio Research Institute Warsaw, Poland*	Printed Thick Copper Films for Power Applications Jan Reboun[1], Jiri Hlina[1], Radek Soukup[1], Jan Johan[2] *1: University of West Bohemia Pilsen, Czech Republic; 2: ELCERAM a.s. Hradec Kralove, Czech Republic*
	UV Assisted Chip-on-Wafer Direct Transfer Bonding (CoW DTB) Yoichiro Kurita[1], Hiroshi Uemura[1], Kazuya Ohira[1], Kaori Warabi[1], Hideto Furuyama[1], Miki Inamura[2], Yasuhide Kakumoto[2], Tomoyuki Abe[2] *1: Toshiba Corporation, Japan; 2: Ayumi Industry, Co., Ltd, Japan*	Microstructural and Chemical Investigation of Dielectric Breakdown Areas in Engineering Plastics Rico Bernhardt[1], Bianca Böttge[1], Sandy Klengel[1], Michael Bron[2], Sebastian Wels[3], Albert Claudi[3] *1: Fraunhofer IMWS, Germany; 2: Martin-Luther-Universität Halle-Wittenberg, Germany; 3: University of Kassel, Germany*
	Interfacial Reaction of Sn-Ag-Cu-Ni Solder/Cu Joints by Laser Process Hiroshi Nishikawa[1], Ryo Matsunobu[1] *1: Osaka University, Japan*	Thermographic Inspection Method for Quality Assessment of Power Semiconductors in the Manufacture of Power Electronics Modules Michael Schaulin[1], Martin Oppermann[1], Thomas Zerna[1] *1: Technische Universität Dresden, Germany*

10:15	**Coffee break** Coffee and snacks will be served in the exhibition area located in **Foyer** and in **Bellevue 1** as well as in **Palace Restaurant A** and **Atrium**.

Palace Restaurant A

INTS2A

Interactive Session is based on a poster exhibition, where audience and speaker can discuss the presented results during the whole session. Posters are shown during both session parts A and B. In addition speakers give a short introduction to their posters topic scheduled as follows.

Non-destructive Characterisation of Flexible Type Material using a White Light Interferometer	8:30
Investigations of BGA Components' Balls Remanufacturing Techniques for Circular Economy Applications	8:38
UV Assisted Chip-on-Wafer Direct Transfer Bonding (CoW DTB)	8:46
Interfacial Reaction of Sn-Ag-Cu-Ni Solder/Cu Joints by Laser Process	8:54
Intelligent Power Module Featuring Optimised Active Gate Driver and IGBT Module Integration for Electric Vehicle Application	9:02
Printed Thick Copper Films for Power Applications	9:10
Microstructural and Chemical Investigation of Dielectric Breakdown Areas in Engineering Plastics	9:18
Thermographic Inspection Method for Quality Assessment of Power Semiconductors in the Manufacture of Power Electronics Modules	9:26
Plasma Dicing Technology and Total Process	9:34
Step Cut Process of a Multilayered PCB with a Metal Defined Package Edge	9:42

Plasma Dicing Technology and Total Process

James Weber[1], Masaru Nonomura[2], Atsushi Harikai[2]
1: Panasonic Industry Europe GmbH, Germany; 2: Panasonic Smart Factory Solutions Co., Ltd., Japan

Step Cut Process of a Multilayered PCB with a Metal Defined Package Edge

David Bonnici[1], Brenda Farrugia[1]
1: ST Microelectronics, Malta

Please visit the Industrial Exhibition. More details on page 48.

Room	Bellevue 2	Bellevue 3
Session	AP4	MAT2
Chairs	Andreas Munding Infineon Technologies, Germany Heinz Wohlrabe TU Dresden, Germany	Jan Felba University Wroclaw, Poland Nan Wang SHT Smart High Tech AB
10:45	Miniaturized Printed Wiring Board Consisting of Polyimide Layers and Three Embedded Integrated Circuit Chips in Stacked Configuration Shunsuke Sato[1], Koji Munakata[2], Masakazu Sato[1], Nobuki Ueta[1], Yoshio Nakao[1], Osamu Nakao[1] *1: Fujikura Ltd., Japan; 2: Fujikura Europe Ltd., UK*	Flux-Induced Porous Structures in Cu-SnAg Solid-Liquid-Interdiffusion Microbump Interconnects Jörg Meyer[1], Prathamesh Jayant Upasani[1], Steffen Bickel[1], Iuliana Panchenko[1,2], M. Jürgen Wolf[2] *1: Technische Universität Dresden, Germany; 2: Fraunhofer Institute for Reliability and Microintegration - ASSID, Germany*
11:15	TCB Optimization for Stacking Large Thinned Dies with 40 and 20 µm Pitch Microbumps Carine Gerets[1], Jaber Derakhshandeh[1], Pieter Bex[1], Melina Lofrano[1], Vladimir Cherman[1], Tom Cochet[1], Kenneth June Rebibis[1], Gerald Beyer[1], Andy Miller[1], Eric Beyne[1] *1: Imec, Belgium*	Evaluation of Silver and Copper Sintering of First Level Interconnects for High Power LEDs Sri Krishna Bhogaraju[1], Alexander Hanß[1], Maximilian Schmid[1], Gordon Elger[1], Fosca Conti[2] *1: Ingolstadt University of Applied Sciences, Germany; 2: University of Padova, Italy*
11:40	Study of the Influence of Material Properties and Geometric Parameters on Warpage for Fan-Out Wafer Level Packaging Abdellah Salahouelhadj[1], Mario Gonzalez[1], Arnita Podpod[1], Kenneth June Rebibis[1], Eric Beyne[1] *1: Imec, Belgium*	Potential of BiSn Solders for High-Temperature Electronics Andrej Novikov[1], Mathias Nowottnick[1] *1: University of Rostock, Germany*
12:05	High-Q 3D-IPD Diplexer with High Aspect Ratio Cu Pillar Inductor Sheng-Chi Hsieh[1], Cheng-Yuan Kung[1], Teck Chong Lee[1], Hung-Yi Lin[1], Pao-Nan Lee[1], Chen-Chao Wang[1] *1: ASE Group, Taiwan*	High Reliability Lead-free Alloys for Performance-Critical Applications Pritha Choudhury[1], Suresh Telu[1], Anil Kumar[1], Morgana Ribas[1], Siuli Sarkar[1] *1: Alpha Assembly Solutions, India*

12:30	**Lunch break** Lunch buffet will be served in the exhibition area located in **Foyer** and in **Bellevue 1** as well as in **Palace Restaurant A** and **Atrium**.

Palace Restaurant B	Boardroom 1/2	Room
PE1	**MEMS2**	Session
Kay Essig ASE Group, Germany Jürgen Schuderer ABB Corporate Research, Switzerland	Hemant Desai Intel, USA Mervi Paulasto-Kröckel Aalto University, Finland	Chairs
Heterogeneous Integration of Vertical GaN Power Transistor on Si Capacitor for DC-DC Converters Zechun Yu[1,2], S. Zeltner[1], N. Boettcher[1], G. Rattmann[1], J. Leib[1], C. F. Bayer[1,2], A. Schletz[1], T. Erlbacher[1,2], L. Frey[1,2] *1: Fraunhofer IISB, Germany; 2: Friedrich-Alexander University Erlangen-Nuremberg, Germany*	Metal Films for MEMS Pressure Sensors: Comparison of Al, Ti, Al-Ti Alloy and Al/Ti Film Stacks Elizaveta Vereshchagina[1], Erik Poppe[1], Kari Schjølberg-Henriksen[1], Markus Wöhrmann[2], Sigurd Moe[1] *1: SINTEF Digital, Norway; 2: Fraunhofer IZM, Germany*	10:45
High Temperature Resistant Interconnection for SiC Power Devices Using Ni Micro-electroplating and Ni Nano Particles Kohei Tatsumi[1], Yasunori Tanaka[1], Tomonori Iizuka[1], Keiko Wada[1], Minoru Fukumori[1], Isamu Morisako[1], Yoon Jeongbin[1], Norihiro Murakawa[1] *1: Waseda University, Japan*	Ultrafast Miniaturized Pulsed Electron Gun for Time-Resolved Surface Measurements Dennis Epp[1], Gero Storeck[1], Simon Vogelgesang[1], Murat Sivis[1], Sascha Schäfer[1], Claus Ropers[1] *1: University of Göttingen, Germany*	11:15
Minimizing Form Factor and Parasitic Inductances of Power Electronic Modules: The p² Pack Technology Thomas Gottwald[1], Christian Roessle[1] *1: Schweizer Electronic AG, Germany*	Process Integration and Reliability of Wafer Level SLID Bonding for Poly-Si TSV capped MEMS Vesa Vuorinen[1], Glenn Ross[1], Heikki Viljanen[2], James Decker[2], Mervi Paulasto-Kröckel[1] *1: Aalto University, Finland; 2: VTT Technical Research Centre of Finland*	11:40
Study of a Topology of Low-Loss Magnetic Component for PCB-Embedding Yoann Pascal[1], Mickaël Petit[1], Denis Labrousse[1], François Costa[1] *1: Lab. SATIE, France*	Additive Manufacturing of Micro-scale Tunnels on a Silicon Substrate with in-situ UV LED Curing for MEMS Applications Shi-Wei Ricky Lee[1], Qianwen Xu[1], Jeffery Chi Chuen Lo[1] *1: Hong Kong University of Science & Technology, Hong Kong*	12:05

Note about Boardroom 1/2: Presentations will be given in Boardroom 1. As an addition to capacity there will be a real-time video and audio broadcast to Boardroom 2.

Please visit the Industrial Exhibition. More details on page 48.

Room	Palace Restaurant A	
Session	**Interactive Session 2B**	
Chairs	Jukka Hast VTT, Finland Oliver Krammer University Budapest, Hungary	
10:45	Printed Flexible FE Memory Array Testing System Shoude Chang[1], Yanguang Zhang[1], Badrou Reda Aich[1], Ye Tao[1] *1: National Research Council Canada*	Integration of Lighting Functionality within Textiles by Flexible OLED Jan Hesse[1], Christian May[1], Claudia Keibler-Willner[1] *1: Fraunhofer FEP, Germany*
	Hybrid (PI-PDMS) Superhydrophobic Wearable Dry-Patching Flexible and Transparent Substrate Yongjin Kim[1], Joon Yub Song[1], Jae Hak Lee[1], Seung Man Kim[1] *1: Korea Institute of Machinery and Materials, South Korea*	Development of PEB Face-Down Interconnect Process for Wearable Device Jae Hak Lee[1], Chung Woo Lee[1], Yong Jin Kim[1], Seung Man Kim[1], Jun-Yeob Song[1] *1: Korea Institute of Machinery and Materials, South Korea*
	Development of a Flexible Label Integrating a Silicon Bare Die Ahmad Itawi[1], Jean-Charles Souriau[1] *1: CEA – Leti, France*	Lateral Strain Force Sensitivity Measurements for Piezoelectric Polyvinylidenefluoridene Sensor Array Sampo Tuukkanen[1], Veikko Sariola[1] *1: Tampere University of Technology, Finland*
	Multilayer Plastic Substrate for Electronics Arttu Huttunen[1], Timo Kurkela[1], Kaisa-Leena Väisänen[1], Eveliina Juntunen[1] *1: VTT Technical Research Centre of Finland*	Evaluation of Nanoparticle Inks on Flexible and Stretchable Substrates for Biocompatible Application Martin Schubert[1], Y. Wang[1], M. Vinnichenko[2], L. Rebohle[3], M. Fritsch[2], T. Schumann[3], K. Bock[1] *1: Technische Universität Dresden, Germany; 2: Fraunhofer IKTS, Germany; 3: Helmholtz-Zentrum Dresden-Rossendorf, Germany*

12:30	**Lunch break** Lunch buffet will be served in the exhibition area located in **Foyer** and in **Bellevue 1** as well as in **Palace Restaurant A** and **Atrium**.

Palace Restaurant A

INTS2B

Interactive Session is based on a poster exhibition, where audience and speaker can discuss the presented results during the whole session. Posters are shown during both session parts A and B. In addition speakers give a short introduction to their posters topic scheduled as follows.

Printed Flexible FE Memory Array Testing System	10:45
Hybrid (PI-PDMS) Superhydrophobic Wearable Dry-Patching Flexible and Transparent Substrate	10:53
Development of a Flexible Label Integrating a Silicon Bare Die	11:01
Multilayer Plastic Substrate for Electronics	11:09
Integration of Lighting Functionality within Textiles by Flexible OLED	11:17
Development of PEB Face-Down Interconnect Process for Wearable Device	11:25
Lateral Strain Force Sensitivity Measurements for Piezoelectric Polyvinylidenefluoridene Sensor Array	11:33
Evaluation of Nanoparticle Inks on Flexible and Stretchable Substrates for Biocompatible Application	11:41
Stability of Fully Printed Flexible Thermistors under Static and Dynamic Thermal Stressing	11:49
LTCC-like Multilayer LCP-Technology for flexible RF-Circuits	11:57

Stability of Fully Printed Flexible Thermistors under Static and Dynamic Thermal Stressing

Silvan Pretl[1], Tomáš Syrový[2], David Kalaš[1]
1: University of West Bohemia Pilsen, Czech Republic; 2: University of Pardubice, Czech Republic

LTCC-like Multilayer LCP-Technology for flexible RF-Circuits

Jens Müller[1], T. Welker[1] and K. Schmitt[1]
1: Technische Universität Ilmenau, Germany

Please visit the Industrial Exhibition. More details on page 48.

Special Workshops

Room	Bellevue 2	Bellevue 3	Boardroom 1/2
13:30	Workshop A	Workshop B	Workshop D

15:00	**Coffee break** Coffee and snacks will be served in the exhibition area located in **Foyer** and in **Bellevue 1** as well as in **Palace Restaurant A** and **Atrium**.

Room	Bellevue 2	Bellevue 3	Boardroom 1/2
15:30	(A continued)	Workshop C	(D continued)

Title	**Workshop A - Heterogeneous Integration Roadmap**
Topic	Our Industry has reinvented itself through multiple disruptive changes in technologies, products and markets. With the rapid migration of logic, memory and applications to the Cloud infrastructures, Data Centers and 5G Networks, the Internet of Things (IoT) to Internet of Everything (IoE), Autonomous Vehicles, the proliferation of Smart Devices everywhere, and increasing interest in artificial intelligence (AI) & Virtual Reality (VR), the pace of innovation is increasing to meet these challenges. What are the paths forward? The IEEE Heterogeneous Integration Technology Roadmap (HIR) is sponsored by the IEEE Electronic Packaging Society (EPS), the Electron Devices Society (EDS), Photonics Society together with ASME EPPD and SEMI. It will address the future directions of heterogeneous integration technologies and applications serving future markets and applications, so very crucial to our profession, our industries, academic and research communities. Following the spirit of ITRS, the HIR is a pre-competitive technology roadmap provides long-term vision to identify the needs of future technology challenges, roadblocks, and potential solutions focused on system integration and broad market applications in order to accelerate progress for the broad electronics industry.
Agenda	**Welcome Messages** — Hubert Lakner (Fraunhofer IPMS) & Karlheinz Bock (TU Dresden) **Heterogeneous Integration Roadmap Overview** — Bill Chen (ASE) & Bill Bottoms (Third Millenium Test Solutions) **Opportunities & Challenges in Automotive Electronics Packaging** — Andreas Middendorf (Fraunhofer IZM) **Photonics Integration** — Gunnar Böttger (Fraunhofer IZM) **ITRW & Power Electronics Integration** — Pete Wilson (University of Bath) & Jing Zhang (Heraeus Electronics) **Heterogeneous Integration Roadmap TWG Panel** Panel Co - Moderators: Jean Trewhella (GLOBALFOUNDRIES) & Klaus Pressel (Infineon) **System-in-Package (SIP)** — Rolf Aschenbrenner (Fraunhofer IZM) **WLP & Fanout** — John Hunt (ASE) **Co-Design & Simulations** — Chris Bailey (University of Greenwich) **5G & Analog & Mixed Signal** — (to be confirmed) **Panel** (all speakers) **Q&A Session** **Wrap-Up** — Bill Bottoms & Bill Chen

Title	**Workshop B - Fan-Out Panel: Is the Industry Ready?**
Topic	Fan-out wafer-level packaging (FO-WLP) technologies have been developed across the industry over the past 15 years and have been in high volume manufacturing for over 8 years. FO-WLP has matured enough that it has come to a crossroads where it has the potential to change the electronic packaging industry by eliminating wire bond and bump interconnections, substrates, leadframes, and the traditional flip-chip or wire bond chip attach and underfill assembly technologies across multiple applications. The next step is economy of scale: the conversion from 300mm to panel! Panel Fan-Out has been an exciting topic for in the US and Asia for over 3 years and we are bringing that excitement to IEEE Electronics Package Society's Electronic System-Integration Technology Conference (ESTC). Panelists representing consortia, OSATs, materials suppliers, and market data research will all speak about how their company or consortium is addressing (or not addressing) the panel fan-out market and discuss the intersection with European markets such as automotive, IoT, and flexible electronics.
Panelists	**BETH KESER, Ph.D., a recognized global leader in the semiconductor packaging industry** with over 20 years of experience, received her B.S. degree in Materials Science and Engineering from Cornell University and her Ph.D. from the University of Illinois at Urbana-Champaign. Beth's excellence in developing revolutionary electronic packages for semiconductor devices has resulted in 27 patents and patents pending and over 40 publications in the semiconductor industry. Based in Munich, Germany, Beth is Director if the Components and Systems Solutions Department at **Intel Corporation** in the Communication Devices Group.
	TANJA BRAUN studied mechanical engineering at Technical University of Berlin and joined **Fraunhofer IZM** in 1999. Since 2000 she is working with the group Assembly & Encapsulation Technologies and since 2016 she is head of this group. In 2013 she received her doctorate degree from the TU of Berlin for the work focusing on humidity diffusion through particle-filled epoxy resins. Her recent research is focused on wafer and panel level packaging technologies and Tanja is leading the Fan-out Panel Level Packaging Consortium at Fraunhofer IZM Berlin. Tanja Braun holds also several patents in the field of advanced packaging. In 2014 she received the Fraunhofer IZM research award.
	JAN KELLAR joined **Deca Technologies** in 2010 where she is responsible for advanced wafer level package design including M-Series fan-out design using Adaptive Patterning™ dynamic lithography technology. Jan has over 25 years of experience working in the semiconductor industry specializing in Advanced Package Design. Prior to joining Deca Technologies, Ms. Kellar was Global IC Package Design Manager at Motorola and Freescale Semiconductor.
	JAN VARDAMAN is president and founder of **TechSearch International, Inc.**, which has provided market research and technology trend analysis in semiconductor packaging since 1987. She is the co-author of How to Make IC Packages, a columnist with Printed Circuit Design & Fab/Circuits Assembly, and the author of numerous publications on emerging trends in semiconductor packaging and assembly. She is a senior member of IEEE EPS and is an IEEE EPS Distinguished Lecturer. She is a member of SEMI, IMAPS, and MEPTEC. She received the IMAPS GBC Partnership award in 2012. Before founding TechSearch International, she served on the corporate staff of Microelectronics and Computer Technology Corporation (MCC), the electronics industry's first pre-competitive research consortium.
	MARION WEIGAND studied Chemical Engineering at the University of Applied Sciences in Darmstadt and jointed **DuPont** in 1987. She spent her 31 years with DuPont in the Electronic Materials business unit, mainly in the semiconductor materials group. In 1997 she was part of the foundation of Hitachi Chemical DuPont MicroSystems (HDMS), a Joint Venture between Hitachi Chemical and DuPont Electronics. Since 2000 she is Managing Director of the European HDMS legal entity with Technical Service and Sales Management experience in Europe and the USA for the HDMS product portfolio of liquid polymer coatings for various semiconductor applications. Additionally, Marion serves as the Chairperson of the Board of Directors & Country Leader of DuPont in Germany.

Special Workshops

Title	**Workshop C - Challenges for Advanced Packaging in the Dawn of Autonomous Driving**
Topic	This panel discussion focuses on the challenges for advanced packaging in the era of ADAS and the dawn of autonomous driving. Package choice, design, and materials impact the performance of Advanced Driver Assistance Systems (ADAS) sensors and the sensor fusion processors used to analyze sensor input. Fan-out wafer level packages (FO-WLPs) are used for automotive radar, but the package designs differ from those found in smartphones. What are the different design considerations for packages used in automotive vs. consumer, computing, and telecom? How important is co-design? Many sensor fusion processors are packaged in flip chip-plastic ball grid arrays (FC-PBGAs), but the materials used to fabricate the substrates differ from packages used for other applications. What failure modes are being observed? What reliability standards should be followed in qualifying packages for ADAS and autonomous driving? Does the industry need to meet Grade 0? Power dissipation requires thermal materials and solutions that can meet automotive reliability specifications. Are current material sets adequate? Are new materials needed and what are the requirements for these materials? A set of experts will address these issues and others in a dynamic discussion setting.
Panelists	**JAN VARDAMAN** is president and founder of **TechSearch International, Inc.**, which has provided market research and technology trend analysis in semiconductor packaging since 1987. She is the co-author of How to Make IC Packages, a columnist with Printed Circuit Design & Fab/Circuits Assembly, and the author of numerous publications on emerging trends in semiconductor packaging and assembly. She is a senior member of IEEE EPS and is an IEEE EPS Distinguished Lecturer. She is a member of SEMI, IMAPS, and MEPTEC. She received the IMAPS GBC Partnership award in 2012. Before founding TechSearch International, she served on the corporate staff of Microelectronics and Computer Technology Corporation (MCC), the electronics industry's first pre-competitive research consortium.
	KARLHEINZ BOCK studied electronics and communication engineering at the University of Saarbrücken, Germany. In 1994 he achieved the Dr.-Ing. degree in RF microelectronics from the University of Darmstadt, Germany. Since January 2001 until September 2014 he has been with the Fraunhofer IZM in Munich (since 2010 renamed to Fraunhofer EMFT), as head of the Polytronic and Multi-Functional Systems department. Since March 2008 until September 2014 he also served as professor of Polytronic Microsystems at the TU Berlin. He received in 2012 the Dr. honoris causa from Polytechnical University of Bukarest in Romania. Since October 2014 he serves as professor of Electronics Packaging and director of the **Institute for Electronic Packaging Technology (IAVT) at the TU Dresden.**
	THORSTEN MEYER is Principal Engineer Package Concept Engineering at **Infineon Technologies** in Regensburg, Germany, responsible for New Package Platforms and New Package Definition. Until March 2015 he was leading the Package Technology and Innovation department at Intel Mobile Communications (IMC) in Regensburg. Prior joining IMC, he was overall project leader for the development of Wafer Level Packaging Technologies at Infineon in Regensburg and earlier in Dresden. Thorsten Meyer is author of multiple publications and holds more than 140 patents and patent applications in the area of advanced packaging.
	(Additional panelists are invited.)

Title	**Workshop D - EuroPAT-MASIP - Recent advantages in electronics packaging**
Topic	EuroPAT-MASIP, ECSEL JU project, strives to increase the competitiveness and the global market share of the European semiconductor industry by fostering the competence and capabilities of semiconductor packaging. The three-year project's total budget is about 30 M€, with roughly half of it from ECSEL and national funding. Coordinated by Amkor technologies, Steffen Kröhnert, partners from nine European countries cover the semiconductor packaging, assembly and test value chain all the way from foundry, packaging, component tests to system tests till the end user. Focusing on fan-out wafer level packaging (FO-WLP), the project develops packages for six pilot products: WLAN front-end IC (NXP France), silicon photomultiplier (KETEK), automotive inertial sensor (Murata), next-generation WL camera (Valeo), 60 GHz radar sensor (InnoSenT) and a car tyre sensor (Nokian Tyres). In addition, the project develops a wide portfolio of technological building blocks for integration concepts. These include modelling and simulation, 3D MtM and SiP, packaging technologies, materials as well as test strategy and methods. The new equipment include e.g. plasma dicing technology.
Panelists	**HEIKKI KUISMA** graduated from the Helsinki University of Technology (now Aalto University) in 1978 with MS degree, electron physics as the major topic. Having worked in VTT, Vaisala Oy and VTI Technologies Oy (now Murata Electronics) he has over 40 years of experience in MEMS technologies and devices including all aspects of the device: MEMS, circuits and packaging. He was a long term Director of Advanced Development in VTI and Murata and is now partially retired but still working as Program Manager for development of selected advanced technologies. He has been a WP leader in many multi-party publicly funded projects. He is an author of tens of patent publications.
	THOMAS UHRMANN is director of business development at EV Group (EVG) where he is responsible for overseeing all aspects of EVG's worldwide business development. Specifically, he is focused on 3D integration, MEMS, LEDs and a number of emerging markets. Prior to this role, Uhrmann was business development manager for 3D and Advanced Packaging as well as Compound Semiconductors and Si-based Power Devices at EV Group. He holds an engineering degree in mechatronics from the University of Applied Sciences in Regensburg and a PhD in semiconductor physics from Vienna University of Technology.
	GHANSHYAM GADHIYA received his M.Sc. degree in Micro and nano systems, with a specialization in Finite element analysis of power module from Technical university of Chemnitz in 2013. Since 2014, he is working as a scientific researcher at the Micro materials center, Fraunhofer ENAS. His main research focus includes parametric finite element modelling, thermo-mechanical simulation and optimization of microelectronics packages using FE analysis. He has been also involved with several industrial projects for residual stress, humidity and vibrational analysis. His current research interests include fan-out wafer level packaging technologies based system-in-package and micro-electronics failure analysis.
	ANDRE CLAUSNER finished his Diplomingenieur degree in applied mechanics in 2007 and joined afterwards the International Research Training Group „Materials and Concepts for Advanced Interconnects" working in the field of advanced materials for microelectronics until 2010. He joined Fraunhofer IKTS in 2013 after completing his dissertation at the Technical University Chemnitz in physics, focusing on the area of nanoindentation. The goal of his doctoral work was the evaluation of nanoindentation methods for the determination of yield stresses in various classes of materials. He brings with him a vast knowledge in the field of mechanical materials behaviour and characterisation methods.
	CHRISTOPHER JOHNSTON is the business development manager for advanced packaging at Plasma-Therm. Christopher comes to Plasma-Therm from Intel Corporation, where he served 16 years in semiconductor Fab high volume manufacturing and assembly R&D. During his last 8 years at Intel, he was the dicing equipment development and supply chain engineer. Christopher dicing technology contributions include the leading wafer laser scribing solution advanced nodes (<10nm) and the most affordable plasma dicing-on-tape solution for small and thin devices. Christopher received a BS degree in Electronics Engineering from DeVry University, MBA and MPM from Keller. Recent publications include "Plasma dicing methods for thin wafers", Chip Scale Review (May-June 2016) and "Plasma Dicing for MEMS", MEPTEC Report (Fall 2016).

Room	Bellevue 2	Bellevue 3
Session	ASS1	MAT3
Chairs	Knut E. Aasmundtveit University of South-East Norway, Norway Thomas Zerna Technische Universität Dresden, Germany	Jens Müller TU Ilmenau, Germany Abdelhafid Zehri Chalmers University, Sweden
8:30	Applying Sintering and SLID Bonding for Assembly of GaN Chips Working at High Temperatures Marcin Mysliwiec[1], Ryszard Kisiel[1] *1: Warsaw University of Technology, Poland*	An in-situ Resistance Measurement to Extract IMC Resistivity and Kinetic Parameter of Alternative Metallurgies for 3D Stacking Lin Hou[1,2], J. Derakhshandeh[2], A. Radisic[2], M. Honore[2], J. De Coster[2], V. Cherman[2], P. Bex[2], K. J. Rebibis[2], G. Beyer[2], E. Beyne[2], I. De Wolf[1,2] *1: KU Leuven, Belgium; 2: IMEC, Belgium*
9:00	3D Multilayered Ceramics – Harsh Environment Interposer Technologies Expand into 3rd Dimension Steffen Ziesche[1], Christian Lenz[1], Axel Mueller-Koehn[1], Uwe Scheithauer[1], Uwe Partsch[1] *1: Fraunhofer IKTS, Germany*	Determination of Stress-Strain Properties Combining Small-Depth Nanoindentation and Numerical Simulation Simon Kuttler[1], Arian Grams[1], Saskia Huber[1], Hans Walter[1], Martin Schneider-Ramelow[2] *1: Fraunhofer IZM, Germany; 2: Technical University Berlin, Germany*
9:25	Digitally-driven Hybrid Manufacture of Ceramic Thick-film Substrates Jack Hinton[1], M. Mirgkizoudi, A. Campos-Zatarain[2], D. Flynn[2], R.A. Harris[1], R.W. Kay[1] *1: University of Leeds, UK; 2: Heriot-Watt University, UK*	Thermal Stability of High Temperature Pb-free Solder Interconnect Characterised by in-situ Electron Microscopy Zhaoxia Zhou[1], Li Liu[1], Changqing Liu[1] *1: Loughborough University, UK*
9:50	Packaging of Ultrathin Flexible Magnetic Field Sensors with thin Silicon and Polyimide Interposer Daniel Ernst[1], Marcel Wild[1], Thomas Zerna[1] *1: Technische Universität Dresden, Germany*	A Metal Interconnection Using a Direct Imaging Method for HySiF (Hybrid System in Flexible) Devices Joon Yub Song[1], Yongjin Kim[1], Jae Hak Lee[1], Seung Man Kim[1] *1: Korea Institute of Machinery and Materials, South Korea*

10:15	**Coffee break** Coffee and snacks will be served in the exhibition area located in **Foyer** and in **Bellevue 1** as well as in **Palace Restaurant A**.

Palace Restaurant B	Boardroom 1/2	Room
RE2	**PE2**	Session
Karsten Meier TU Dresden, Germany Romuald Roucou NXP, The Netherlands	Thomas Harder ECPE, Germany Matthias Heimann Siemens, Germany	Chairs
Chip-package-board Reliability of System-in-Package Using Laminate Chip Embedding Technology Based on Cu Leadframe Peter Fruehauf[1], Andreas Munding[2], Klaus Pressel[2], Michael Vogt[3], Patrick Schwarz[2] *1: Siemens AG, Germany; 2: Infineon Technologies AG, Germany; 3: OSRAM GmbH, Germany*	Power Electronic Assemblies on Printed Wiring Boards Mounted by Silver Sintering Alexander Schiffmacher[1], Lorenz Litzenberger[1], Juergen Wilde[1], Vladimir Polezhaev[2], Till Huesgen[2] *1: IMTEK University of Freiburg, Germany; 2: University of Applied Science Kempten, Germany*	8:30
LED Failure Localization Method due to Thermal Shock and Residual Stress Impact Safa Nocairi[1], Christine Roucoules[1], Sergio Saoo-Joao[2], Guillaume Kermouche[2], Helmut Klöcker[2] *1: Valeo lighting Systems, France; 2: University Lyon, France*	Multi Dies Simultaneous Bonding for Power Device with the Newly Developed Pressure Leveling Film Kazutaka Honda[1], Yuta Koseki[1], Tsuyoshi Ogawa[1], Toshihisa Nonaka[1] *1: Hitachi Chemical Co., Ltd., Japan*	9:00
Stress Analyses in HPC-Soldered Assemblies by Optical Measurement and FEA Rainer Dudek[1], Ralf Döring[1], Sven Rzepka[1], Timo Herberholz[2], Daniel Feil[2], Bettina Seiler[3], Lutz Scheiter[3], Christian Schellenberg[4], Sebastian Fritzsche[5] *1: Fraunhofer ENAS, Germany; 2: Robert Bosch GmbH, Germany; 3: CWM GmbH, Germany; 4: Siemens AG; Germany; 5: Heraeus, Germany*	Nonconchoidal Fracture in Power Electronics Substrates due to Delamination in Baseplate Solder Joints Allen Jose George[1], Marlies Breitenbach[1], Juergen Zipprich[1], Markus Klingler[1], Mathias Nowottnick[2] *1: Robert Bosch GmbH, Germany; 2: University of Rostock, Germany*	9:25
Temp.-dependent Adhesion Measurements of Die Attach Materials to Moulding Compounds and Lead Frame Surfaces Enabling Robust Pack. Designs Nadine Pflügler[1], Reinhard Pufall[1], Michael Goroll[1], Joachim Mahler[1], Georg M. Reuther[1], Bernhard Wunderle[2] *1: Infineon Technologies AG, Germany; 2: Chemnitz University of Technology, Germany*	Accurate, Versatile and Compact Transient Measurement System for Fast Thermal Package Characterization and Health Monitoring Pranav Panchal[1], Tobias von Essen[1], Mohamad Abo Ras[1], Corinna Grosse[1], Daniel May[2], Bernhard Wunderle[2] *1: Berliner Nanotest und Design GmbH, Germany; 2: Technische Universität Chemnitz, Germany*	9:50

Note about Boardroom 1/2: Presentations will be given in Boardroom 1. As an addition to capacity there will be a real-time video and audio broadcast to Boardroom 2.

Please visit the Industrial Exhibition. More details on page 48.

Room	Palace Restaurant A	
Session	**Interactive Session 3A**	
Chairs	Markus Detert University Magdeburg, Germany Malgorzata Jakubovska Warsaw University of Technology, Poland	
8:30	3D-MID for Space Etienne Hirt[1], Klaus Ruzicka[1] *1: Art of Technology AG Zurich, Switzerland*	Thermal Characterization of Endogenously Heated Printed Circuit Boards with Embedded Resistive Layers Dirk Seehase[1], Arne Neiser[2], Fred Lange[1], Andrej Novikov[1], Mathias Nowottnick[1] *1: University of Rostock, Germany; 2: SEHO Systems GmbH, Germany*
	Development and Analysis of High Temperature Stable Interconnections on Thick Films Using Micro Resistance Welding for Sensors and MEMS Paul Gierth[1], Lars Rebenklau[1] *1: Fraunhofer IKTS, Germany*	Textile-Integrated Stretchable Structures for Wearable Wireless Platforms Han He[1], Xiaochen Chen[1], Omid Mokhtari[2], Hiroshi Nishikawa[2], Leena Ukkonen[1], Johanna Virkki[1] *1: Tampere University of Technology, Finland, 2: Osaka University, Japan*
	Innovative Conductive Mesh Structure for the Protection of Security Electronic Circuits Daniel-Ciprian Vasile[1], Paul Mugur Svasta[1] *1: University POLITEHNICA of Bucharest, Romania*	Implementation of 3D Gesture Control System for Environmental Control Madalin Vasile Moise[1], Alin Gheorghita Mazare[2], Paul Mugur Svasta[1] *1: Polytechnic University of Bucharest, Romania; 2: University of Pitesti, Romania*
	Modified CNTs for NO_2 Detection Jiri Stulik[1], Tomas Blecha[1] *1: University of West Bohemia in Pilsen, Czech Republic*	

10:15	**Coffee break** Coffee and snacks will be served in the exhibition area located in **Foyer** and in **Bellevue 1** as well as in **Palace Restaurant A**.

Palace Restaurant A

INTS3A

Interactive Session is based on a poster exhibition, where audience and speaker can discuss the presented results during the whole session. Posters are shown during both session parts A and B. In addition speakers give a short introduction to their posters topic scheduled as follows.

3D-MID for Space	8:30
Development and Analysis of High Temp. Stable Interconn. on Thick Films Using Micro Resistance Welding for Sensors and MEMS	8:38
Innovative Conductive Mesh Structure for the Protection of Security Electronic Circuits	8:46
Modified CNTs for NO_2 Detection	8:54
Thermal Characterization of Endogenously Heated Printed Circuit Boards with Embedded Resistive Layers	9:02
Textile-Integrated Stretchable Structures for Wearable Wireless Platforms	9:10
Implementation of 3D Gesture Control System for Environmental Control	9:18

Please visit the Industrial Exhibition. More details on page 48.

Room	Bellevue 2	Bellevue 3
Session	ASS2	MAT4
Chairs	David Henry CEA-LETI, France Andreas Ostmann Fraunhofer IZM, Germany	Matthias Hutter Fraunhofer IZM, Germany Iuliana Panchenko TU Dresden, Germany
10:45	**Numerical and Statistical Investigation of Weld Formation in a Novel Two-dimensional Copper-copper Bonding Process** Collin Dymel[1], Paul Eichwald[1], Reinhard Schemmel[1], Tobias Hemsel[1], Michael Brökelmann[2], Matthias Hunstig[2], Walter Sextro[1] *1: University Paderborn, Germany; 2: Hesse GmbH Paderborn, Germany*	**Copper Die-Bonding Sinter Paste: Sintering and Bonding Properties** Dai Ishikawa[1], Hideo Nakako[1], Yuki Kawana[1], Chie Sugama[1], Motohiro Negishi[1], Yoshinori Ejiri[1], Suguru Ueda[1], Bao Ngoc An[2], Helge Wurst[2], Benjamin Leyrer[2], Thomas Blank[2], Marc Weber[2] *1: Hitachi Chemical Co. Ltd., Japan; 2: Karlsruhe Institute of Technology, Germany*
11:15	**Control a Joule-Heating Embedded Layer within a Printed Circuit Board** Arne Neiser[1], Dirk Seehase[2], Philipp Koschorrek[3], Andreas Reinhardt[1] *1: SEHO Systems GmbH, Germany; 2: University of Rostock, Germany; 3: Voith Turbo GmbH & Co. KG, Germany*	**Low-Temperature Sintering Bimodal Micro Copper- Nano Silver For Electrical Power Devices** Abdelhafid Zehri[1], Lilei Ye[2], Johan Liu[1,3] *1: Chalmers University of Technology, Sweden; 2: SHT Smart High Tech AB, Sweden; 3: Shanghai University, China*
11:40	**Controlling BGA Joint Microstructures Using Seed Crystals** Zhaolong Ma[1], Sergey Belyakov[1], Jingwei Xian[1], Tetsuro Nishimura[2], Keith Sweatman[2], Chris Gourlay[1] *1: Imperial College London, UK; 2: Nihon Superior Co., Ltd, Japan*	**Heat Capacitive PCB** Jonathan Silvano de Sousa[1], Sabine Liebfahrt[1], Bernhard Reitmaier[1], Maria Prutti[1], Bernd Schuscha[2], Qi Tao[1], Johann Nicolics[3], Michael Unger[3], Paul Fulmek[3] *1: AT&S AG, Austria; 2: Associated Student AT&S AG, Austria; 3: Technische Universität Wien, Austria*
12:05	**High Throughput R2R Printing, Testing and Assembly Processing of Flexible RGB LED Displays** Kimmo Keränen[1], Pentti Korhonen[1], Tuomas Happonen[1], Mikko Paakkolanvaara[1], Jouni Kangas[1], Kari Rönkä[1] *1: VTT Oulu, Finland*	**Tailoring the Cu_6Sn_5 Layer Texture with Ni Additions in Sn-Ag-Cu Based Solder Joints** Yuchen Hsu[1,2], G. Zeng[2], J.W. Xian[2], S.A. Belyakov[2], Christopher M. Gourlay[2] *1: Toshiba Corporation, Japan; 2: Imperial College London, UK*

12:30	**Lunch break** Lunch buffet will be served in the exhibition area located in **Foyer** and in **Bellevue 1** as well as in **Palace Restaurant A**.

Palace Restaurant B	Boardroom 1/2	Room
RE3	**ES1**	Session
Matthias Petzold Fraunhofer IMWS, Germany Olaf Wittler Fraunhofer IZM, Germany	Changqing Liu Loughborough University, UK Klaus-Jürgen Wolter TU Dresden, Germany	Chairs
Experimental Verification of FE-Models for Thermo-Mechanical Loading using Digital Image Correlation Robert Schwerz[1], René Metasch[1], Mike Röllig[1], Klaus-Jürgen Wolter[2] *1: Fraunhofer Institute for Ceramic Technologies and Systems, Germany; 2: Technische Universität Dresden, Germany*	Large-Area Femtosecond Laser Ablation of Silicon to Create Membrane with High Performance CMOS-SOI RF Functions Arun Bhaskar[1,2], J. Philippe[1], M. Berthomé[1], E. Okada[1], J.-F. Robillard[1], D. Gloria[2], C. Gaquière[1], E. Dubois[1] *1: University Lille, France; 2: STMicroelectronics, France*	10:45
Risk Assessment Study of Copper Pillar Structure by using Bayesian Networks Kazuaki Ano[1] *1: Dialog Semiconductor, Japan*	The Effect of Surface Optimization on Post-grinding Yield of 200 mm WLP Applications M. Inac[1,2], M. Wietstruck[2], A. Göritz[2], B. Cetindogan[2], C. Baristiran-Kaynak[2], M. Lisker[2], A. Krüger[2], U. Saarow[2], P. Heinrich[2], T. Voss[2], K. Altin[3], M. Kaynak[2,4] *1: TU Berlin; 2: IHP; 3: PVA TePla Analytical Systems GmbH, all Germany; 4: Sabanci Univ. Istanbul, Turkey*	11:15
Investigations on the High Temperature Suitability of Diffusion Soldered Interconnects Christian Schellenberg[1], Jörg Strogies[1], Klaus Wilke[1], Karsten Meier[2] *1: Siemens AG, Germany; 2: Technische Universität Dresden, Germany*	Surface Activated Bonding Method for Low Temperature Bonding Tadatomo Suga[1], Fengwen Mu[1] *1: The University of Tokyo, Japan*	11:40
In-situ X-ray Characterization of IC Package Warpage at Elevated Temperatures Oliver Albrecht[1], Heinz Wohlrabe[1], Karsten Meier[1], Martin Oppermann[1], Thomas Zerna[1] *1: Technische Universität Dresden, Germany*	Bus-based, Miniaturized Multi-sensory Catheter System David Wagner[1], Philipp Bachmann[1], Sven Brinkhues[1], Hanna Petrova[1], Sebastian Freidank[1], Ulrich Schumann[1], Bertram Schmidt[1], Markus Detert[1] *1: Otto-von-Guericke-University Magdeburg, Germany*	12:05

Note about Boardroom 1/2: Presentations will be given in Boardroom 1. As an addition to capacity there will be a real-time video and audio broadcast to Boardroom 2.

Please visit the Industrial Exhibition. More details on page 48.

Room	Palace Restaurant A	
Session	**Interactive Session 3B**	
Chairs	Guangbin Dou Imperial College London, UK Lars Brusberg Corning, USA	
10:45	Using Microfluidic Electroless Interconnection for Low-Temperature, Pressureless Bonding of Micro Bumps C Robert Kao[1], Sean Yang[1], H. T. Hung[1] *1: National Taiwan University*	How my Electronics Should be Oriented: A Thermal Point of View Study to Understand the Impact of Orientation on Internal Air Temperature Tejas Manohar Kesarkar[1], Nitesh Kumar Sardana[1] *1: Robert Bosch Engineering and Business Solutions Pvt. Ltd., India*
	A Novel TSV Interposer Based System-in-Package for RF Applications Rongfeng Luo[1], Yuan Chai[1], Shenglin Ma[1], Xiaoyuzhang[2], Feng Ji[2], Qi Zhong[2] *1: Xiamen University, China; 2: China Aerospace Science and Industry Corporation, China*	Numerical Estimation of Localized Transient Temperature and Strain Fields in Soldering Process Abhiroop Satheesh[1], Midhun Kattisseri[1], Vijeesh Vijayan[1] *1: Robert Bosch Engineering and Business Solutions Pvt. Ltd., India*
	Board Level Reliability Assessment of Wafer Level Chip Scale Packages for SACQ, a Lead-free Solder with a Novel Life Prediction Model Balaji Nandhivaram Muthuraman[1], Baltazar Canete[1] *1: Dialog Semiconductor GmbH, Germany*	Calculation of Local Solder Temperature Profiles in Reflow Ovens Adam Yuile[1], Steffen Wiese[1] *1: Saarland University, Germany*
	High Signal Integrity Transmission Line Using Microchip Capacitors and its Design Methodology Shumpei Matsuoka[1], Moritoshi Yasunaga[1] *1: University of Tsukuba, Japan*	Modelling Approaches of Vapour Phase Reflow Soldering Attila Géczy[1], István Bozsóki[1], Balázs Illés[1] *1: Budapest University of Technology and Economics, Hungary*

12:30	**Lunch break** Lunch buffet will be served in the exhibition area located in **Foyer** and in **Bellevue 1** as well as in **Palace Restaurant A**.

Palace Restaurant A

INTS3B

Interactive Session is based on a poster exhibition, where audience and speaker can discuss the presented results during the whole session. Posters are shown during both session parts A and B. In addition speakers give a short introduction to their posters topic scheduled as follows.

Using Microfluidic Electroless Interconnection for Low-Temperature, Pressureless Bonding of Micro Bumps	10:45
A Novel TSV Interposer Based System-in-Package for RF Applications	10:53
Board Level Reliability Assessment of Wafer Level Chip Scale Packages for SACQ, a Lead-free Solder with a Novel Life Prediction Model	11:01
High Signal Integrity Transmission Line Using Microchip Capacitors and its Design Methodology	11:09
How my Electronics Should be Oriented: A Thermal Point of View Study to Understand the Impact of Orientation on Intern. Air Temp.	11:17
Calculation of Local Solder Temperature Profiles in Reflow Ovens	11:25
Modelling Approaches of Vapour Phase Reflow Soldering	11:33
Interaction Effects Between the Preferred Growth of β-Sn Grains and Thermo-mechanical Response in Microbump Interconnects …	11:41

Interaction Effects Between the Preferred Growth of β-Sn Grains and Thermo-mechanical Response in Microbump Interconnects under Thermal Cycling

Shui-Bao Liang[1,2], Xin-Ping Zhang[1], Cheng Wei[1], Chang-Bo Ke[1], Changqing Liu[2]

1: South China University of Technology, China; 2: Loughborough University, UK

Please visit the Industrial Exhibition. More details on page 48.

Room	Bellevue 2	Bellevue 3
Session	**ASS3**	**MAT5**
Chairs	Ryszard Kisiel Warsaw University of Technology, Poland David Whalley University of Loughborough, UK	Lars Rebenklau Fraunhofer IKTS, Germany Sven Rzepka Fraunhofer ENAS, Germany
13:30	Wire Bonding of Surface Acoustic Wave (SAW) Sensors for High Temperature Applications Daniel Ernst[1], Erik Brachmann[2], Siegfried Menzel[2], Karlheinz Bock[1] *1: Technische Universität Dresden, Germany; 2: Leibniz Institute for Solid State and Materials Research Dresden, Germany*	Phase Determination in SLID Bonding Knut E. Aasmundtveit[1], Hui Jiang[2], Torleif A. Tollefsen[3], Thi-Thuy Luu[4], Hoang-Vu Nguyen[1] *1: University of South-Eastern Norway; 2: Oxford Instruments NanoAnalysis, UK; 3: TEGma AS, Norway; 4: Zimmer and Peacock AS, Norway*
14:00	Cu Pillar as Interconnect for 10µm Pitch and Below: Fabrication Issues and Assembly Results Marion Volpert[1], Divya Taneja[1], Alain Gueugnot[1], David Henry[1], Tarik Chaira[1], Fiqiri Hodaj[2] *1: CEA, LETI, France; 2: Grenoble INP, France*	Ag Sintering – An Alternative Large Area Joining Technology Constanze Weber[1], Matthias Hutter[1] *1: Fraunhofer IZM, Germany*
14:25	Investigation of a Low-Cost Sequential Plating Based Process for Pb-free Bumping Abderrahim El Amrani[1], Etienne Paradis[1], David Danovitch[1], Dominique Drouin[1] *1 Université de Sherbrooke, Canada*	Design of a Novel Epoxy Mold Compound with Locally Varying Thermal Properties for an Improved Thermal Management of SMD Packages M. Morak[1], M. Gschwandl[1], P. F. Fuchs[1], P. Marx[1], F. Wiesbrock[1], T. Antretter[2], M. Pfost[3] *1: Polymer Competence Center Leoben GmbH; 2: Montanuniversitaet Leoben, Austria; 3: Dortmund Techn. Univ., Germany*
14:50	New Flip-chip Bonder Dedicated to Direct Bonding for Production Environment Pascal Metzger[1], Nicolas Raynaud[1], Amandine Jouve[2], Nicolas Bresson[2], Loïc Sanchez[2], Frank Fournel[2], Severine Cheramy[2] *1: SET Corporation, France; 2: CEA, LETI, France*	Heat Transfer Efficiency Measurements with Using Thermography for Low-Temperature and Low-Pressure Sintered Silver Joints Krzysztof Stojek[1], Jan Felba[1], Tomasz Falat[1], Damian Nowak[1], Andrzej Moscicki[2], Agata Surmiak[1] *1: Wroclaw University of Science and Technology, Poland; 2: Amepox Microelectronics LTD, Poland*
15:15	**Coffee break** Coffee and snacks will be served in the exhibition area located in **Foyer** and in **Bellevue 1** as well as in **Palace Restaurant A**.	

Palace Restaurant B	Boardroom 1/2	Room
RE4	**ES2**	Session
Peter Frühauf Siemens, Germany Steffen Wiese University of Saarland, Germany	Martin Oppermann TU Dresden, Germany Martin Schneider-Ramelow Fraunhofer IZM, Germany	Chairs
An Advanced Method for Cyclic Delamination Studies of Thin Film Multilayers in Electronics Thomas Walter[1], Golta Khatibi[1] *1: TU Vienna, Austria*	Microfluidic Interposer for High Performance Fluidic Chip Cooling W. Steller[1], F. Windrich[1], D. Bremner[2], S. Robertson[2], R. Mroßko[3], J. Keller[3], T. Brunschwiler[4], G. Schlottig[5], H. Oppermann[6], M. J. Wolf[1], K.-D. Lang[7] *1: Fraunhofer IZM - ASSID, Germany; 2: Optocap LTD., UK; 3: AMIC GmbH, Germany; 4: IBM Research, Switzerland; 5: ABB Ltd., Switzerland; 6: Fraunhofer IZM, Germany; 7: TU Berlin, Germany*	13:30
Status and Review of Advanced Mixed-Mode Bending Fracture Test (AMB) Marcus Schulz[1], Jürgen Keller[1], Clemence Vernier[2], Marc Dressler[2], Bernhard Wunderle[3] *1: AMIC GmbH, Germany; 2: Robert Bosch GmbH, Germany; 3: Chemnitz University of Technology, Germany*	Organic packaging with integrated NFC for harsh environments Sven Johannsen[1], Eckardt Bihler[1], Marc Hauer[1] *1: DYCONEX AG, Switzerland*	14:00
Investigation on the Lifetime of Copper Wire Bonds in Electronic Packages under Thermal and Mechanical Cyclic Loading Ali Mazloum-Nejadari[1], Martin Lederer[2], Golta Khatibi[2], Bernhard Czerny[2], Laurens Weiss[1], Johann Nicolics[2] *1: Infineon AG, Germany; 2: TU Vienna, Austria*	Will 3D-semiadditive Packaging with High Conductive Redistribution Layer and Process Temperatures Below 100°C Enable New Electronic Applications? Tobias Tiedje[1], Sebastian Lüngen[1], Krzysztof Nieweglowski[1], Karlheinz Bock[1] *1: Technische Universität Dresden, Germany*	14:25
Assessment of Wire Bond Reliability by Static Shear, Active Power Cycling and Accelerated Mechanical Fatigue Testing Bernhard Czerny[1] *1: TU Vienna, Austria*	Future Interconnect Materials and System Integration Strategies for Data-Intensive Applications P. Apte[1], T. Salmon[1], R. Rice[2], M. Gerber[2], R. Beica[3], J. Calvert[3], D. Hemker[4], Y. Dordi[4], M. Ranjan[4], S. Ramalingam[5], J. Gandhi[5], A. Kaviani[5], S. Mitra[6], P. Wong[6], V. Lee[6], M. El-Sabry[6] *1: SEMI; 2: ASE Inc.; 3: Dow Chemical; 4: Lam Research; 5: Xilinx; 6: Stanford University, all USA*	14:50

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