

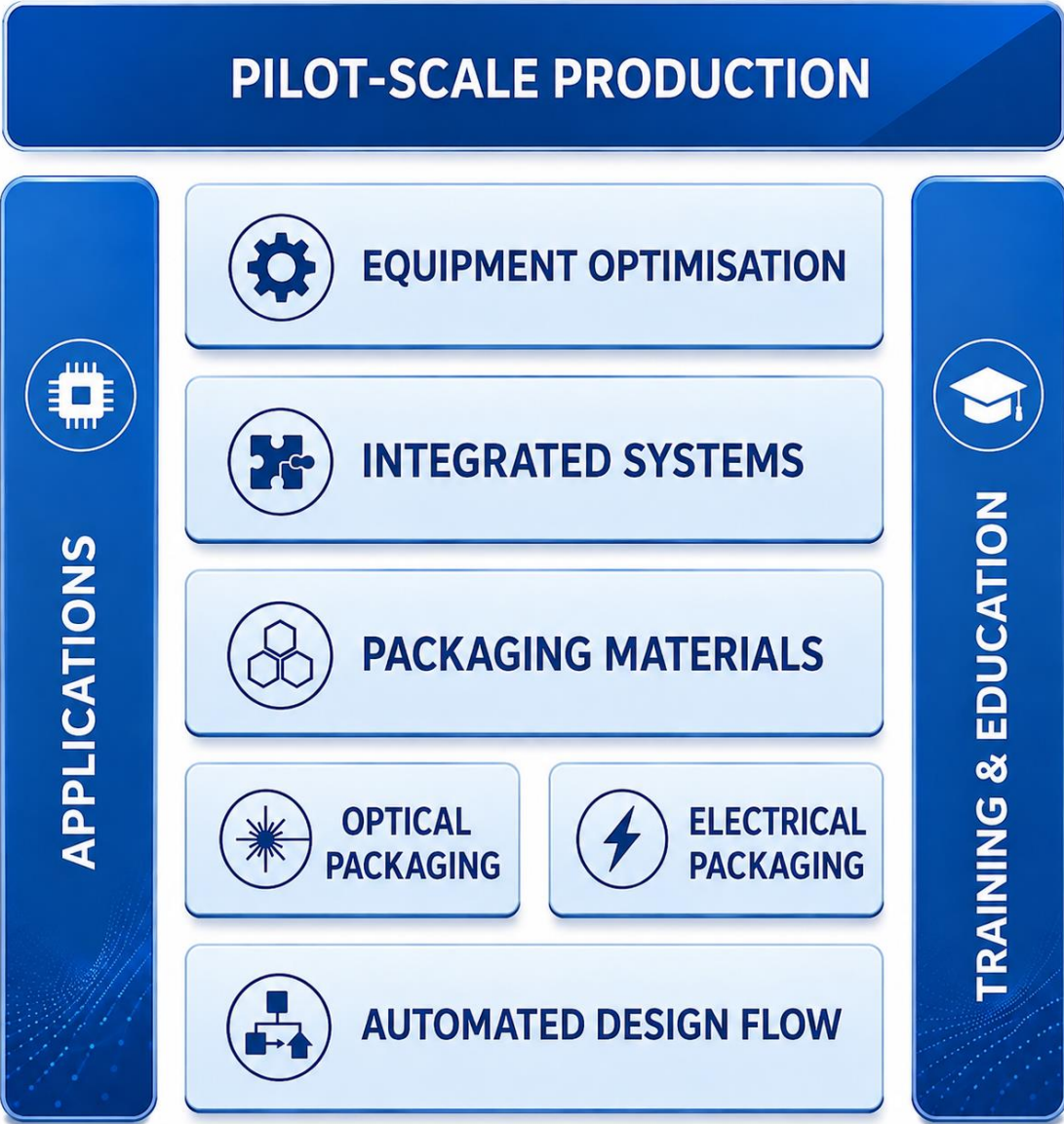
Integrated Photonic Packaging

Materials, Processes, Equipment, and Scaling to Production

Course Instructor

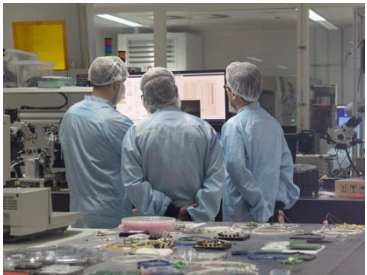
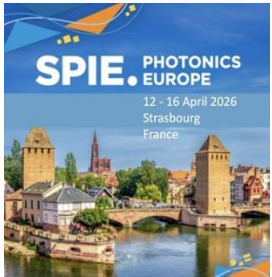
Prof. Peter O'Brien, Tyndall National Institute, Ireland

Advanced Packaging @ Tyndall Institute

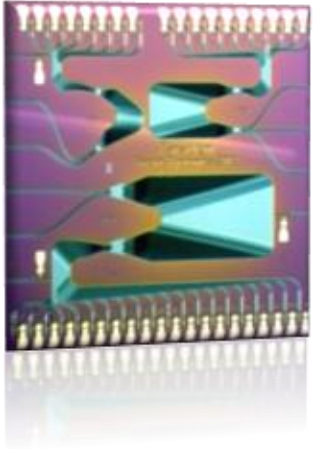


Advanced Packaging @ Tyndall Institute

Fundamental Research to
Ecosystem Building



Photonic Packaging (the technologies)

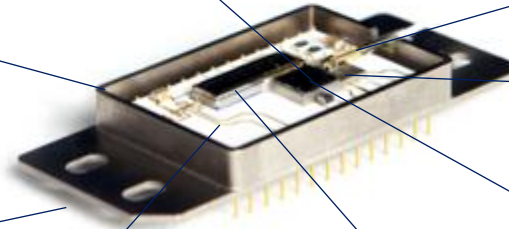


***Photonic Integrated Circuit
(PIC)***



Fibre Optics

Mechanical Package



Micro Optics

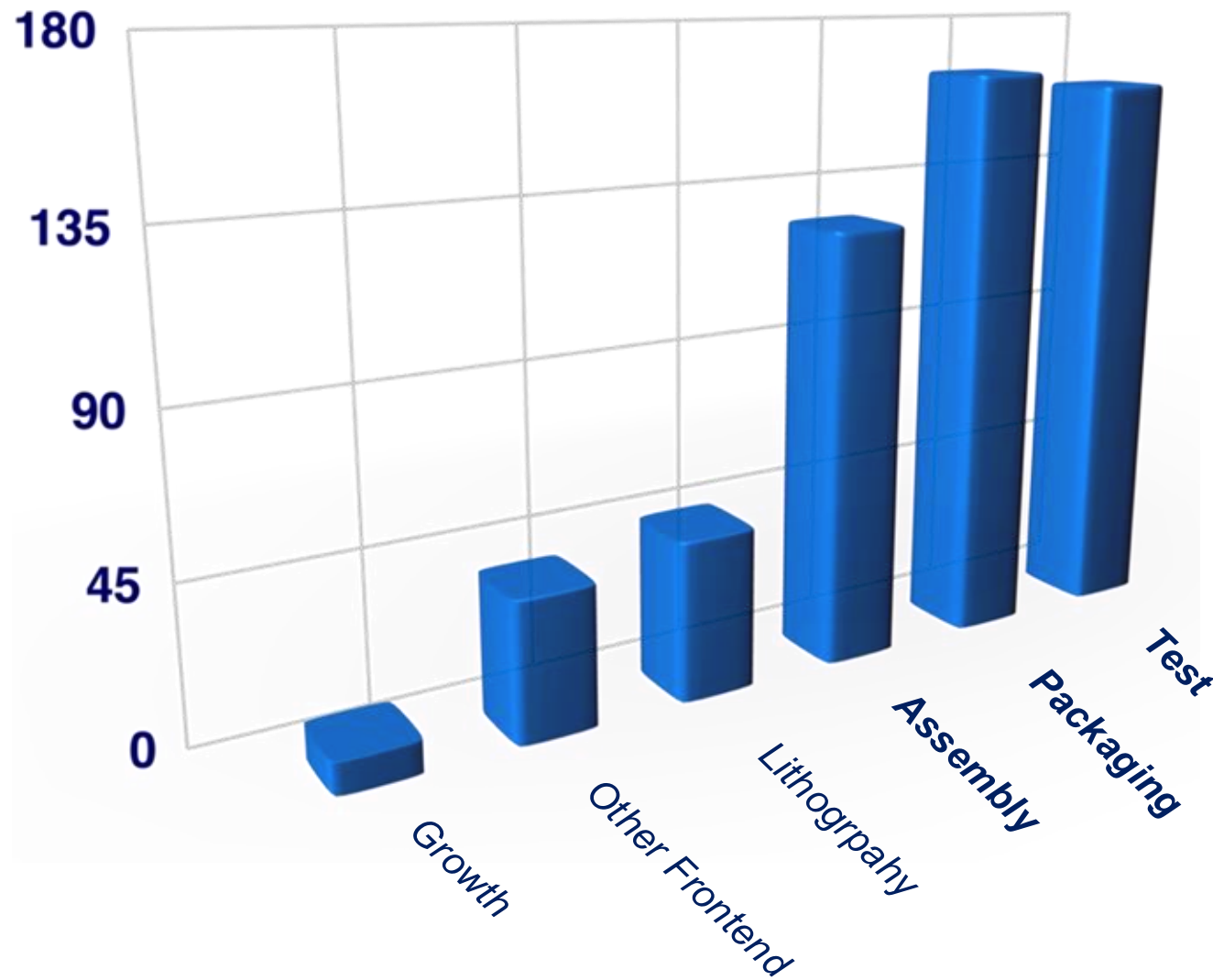
Thermal Management

Source Integration

Electrical Packaging

Electronic Integration

The Cost of Photonic Packaging



Process Step

Percentage Cost

Assembly & Packaging

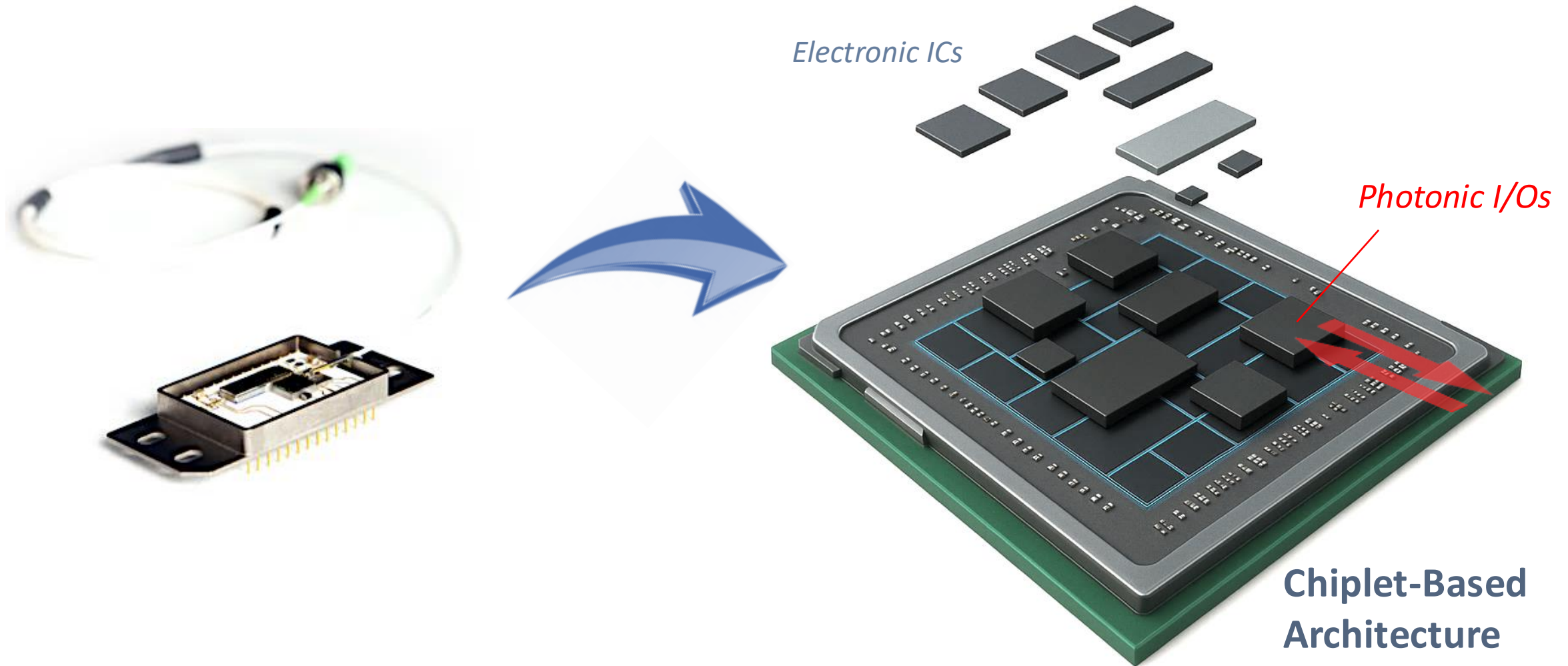
> 50%

Assembly, Packaging
& Test

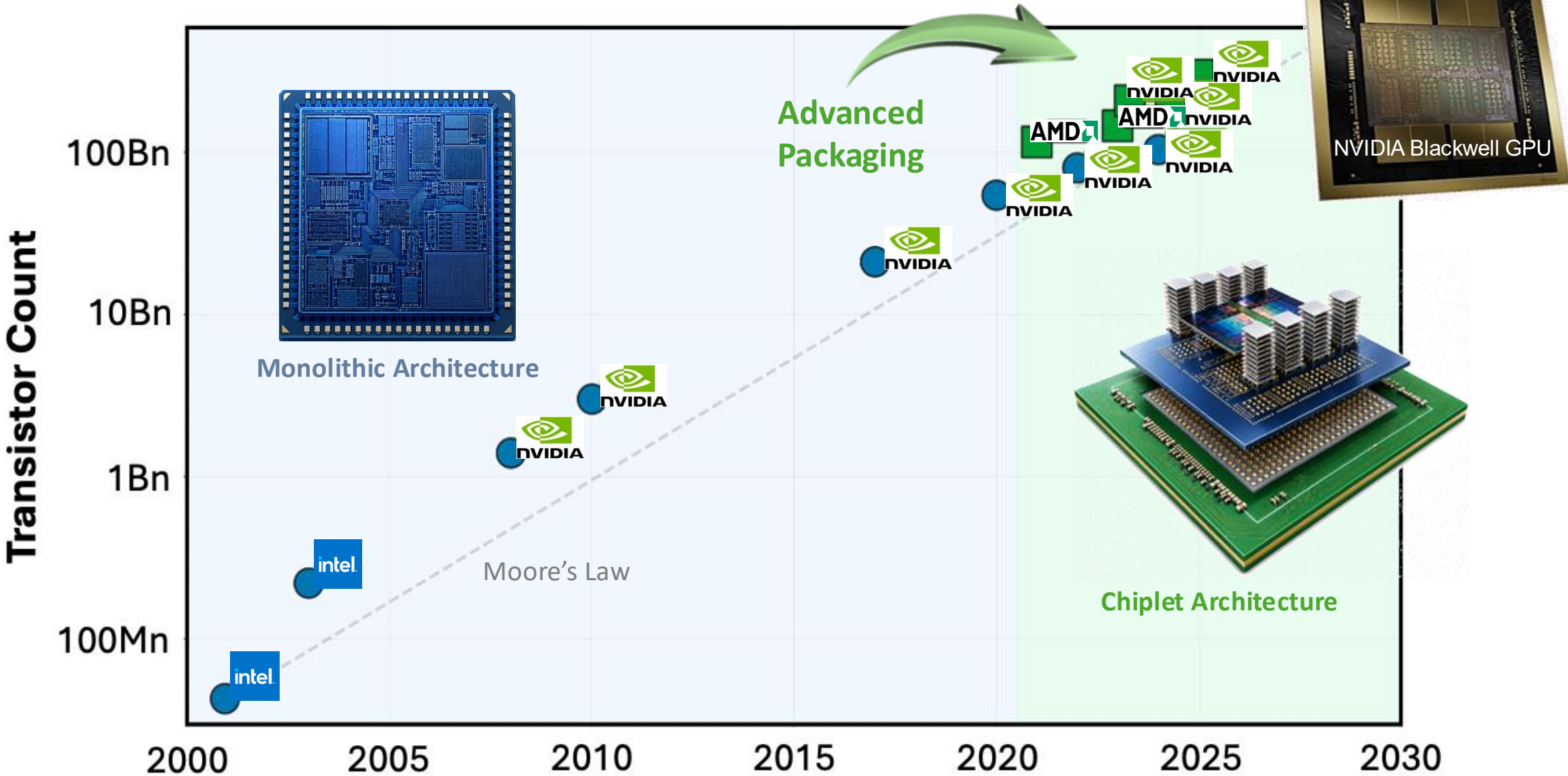
> 80%

Process-Based Cost Modeling of Photonics Manufacture: The Cost Competitiveness of Monolithic Integration of a 1550-nm DFB Laser and an Electroabsorptive Modulator on an InP Platform, IEEE Journal of Lightwave Technology, Vol. 24, No. 8, 2006.

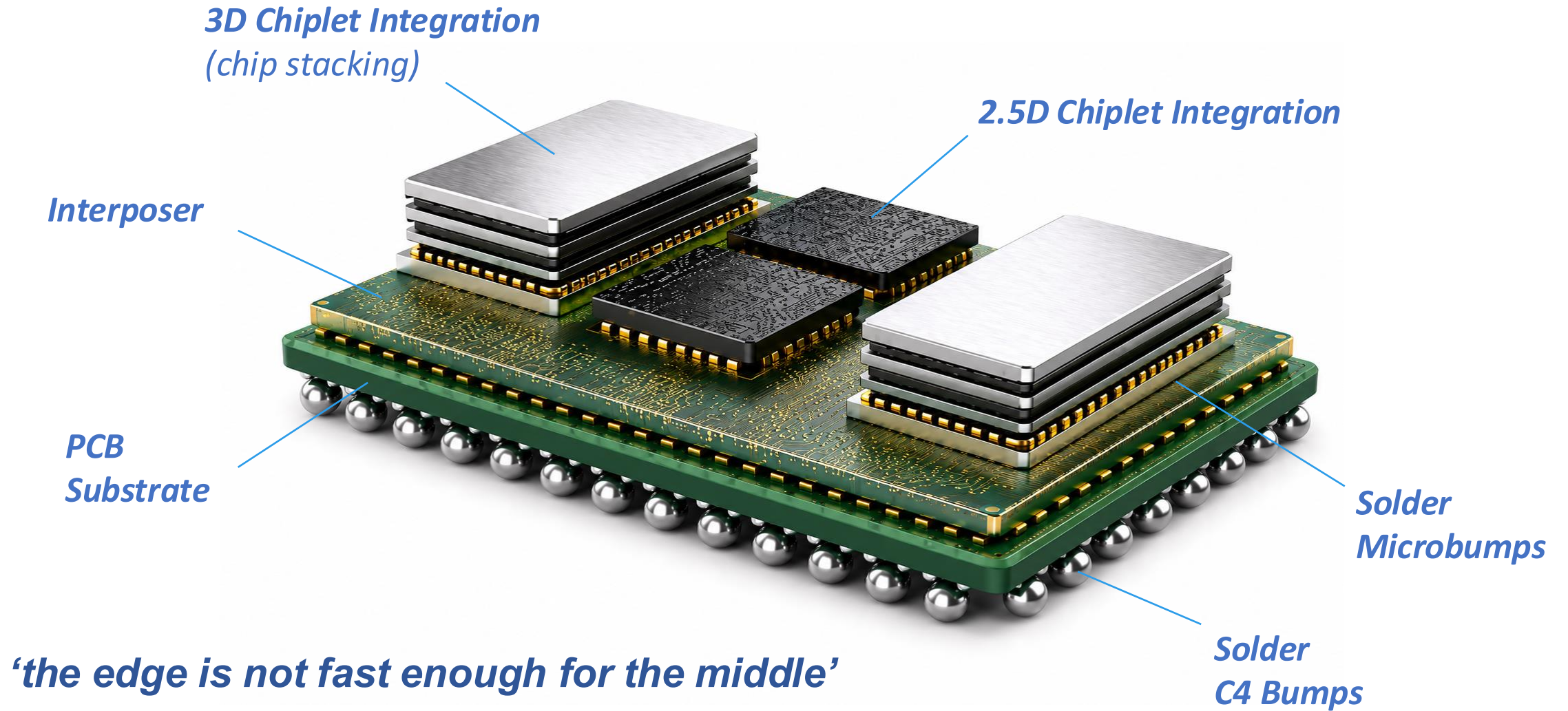
Increasing Photonics Complexity (co-packaging with electronics)



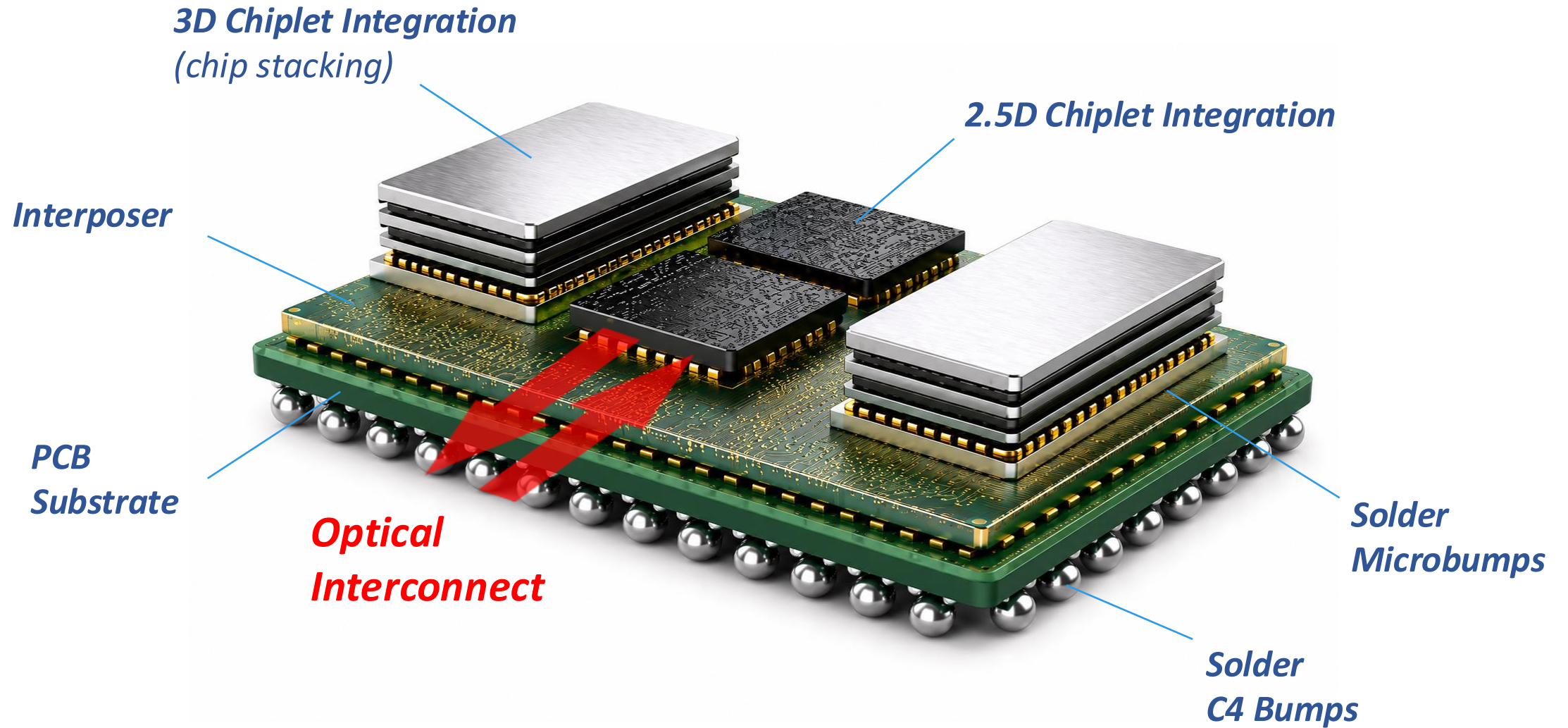
Advanced Packaging, Chiplets & Interposers



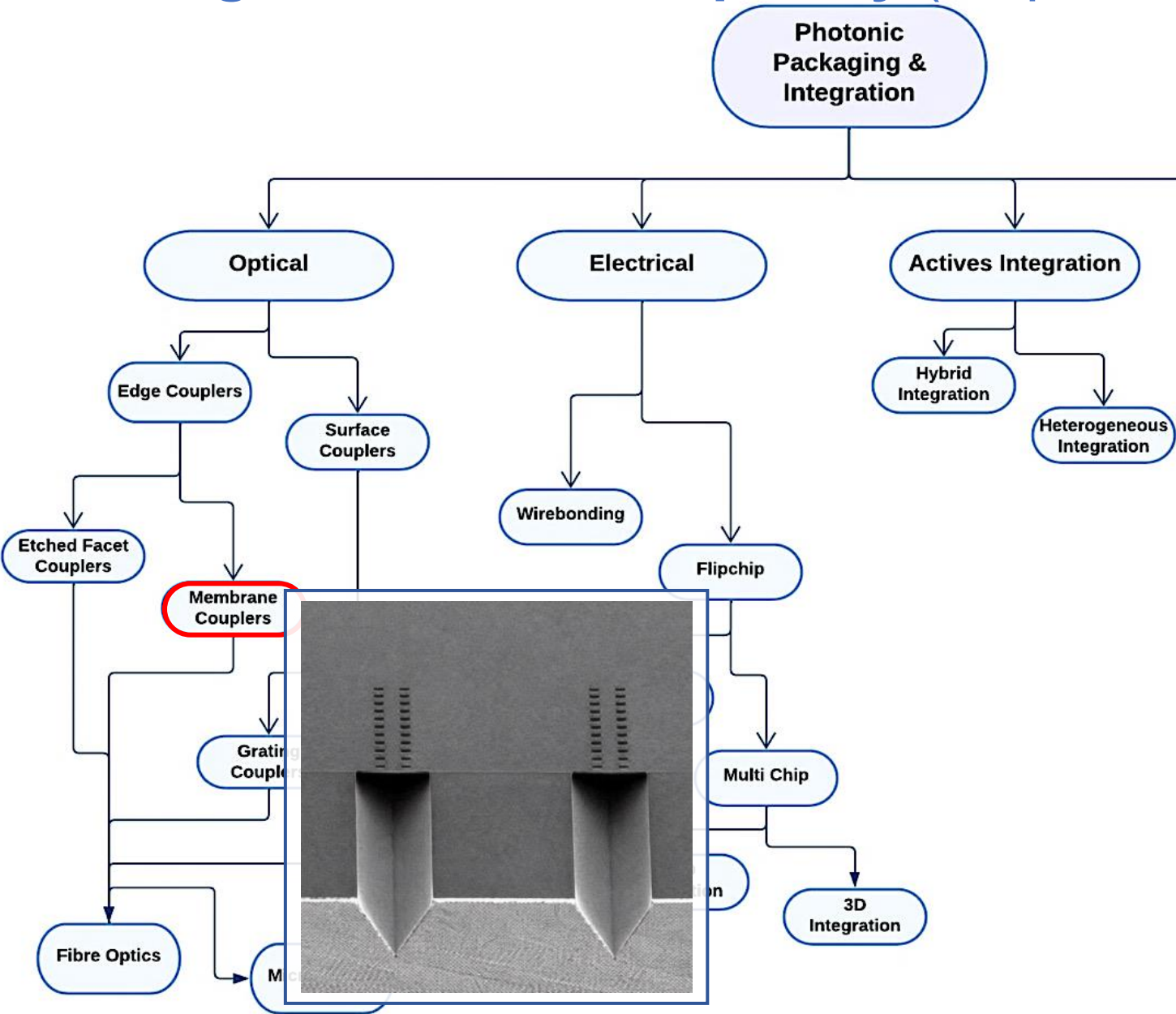
Advanced Packaging, Chiplets & Interposers



Advanced Packaging, Chiplets & Interposers

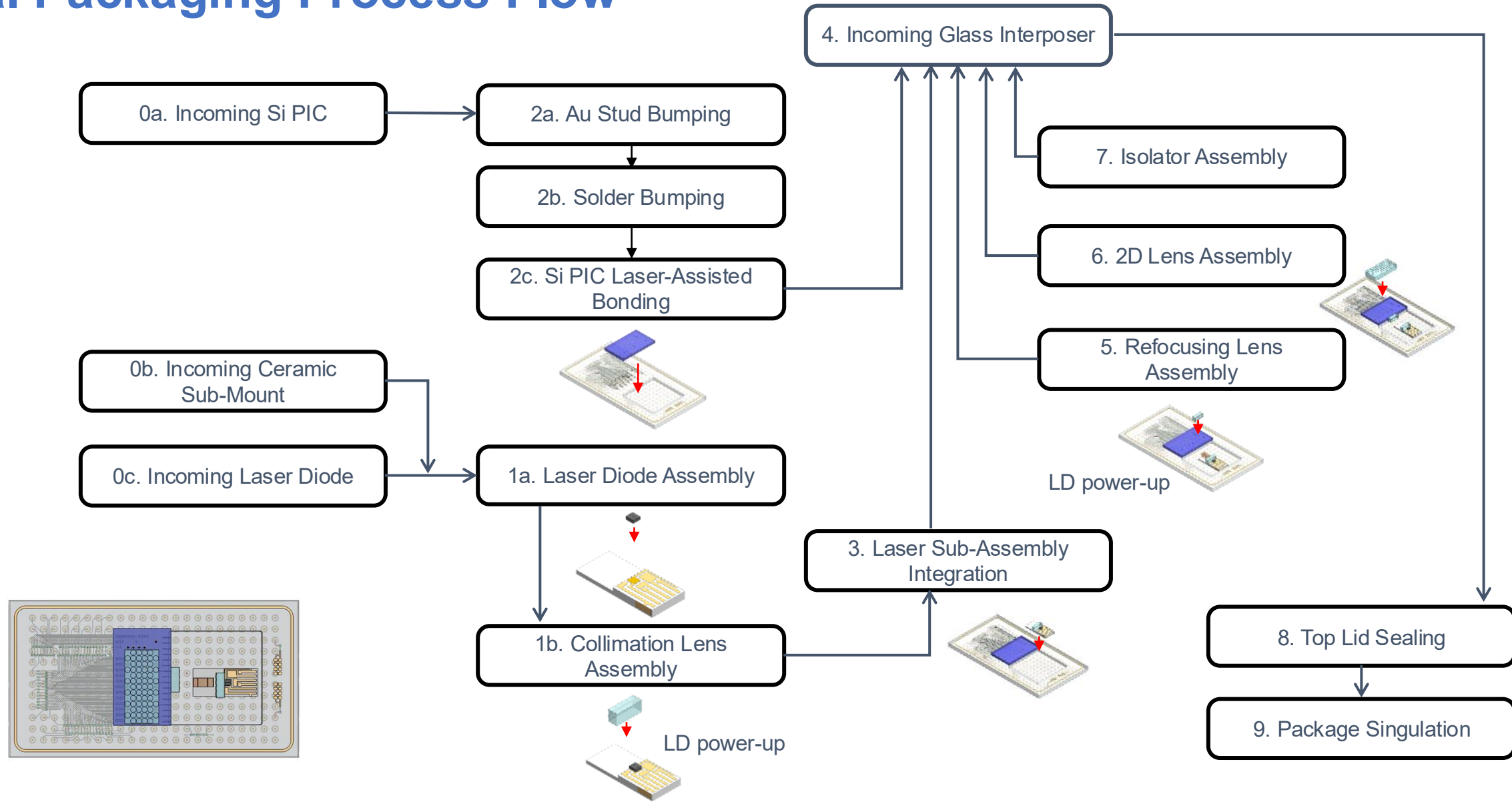


Increasing Photonics Complexity (co-packaging with electronics)



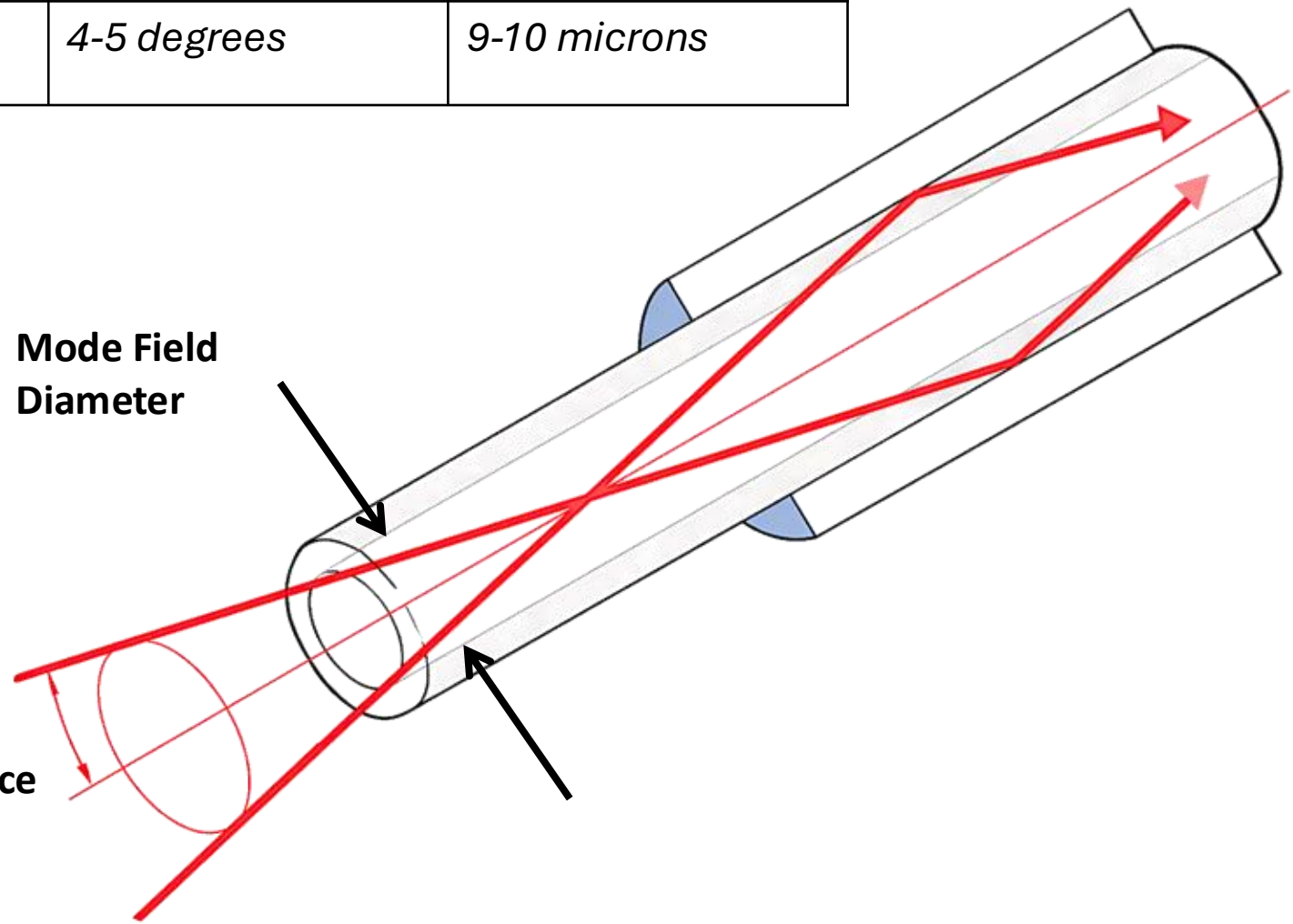
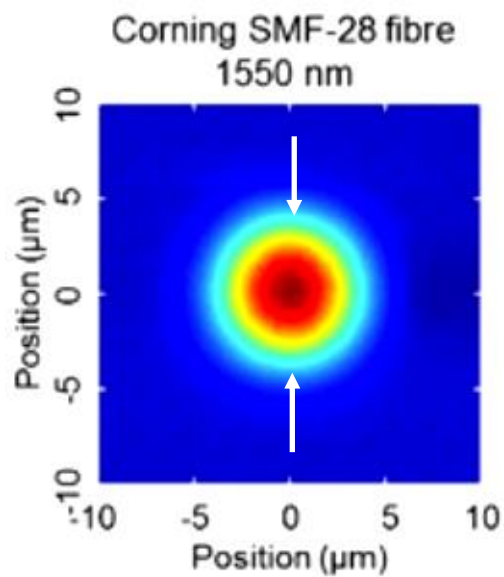
Integrated silicon photonic MEMS
Nature Microsystems & Nanoengineering
Vol. 9, March 2023.

Typical Packaging Process Flow

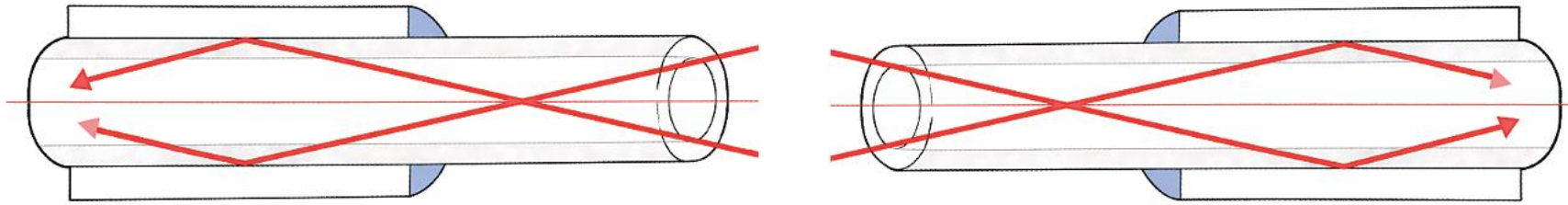


Photonic Packaging (optical)

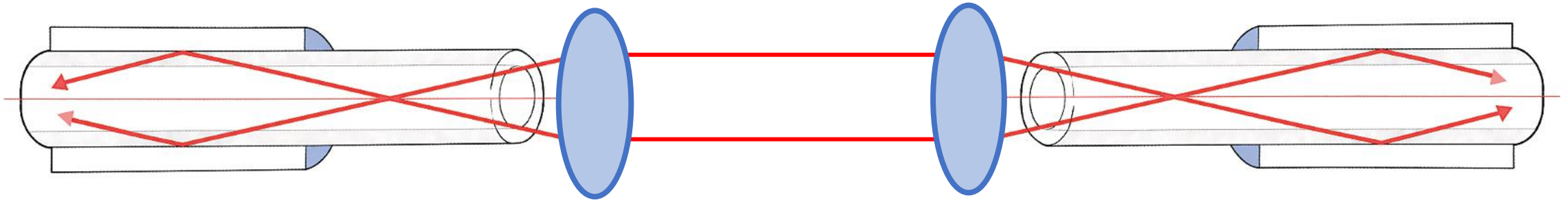
Fiber Type	Numerical Aperture	Beam Divergence (half angle)	Mode Field Diameter
Single Mode Fibre	0.10-0.14	4-5 degrees	9-10 microns



Photonic Packaging (optical)



Optical Fibre Splicing

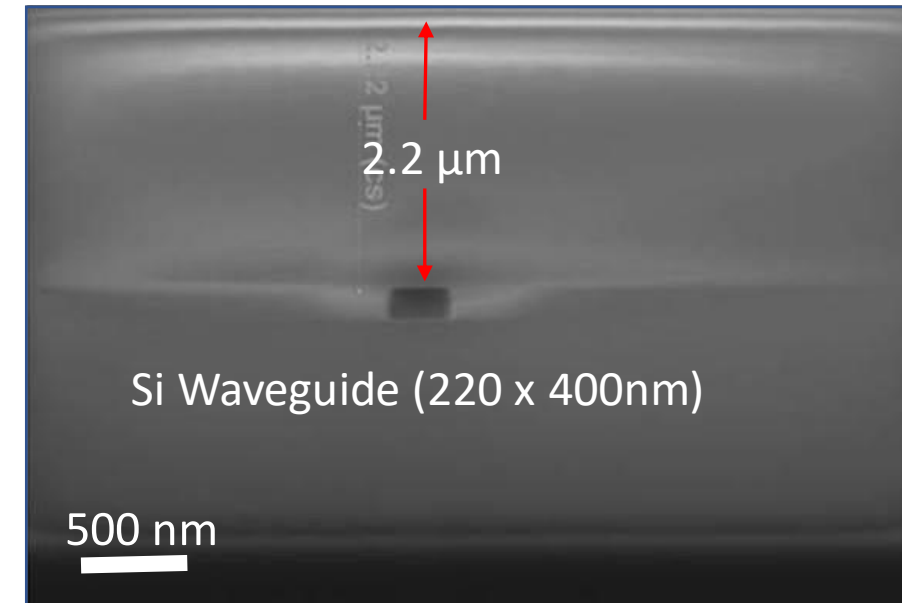


Microlens Coupling

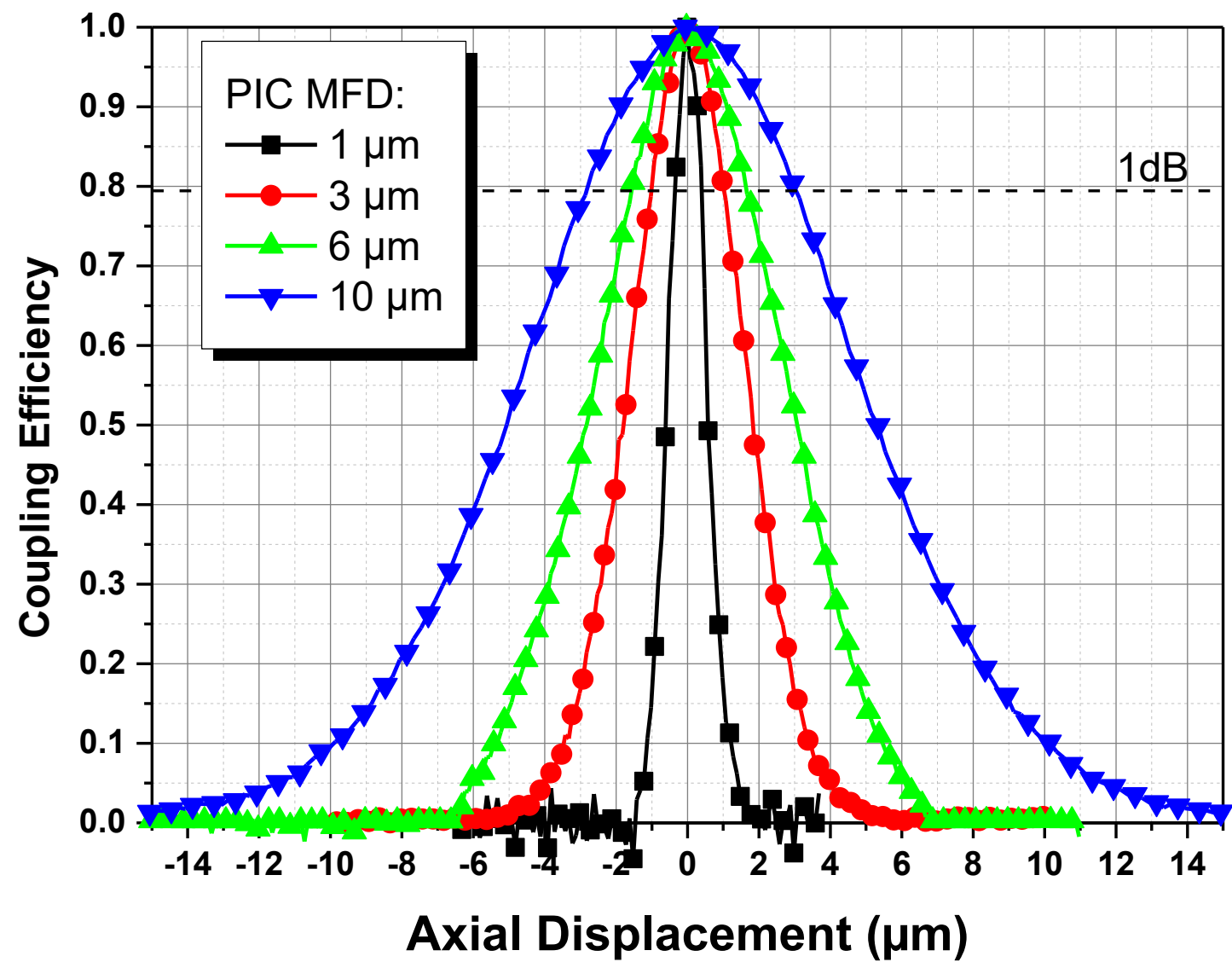
Photonic Packaging (optical)

Single Mode Fibre	0.10-0.14	9-10 microns
Silicon Edge Nano Waveguide	> 0.3-0.6	0.2 microns
Silicon Top Grating Coupler	0.08-0.15	Matched to optical fibre
Silicon Edge Mode Adaptor	0.10-0.15	Matched to optical fibre

Efficient optical coupling between optical fibre and PIC waveguide requires NAs to be matched (directly or indirectly)

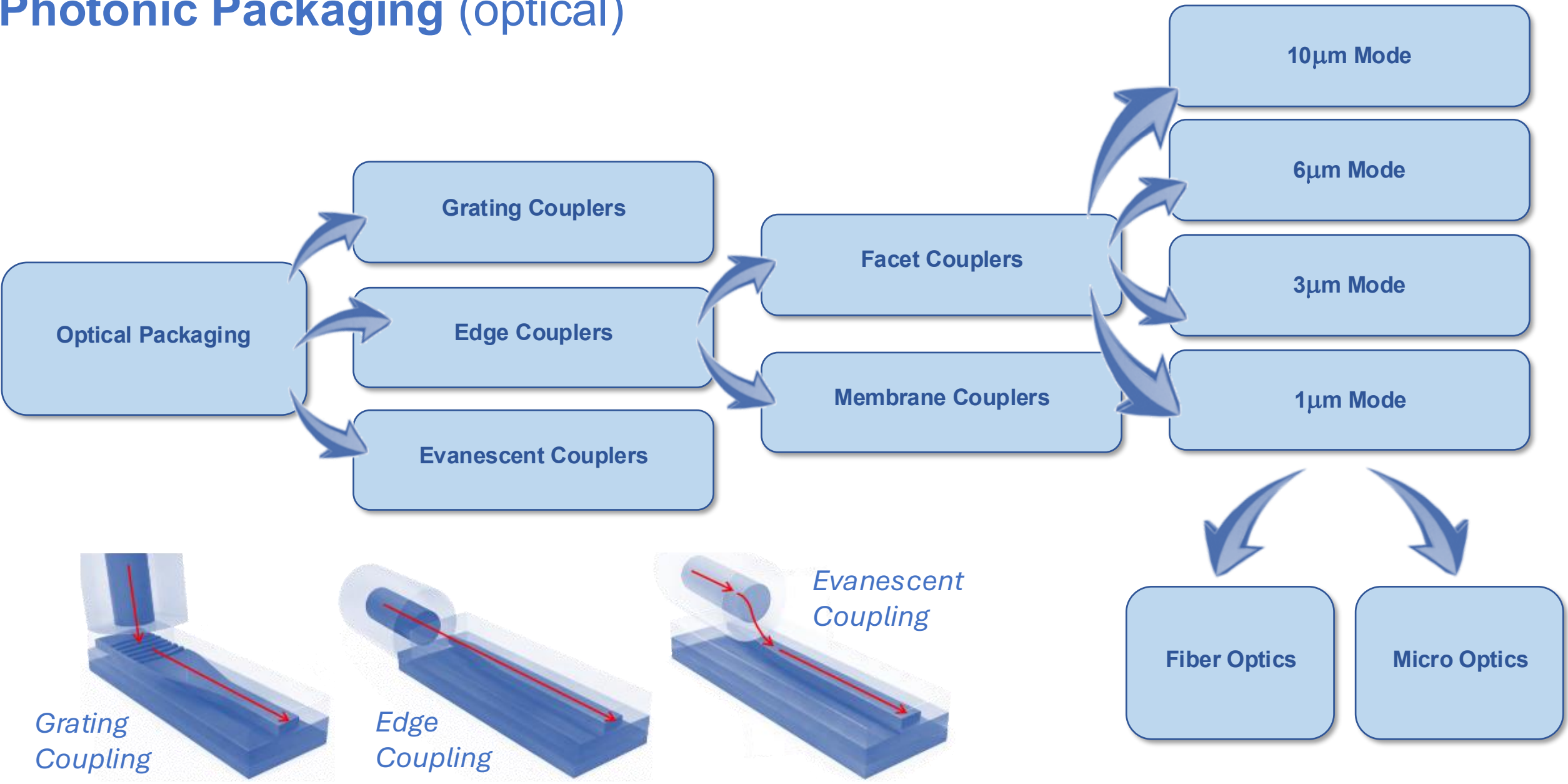


Optical Coupling Requirements (mode sizes)

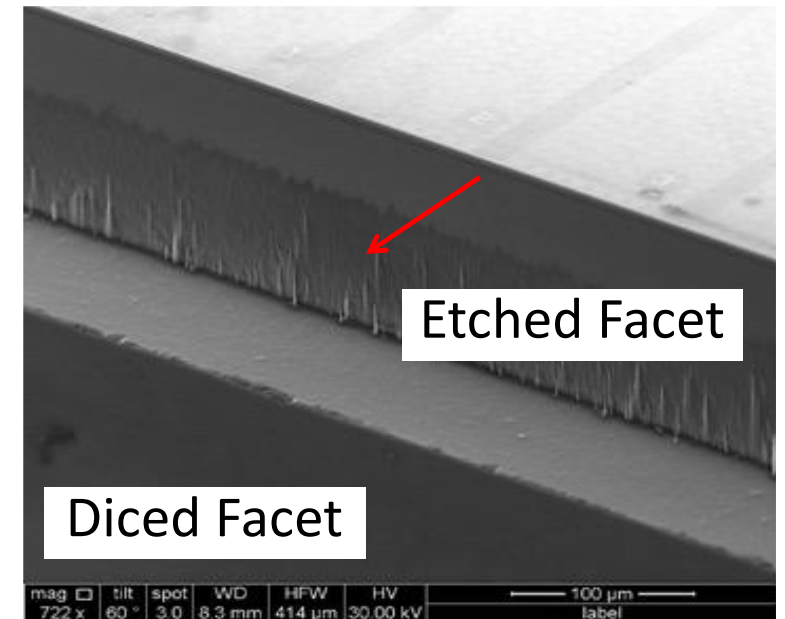
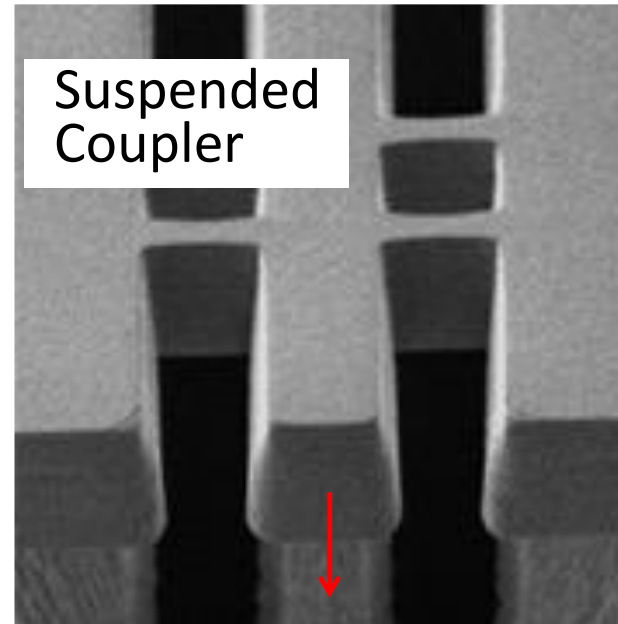
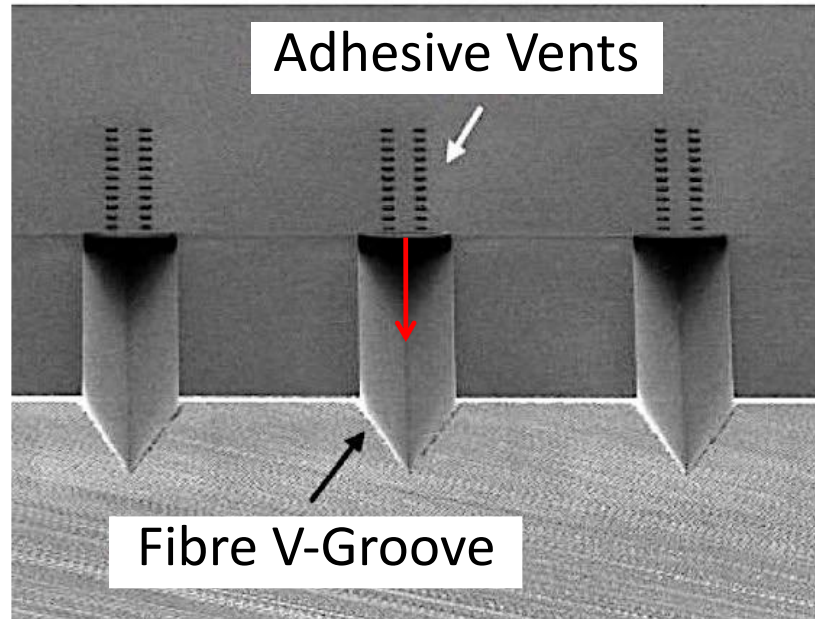


Nominal PIC MFD [μm]	1dB Alignment Tolerance [μm]
1	0.4
3	1.0
6	1.7
10	3.0

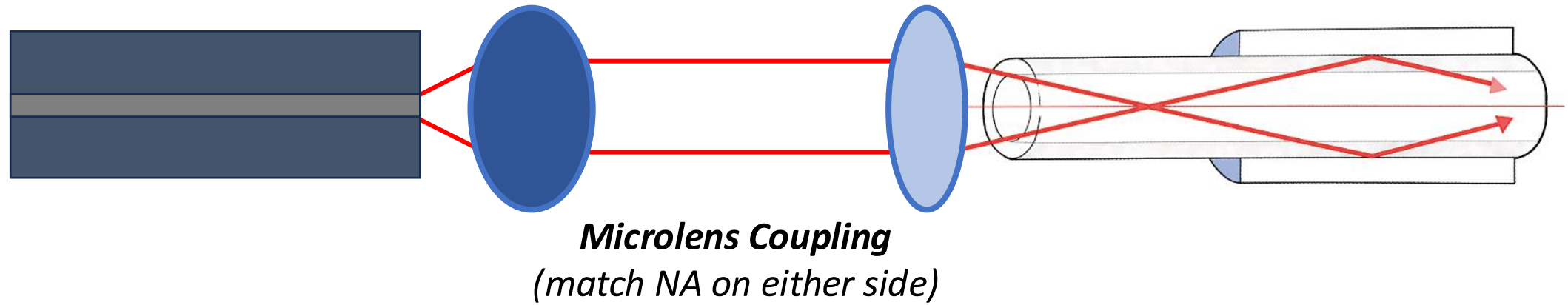
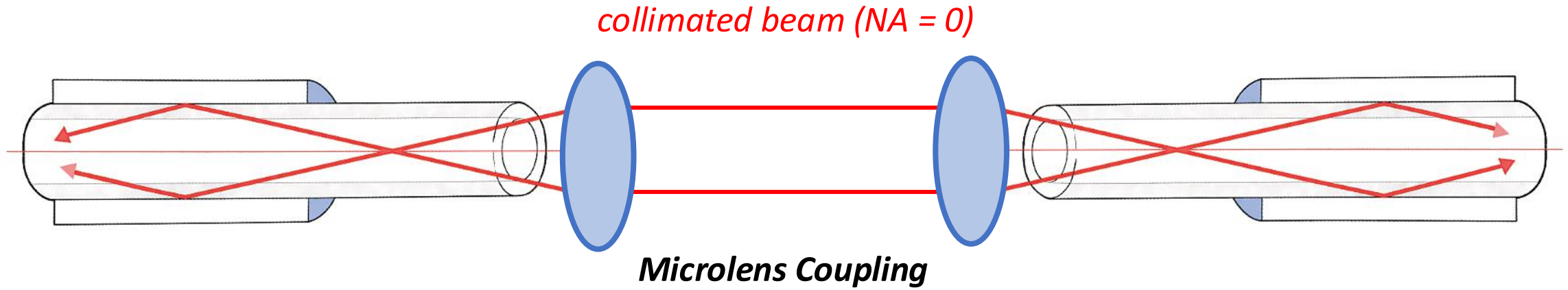
Photonic Packaging (optical)



Photonic Packaging (optical)

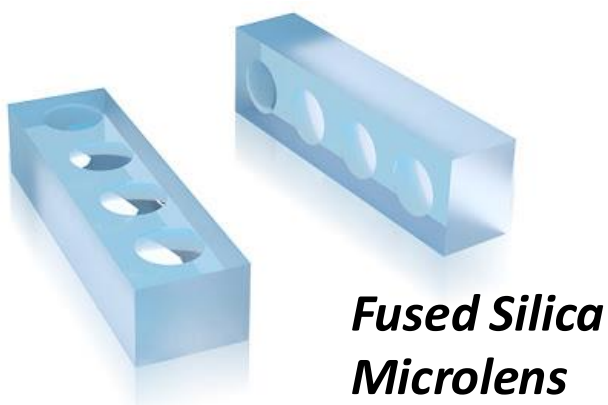
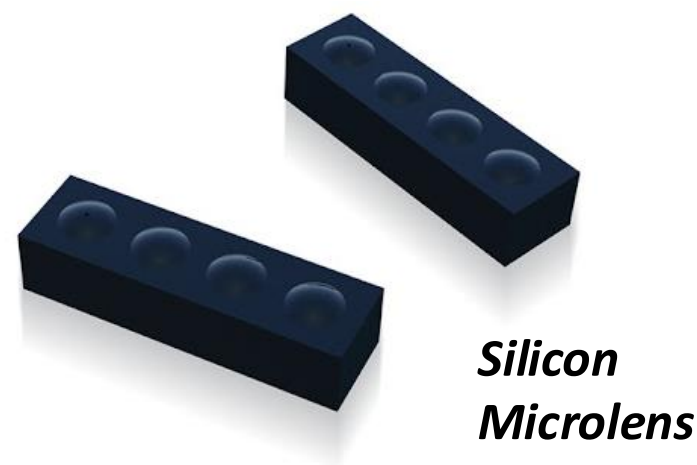


Photonic Packaging (optical)

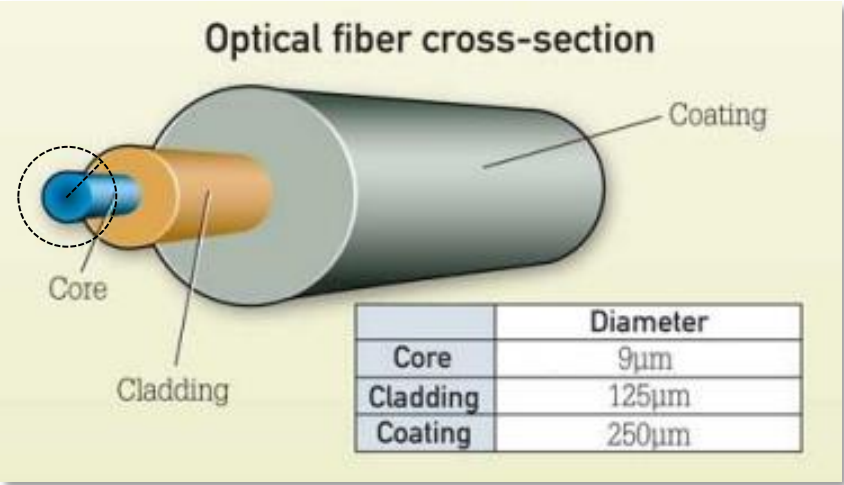


Photonic Packaging (optical)

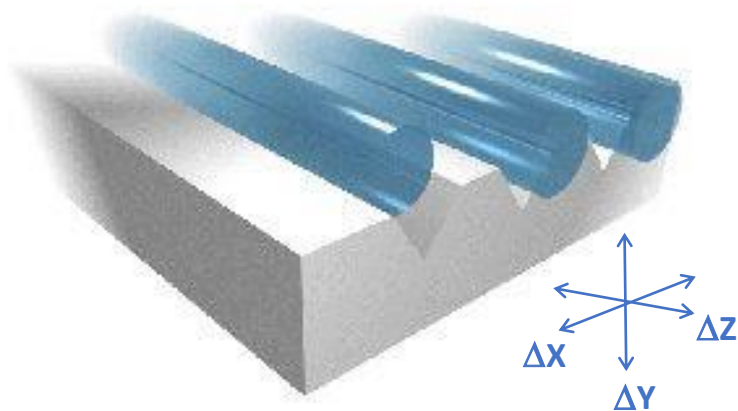
Optical Component	Numerical Aperture (NA)	Refractive Index (1550 nm)	Notes / Typical Use
Single-mode optical fiber	0.10 – 0.14	Core ~1.45	Telecom SMF; defines acceptance cone for coupling
Fused Silica Microlens	0.10 – 0.30	≈ 1.44	Moderate NA; commonly used for fiber and free-space coupling
Silicon Microlens	0.30 – 0.70 (or higher)	≈ 3.45	High-index lens; enables fast focusing for silicon photonics



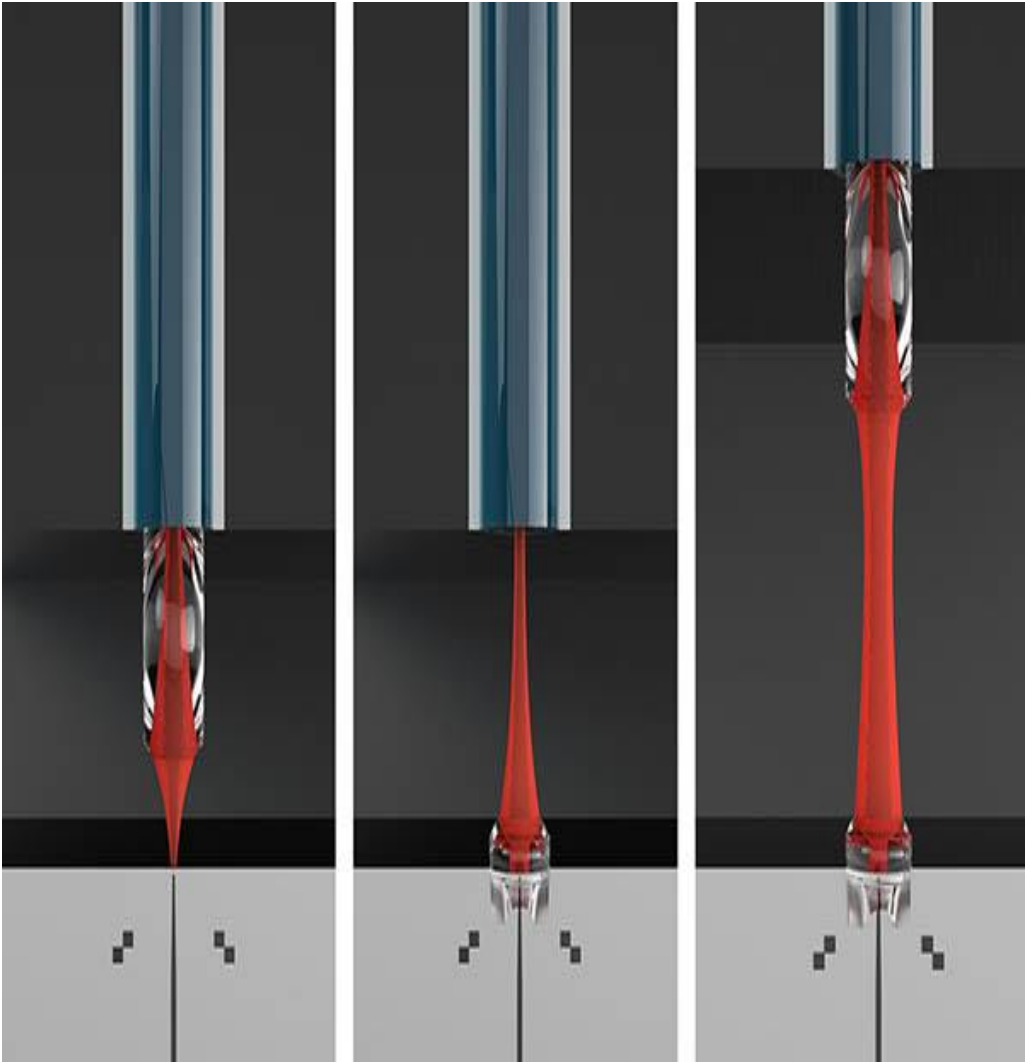
Fiber Optic Packaging (edge coupled)



Fibre Core Concentricity

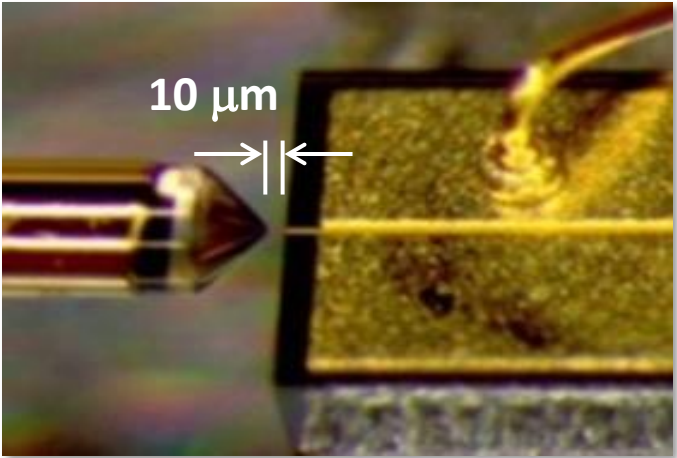
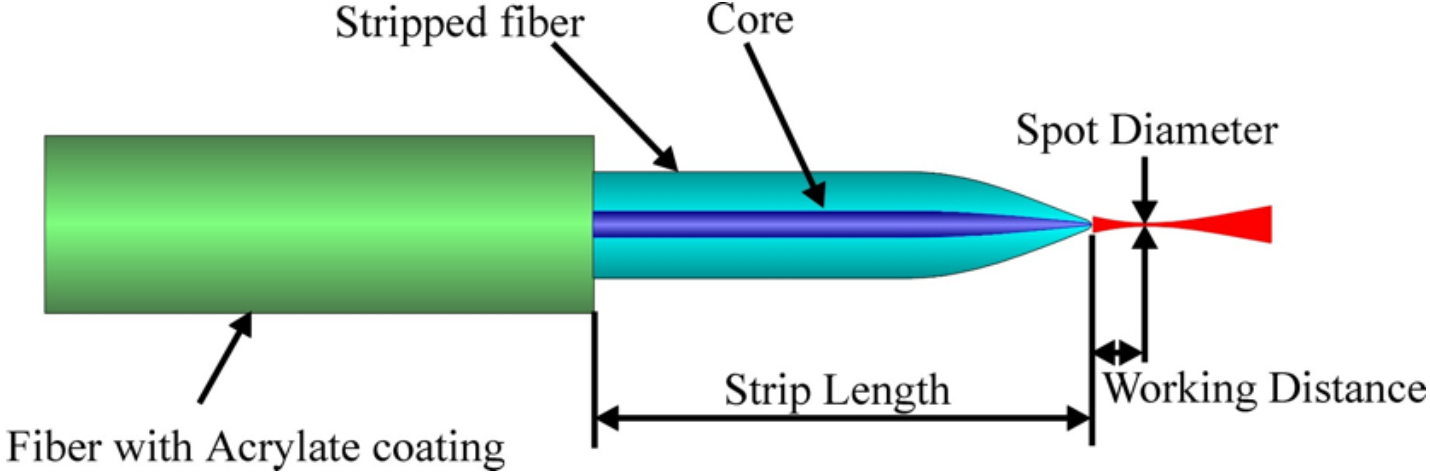


Fibre Alignment in V-Grooves



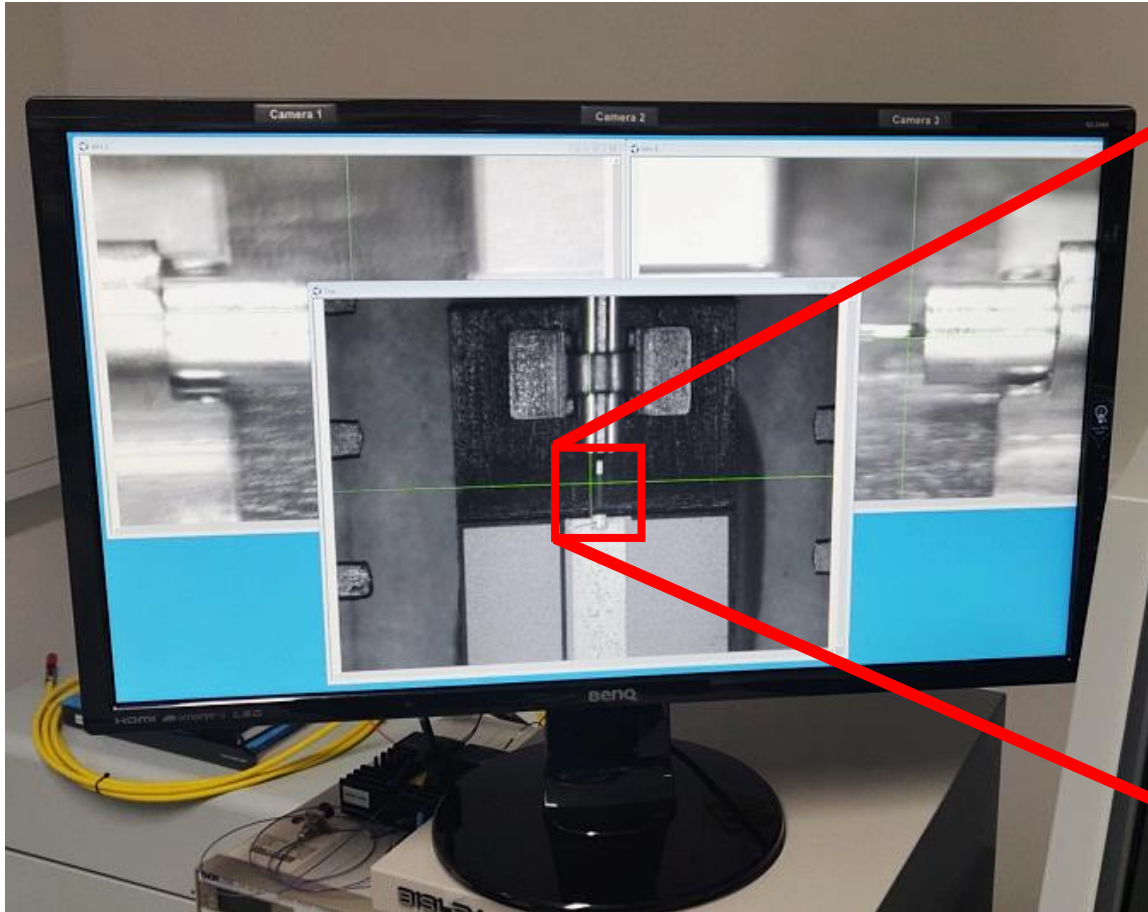
Optical Fibre Coupling to PICs

Fiber Optic Packaging (edge coupled)



Spot Size (μm) @ 1550nm	Working Distance (μm)
1.7 +/- 0.3	4 +/- 1.0
2.0 +/- 0.3	6 +/- 1.0
3.0 +/- 0.3	10 +/- 1.5
4.0 +/- 0.3	13 +/- 1.5
5.0 +/- 0.3	16 +/- 1.5
6.0 +/- 0.3	18 +/- 2
9.0 +/- 0.3	25 +/- 2.0

Fiber Optic Packaging (edge coupled)

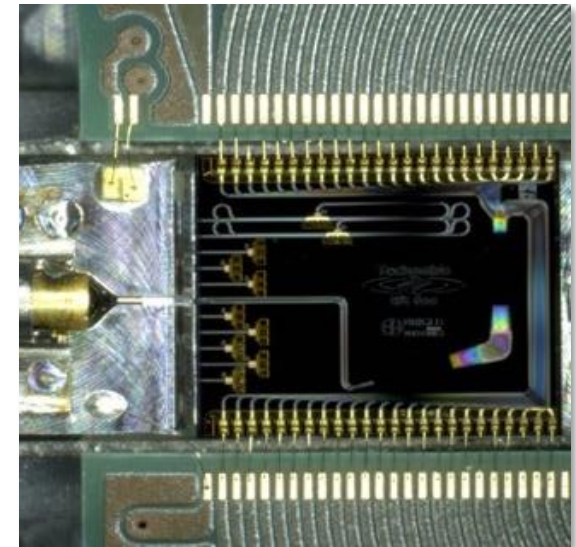
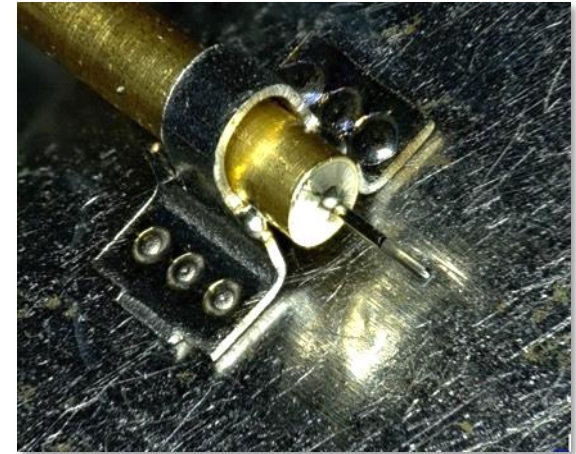
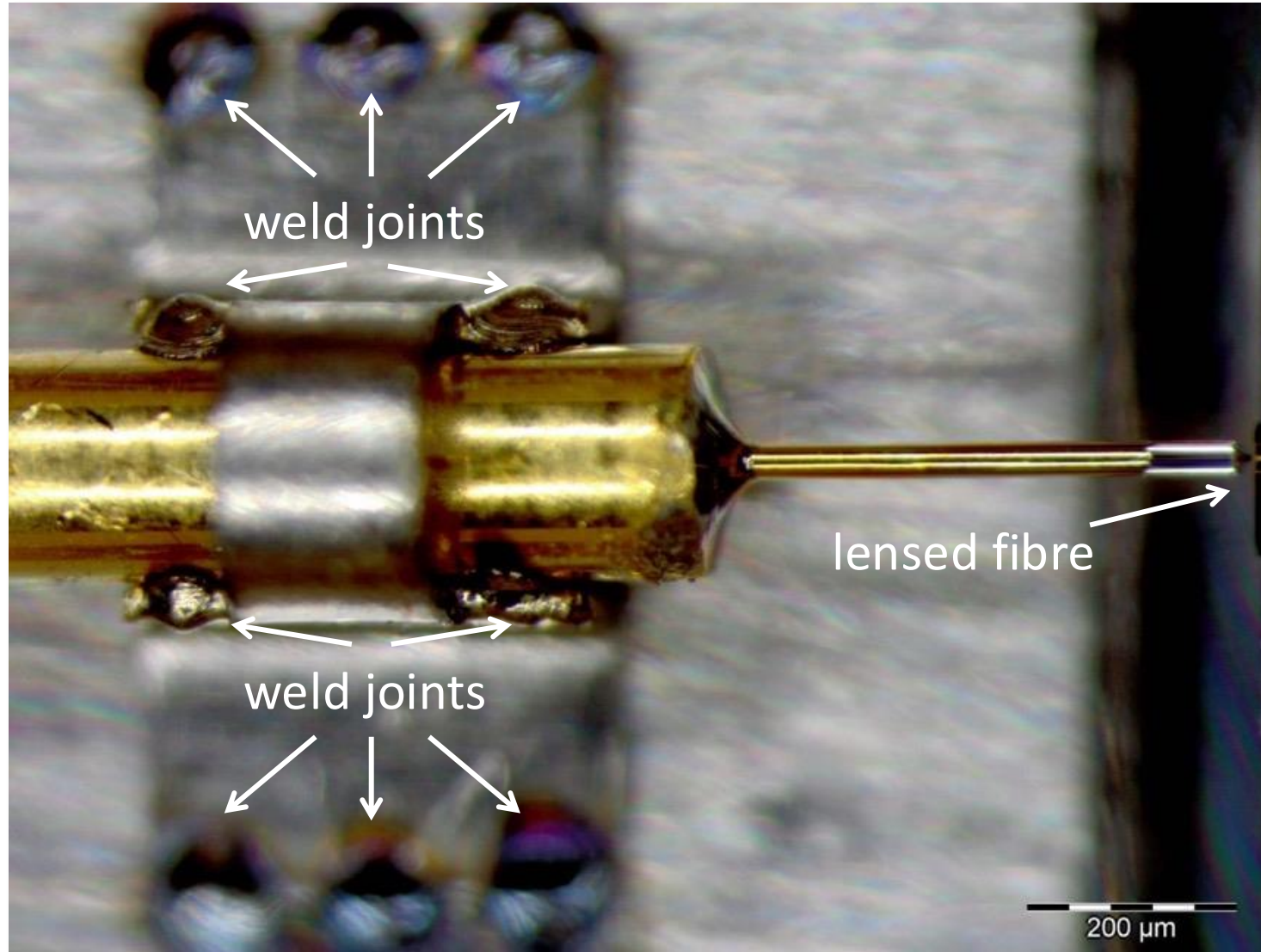


Three Cameras to Facilitate (Coarse) Visual Alignment as well as Weld Spot Placement.

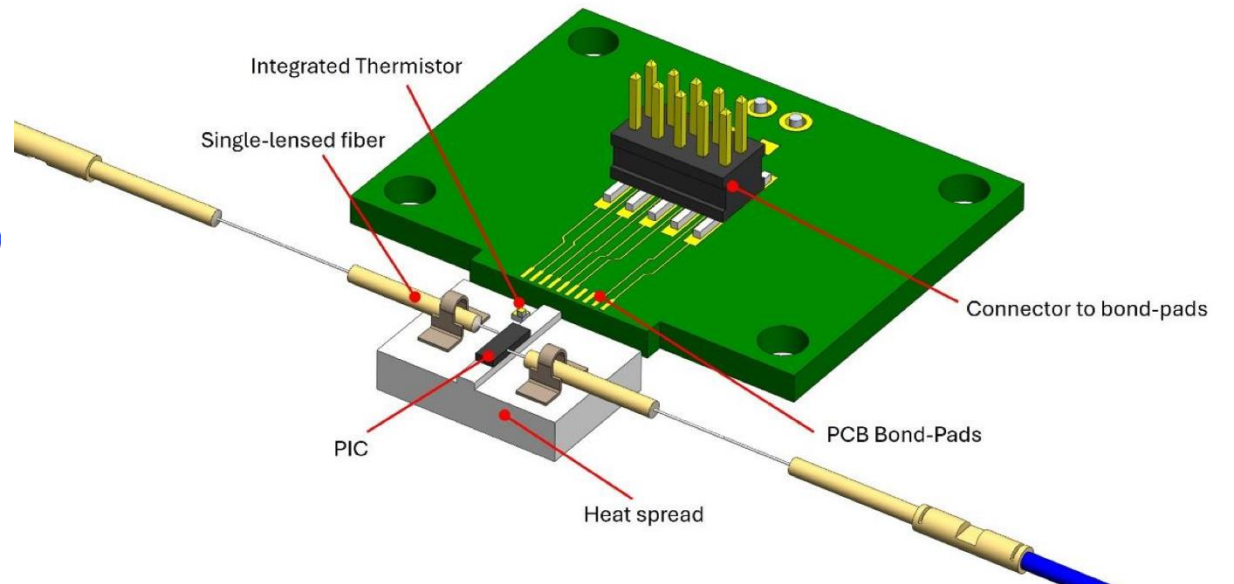
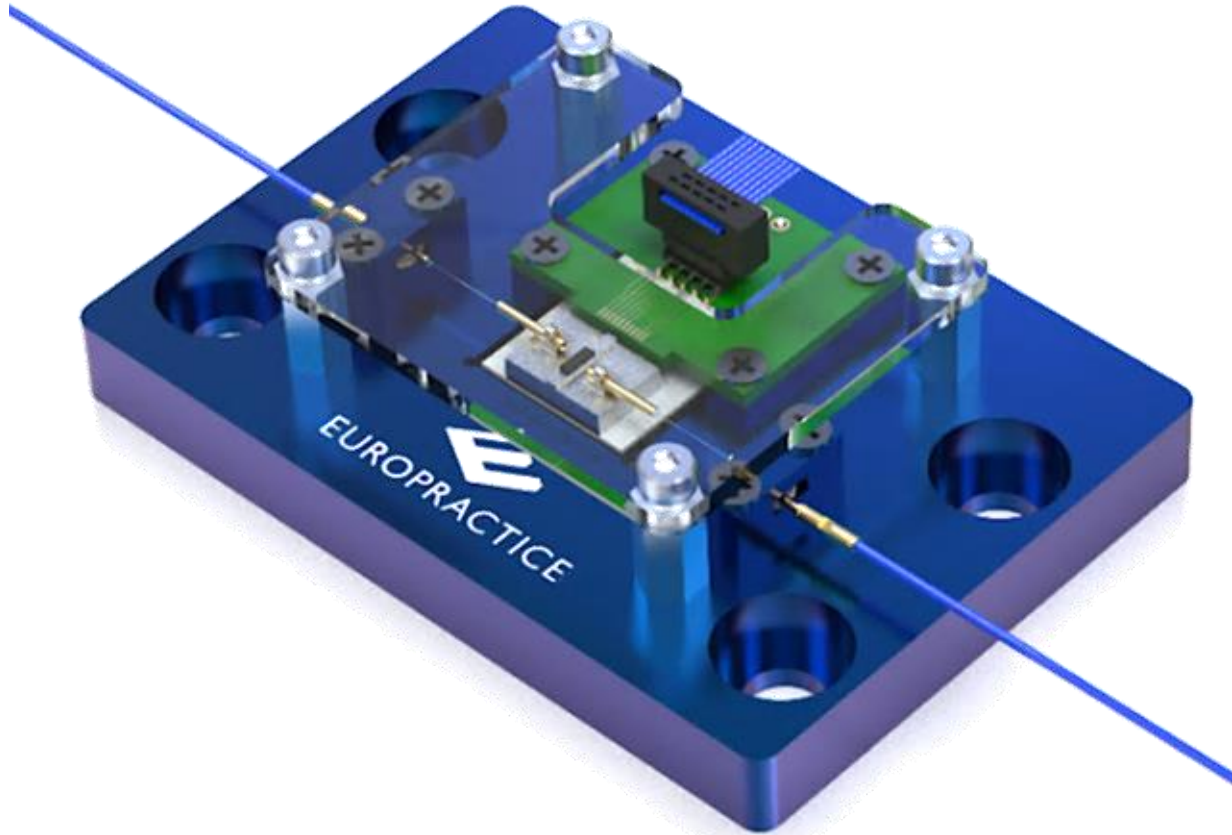


Microscope View of a Tapered Lensed Fibre Attached Using the Laser Welder

Fiber Optic Packaging (edge coupled)



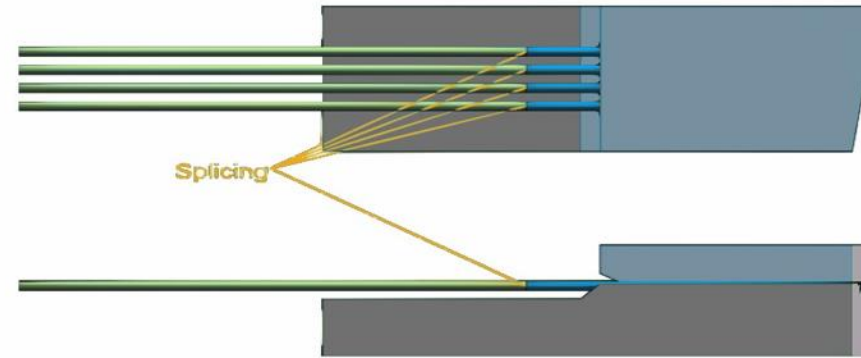
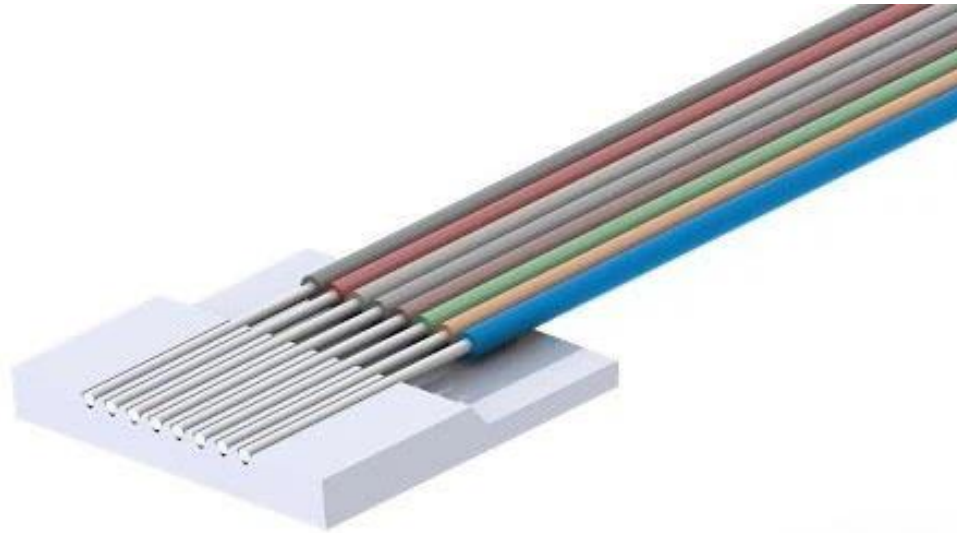
Fiber Optic Packaging (edge coupled)



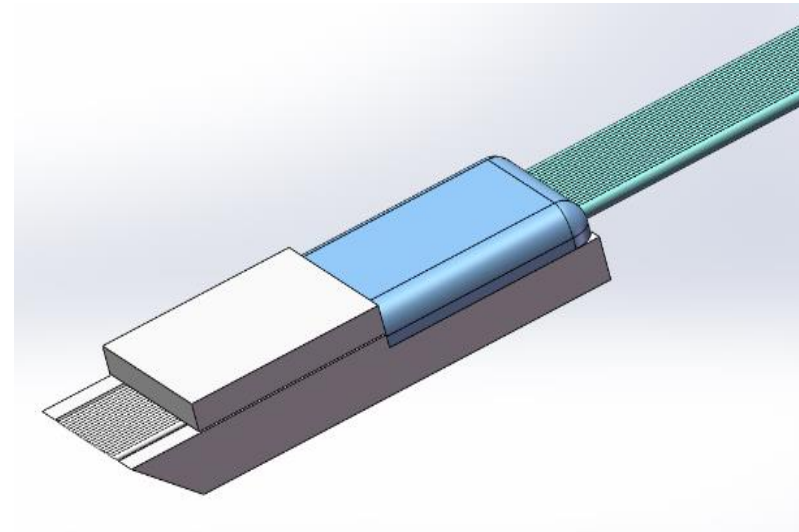
Fiber Optic Packaging (fiber arrays)



Meisu Optics

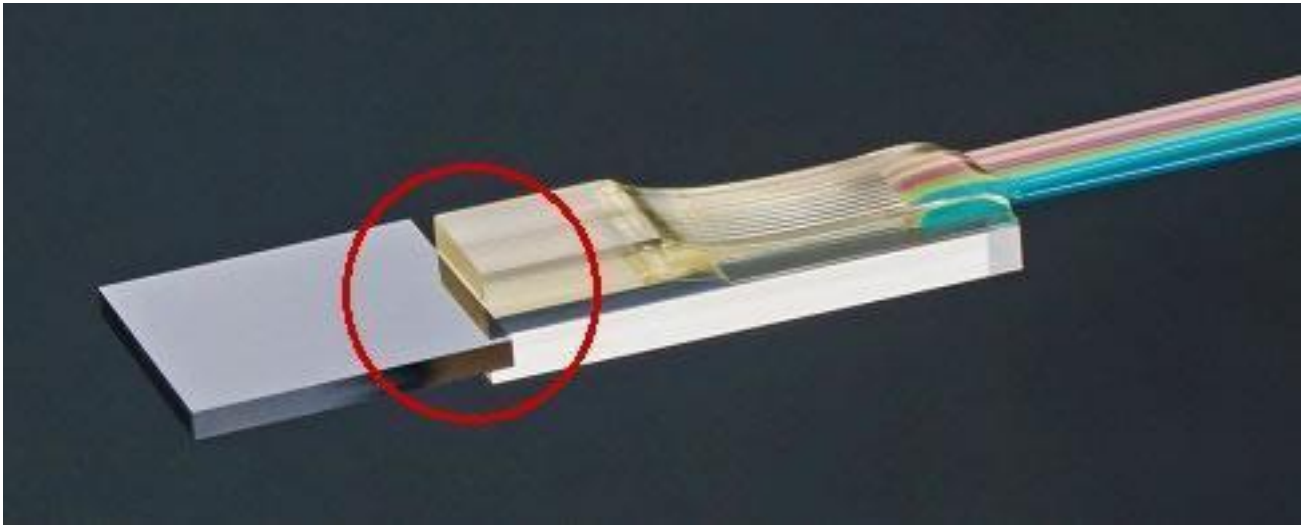


-  Standard single mode fiber
-  High-NA fiber

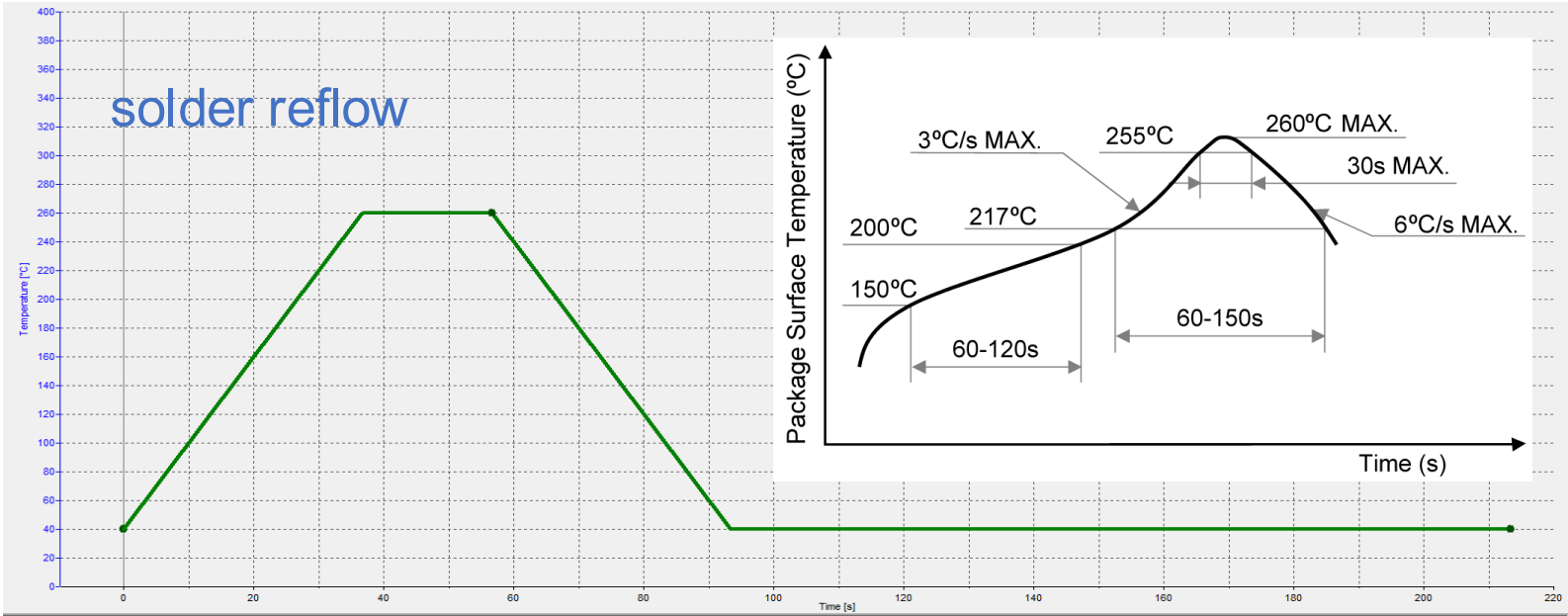
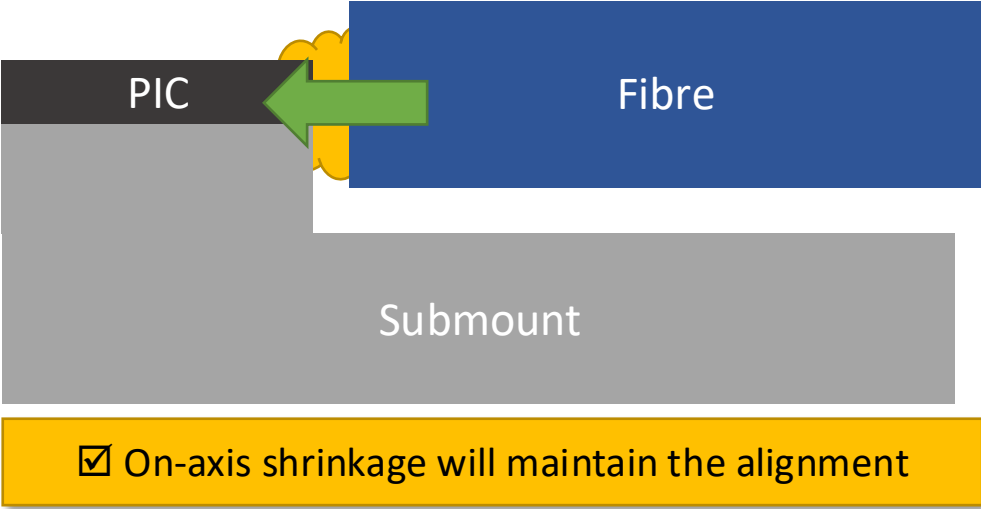
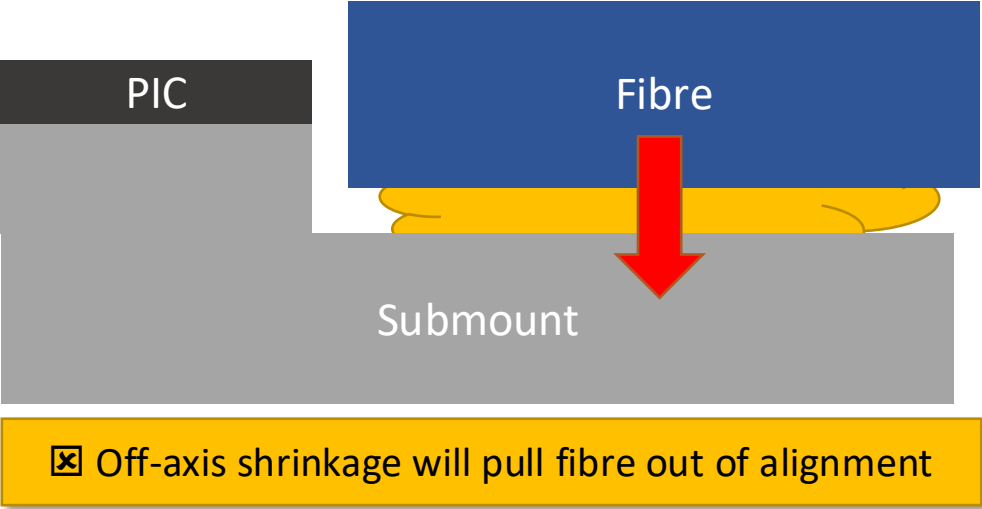


Fiber Optic Packaging (epoxies)

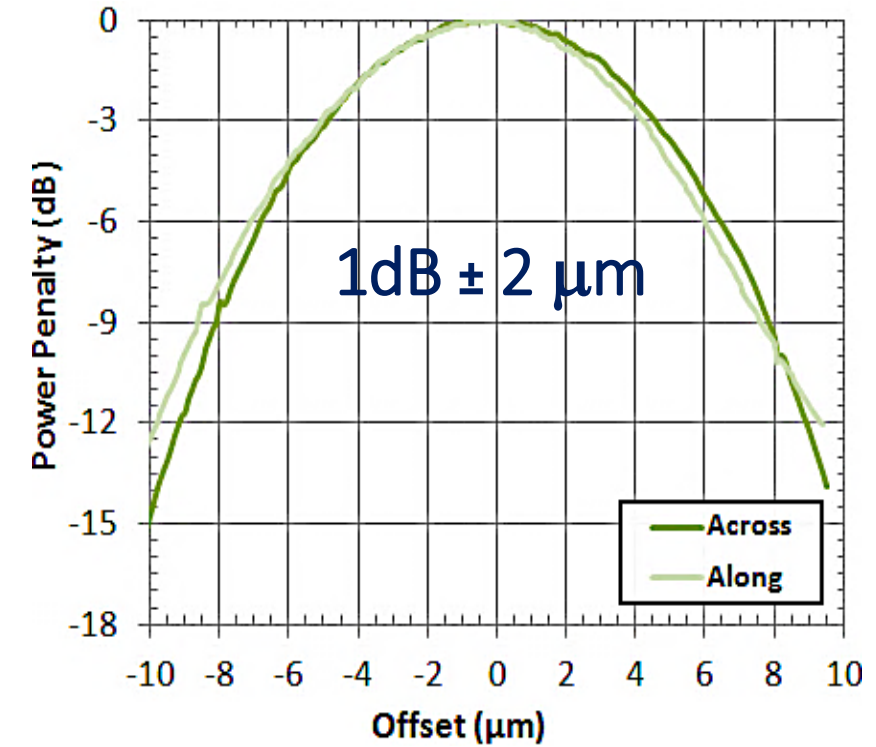
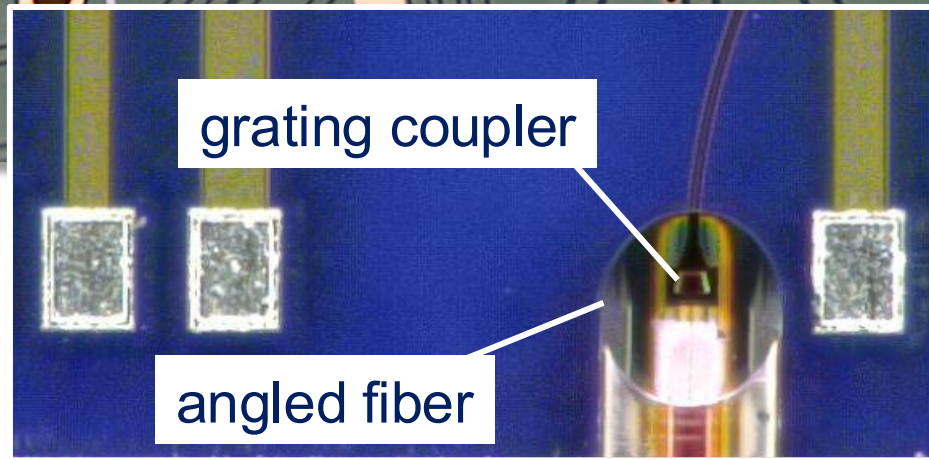
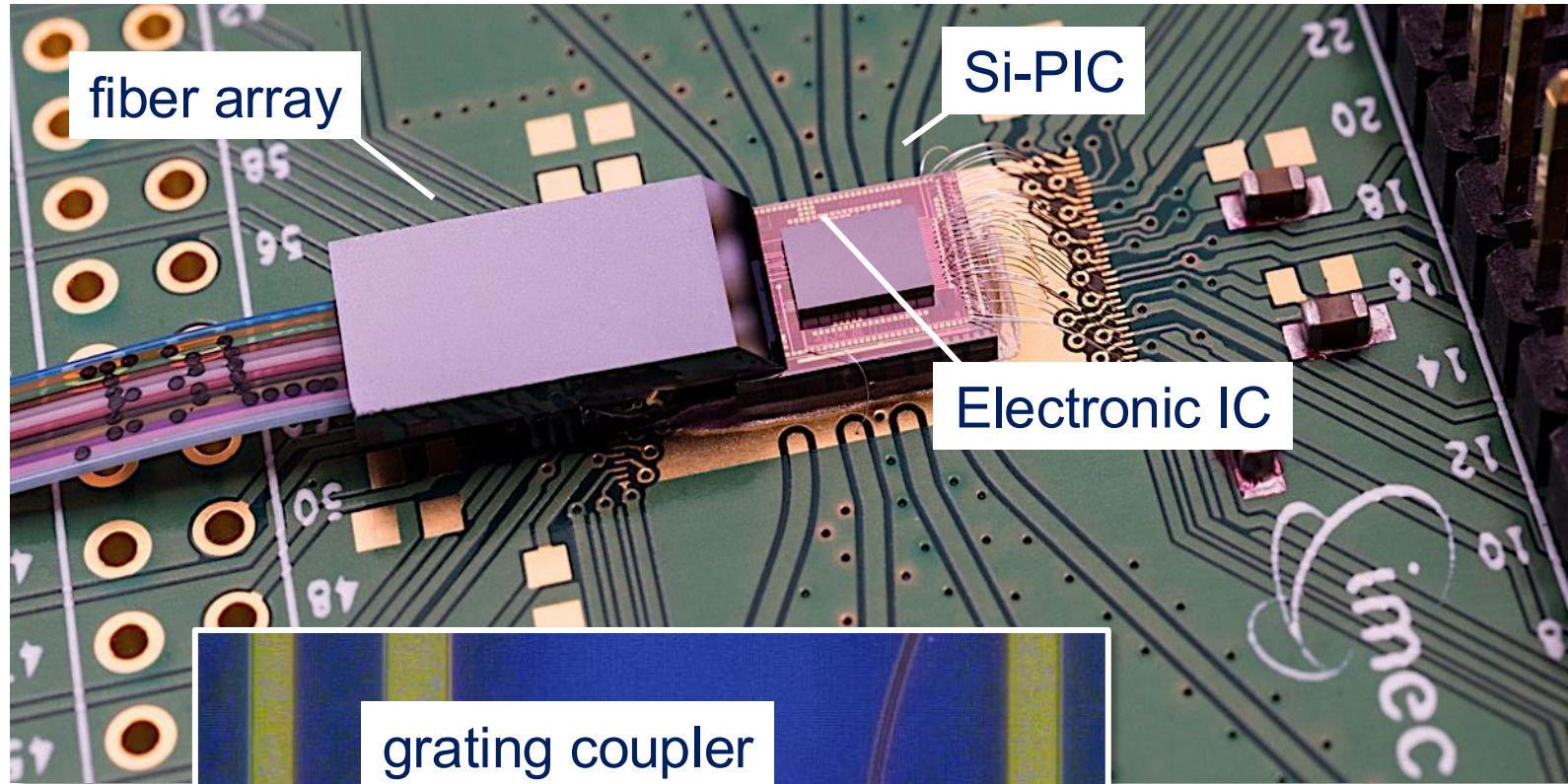
Model# [Main ingredient]	Viscosity (mPa·s)	Curing conditions [irradiation level &time]	Curing Shrinkage Rate (%)	Glass transition temperature Tg (°C)	Thermal Expansion Coefficient (ppm/°C)	Bending adhesion strength (kgf/cm ²)	
						Initial period	121°C100% after10h
AT3862P [Epoxy]	500,000	100mW/cm2 2min	0.5	195	20	>210	>114
AT3916P [Epoxy]	20,000	100mW/cm2 5min	0.9	233	18	>220	>128



Fiber Optic Packaging (epoxies)

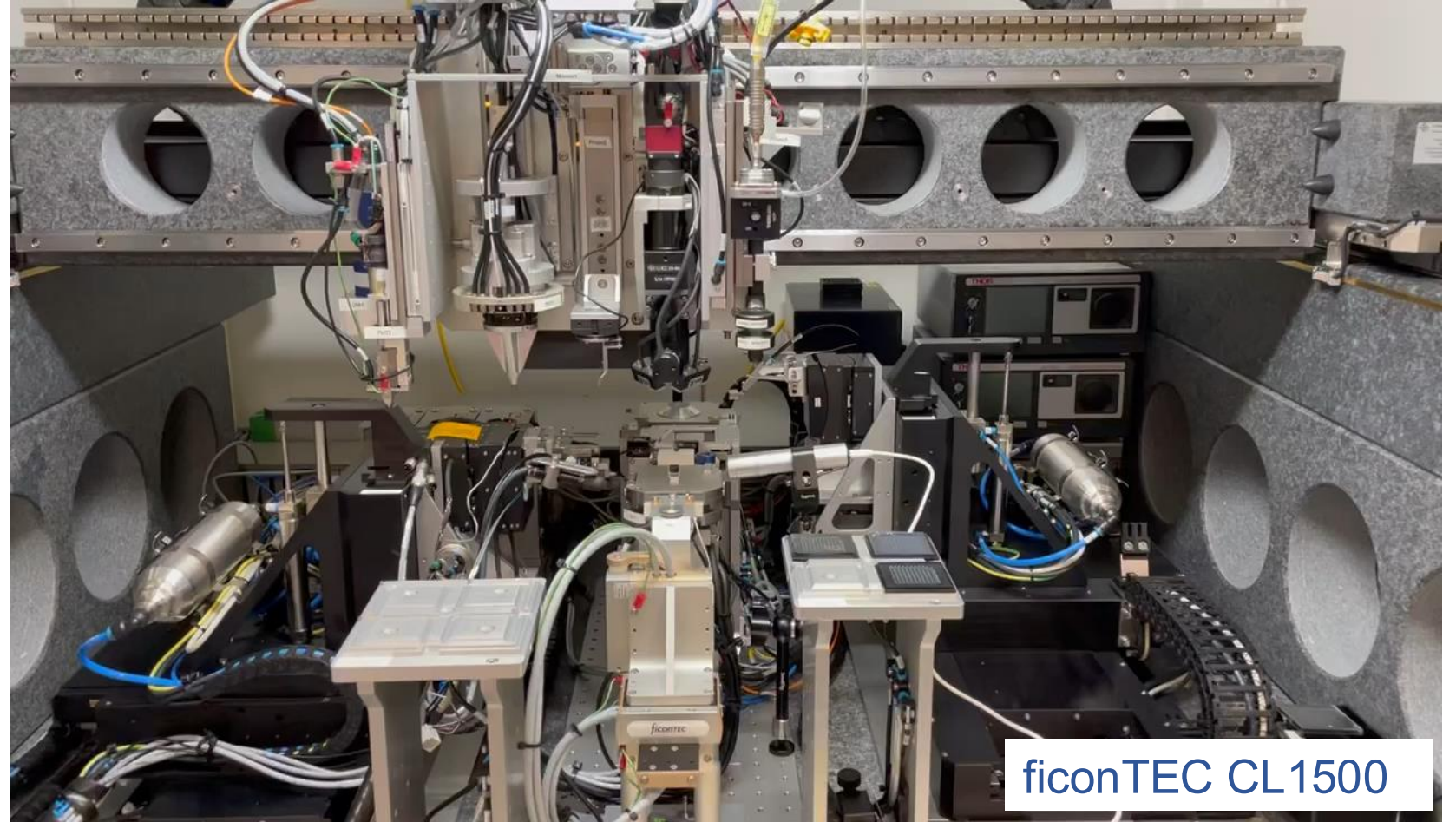
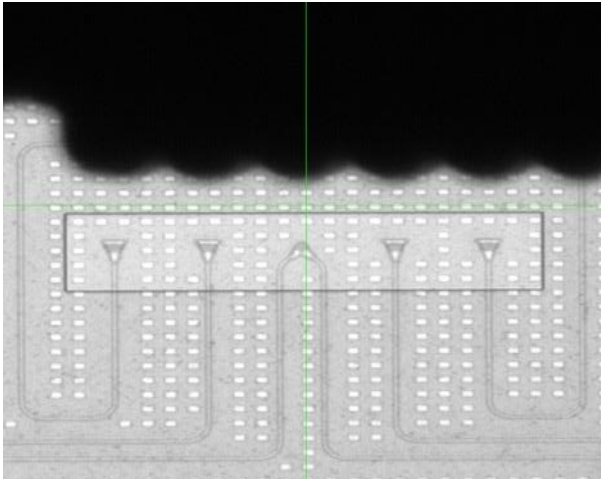
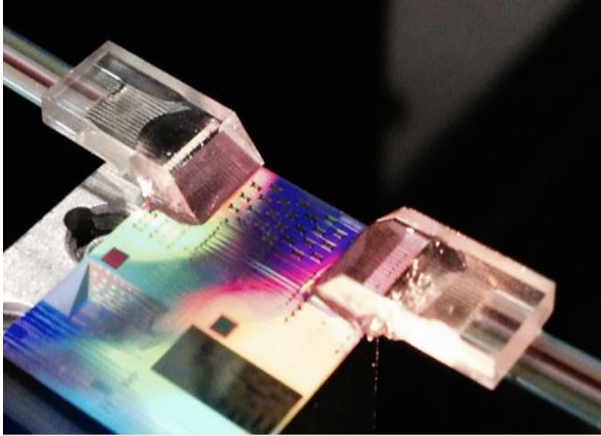


Fiber Optic Packaging (grating coupled)



4×20Gb/s WDM ring-based hybrid CMOS silicon photonics transceiver, ISSCC, San Francisco, 2015.

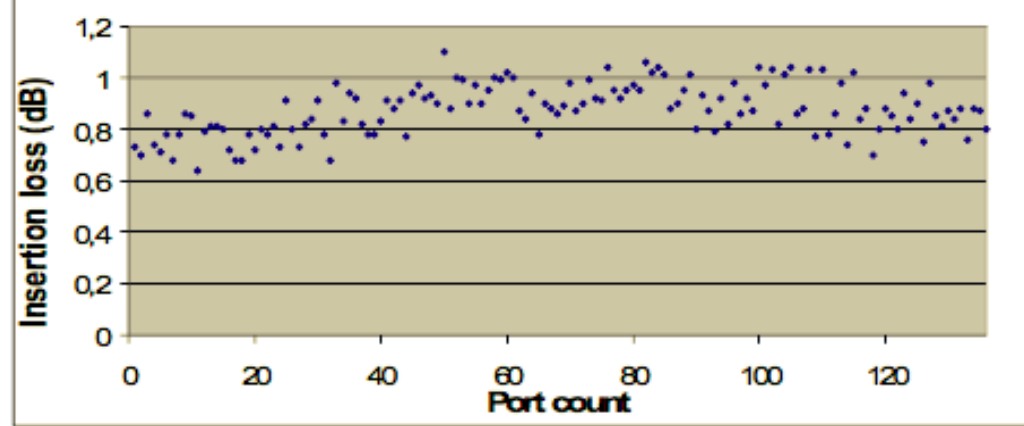
Fiber Optic Packaging (grating coupled)



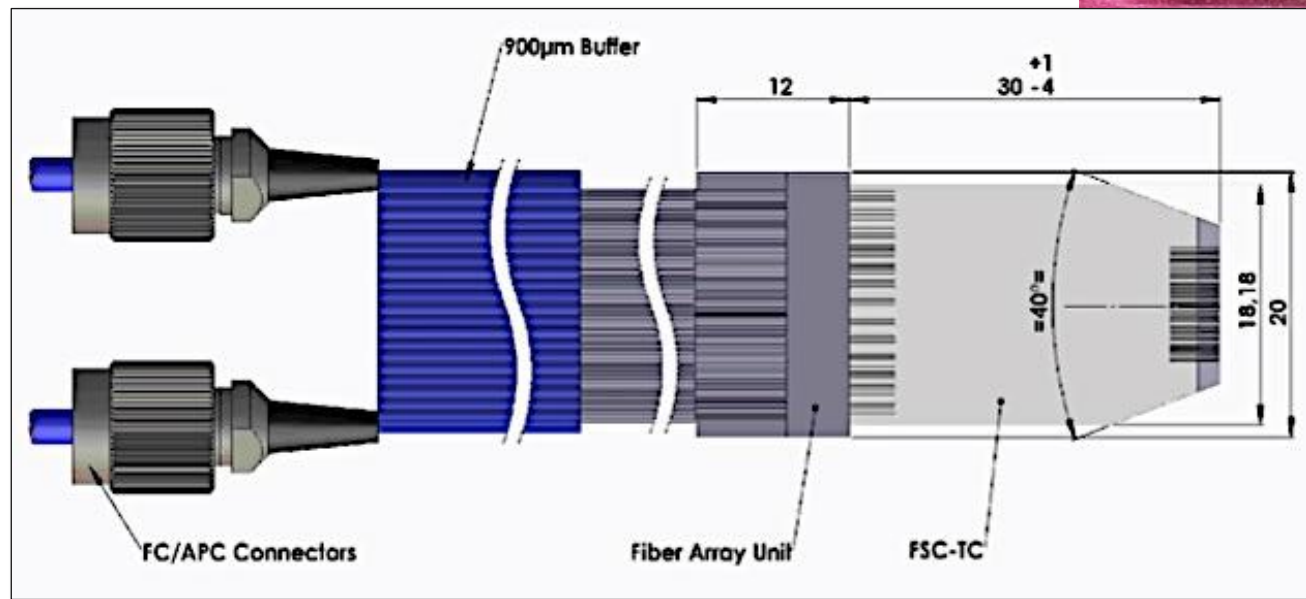
Experimental Characterization of Particle Swarm Optimized Focusing Non-Uniform Grating Coupler for Multiple SOI Thicknesses
IEEE Journal of Lightwave Technology, Vol 39, Issue 15, 2021

Fiber Optic Packaging (grating coupled)

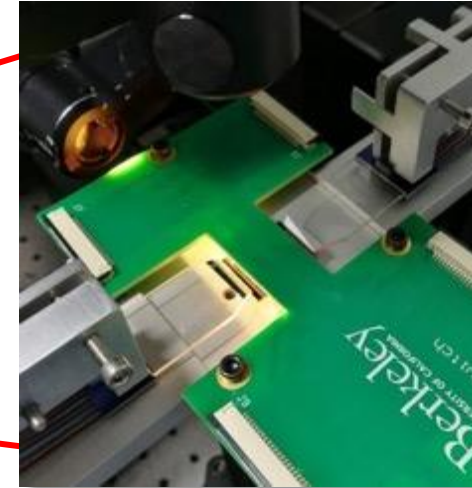
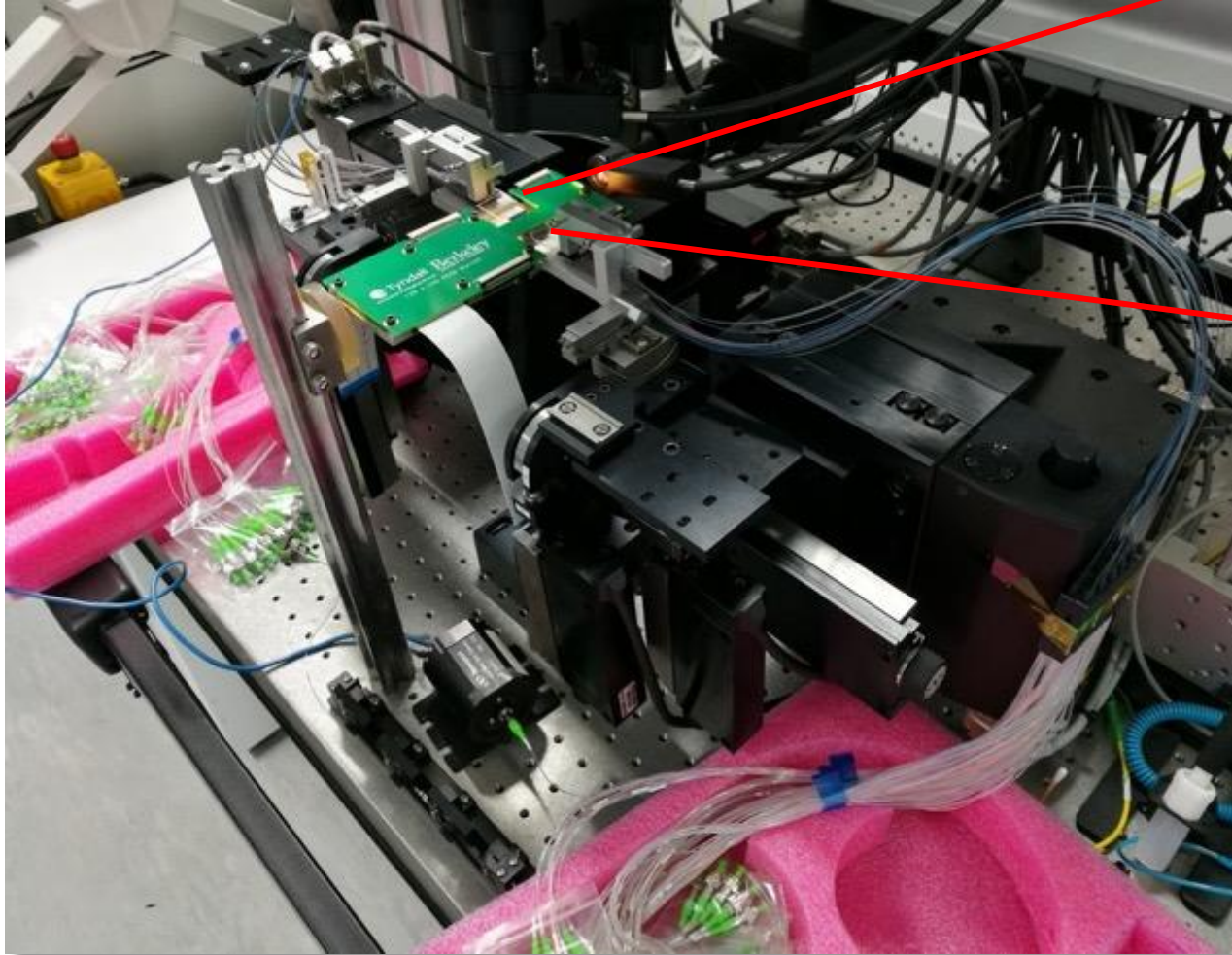
136 Channel Planar Fiber Array



Fiber Array Block

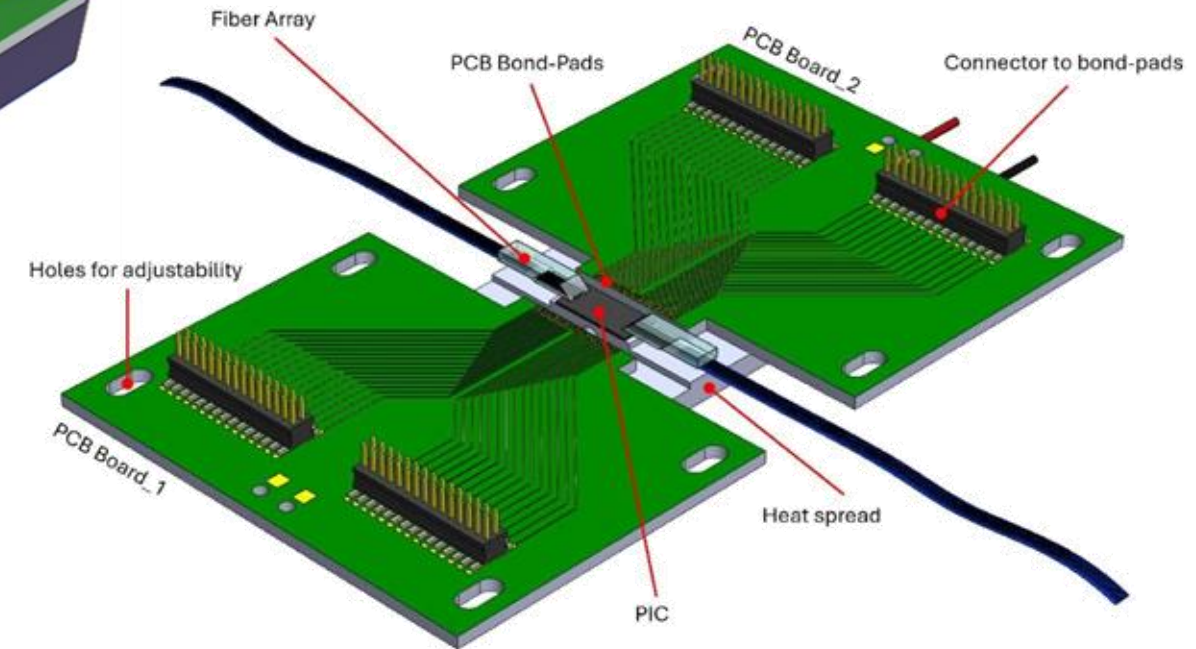
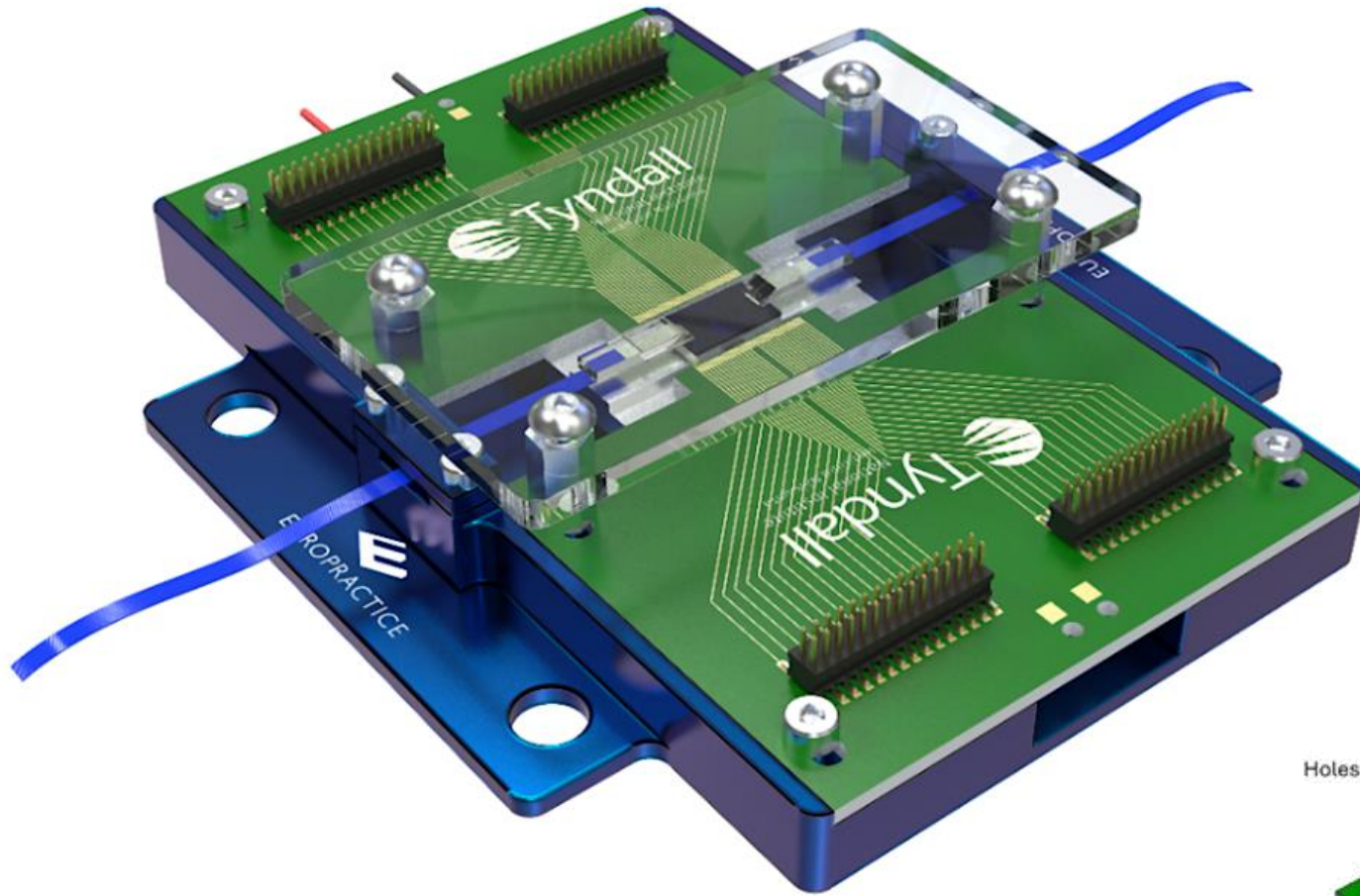


Fiber Optic Packaging (grating coupled)

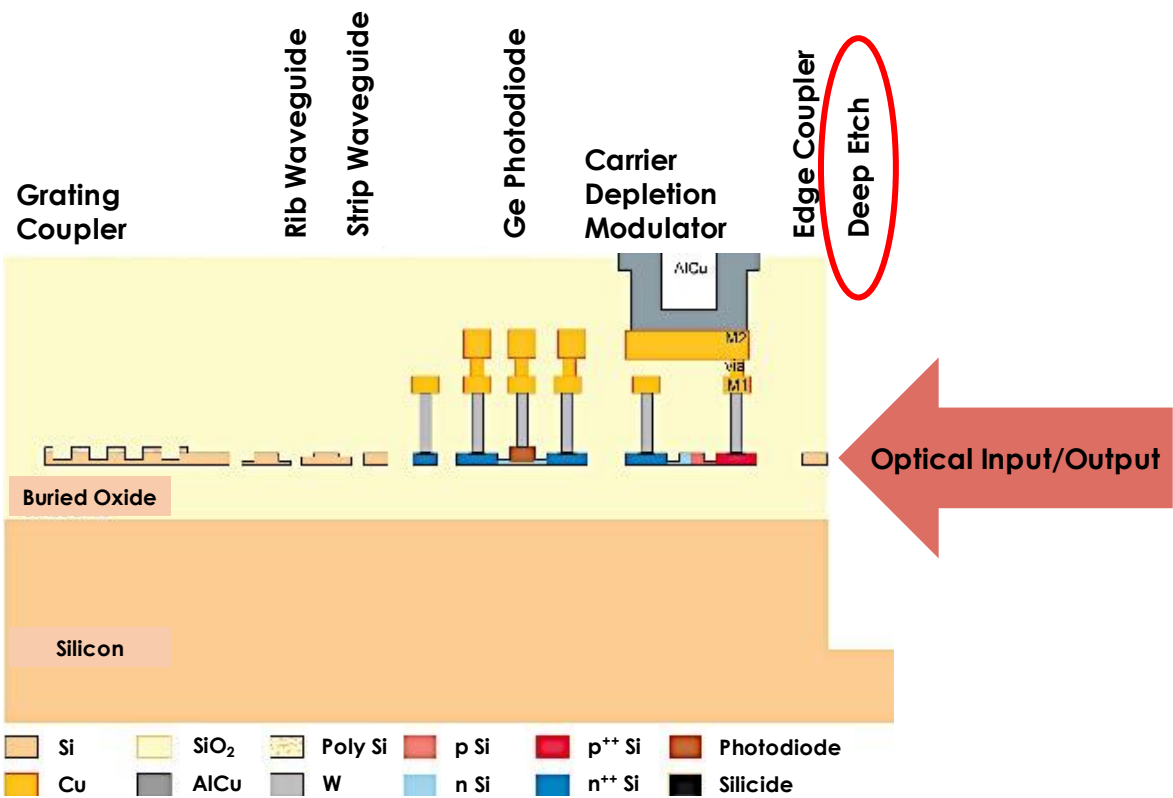


'Flip Chip Packaging of Digital Silicon Photonics MEMS Switch for Cloud Computing and Data Centre', HY Hwang, JS Lee, TJ Seok, A Forencich, HR. Grant, D Knutson, N Quack, S Han, RS Muller, GC Papen, MC Wu, P O'Brien, IEEE Photonics Journal, Volume: PP, Issue: 99, June 2017.

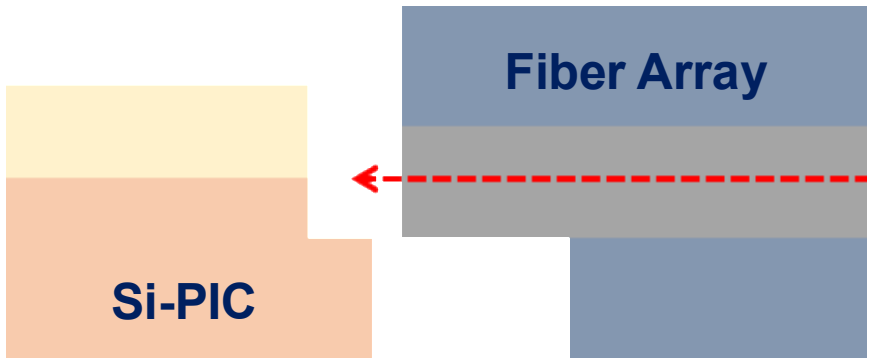
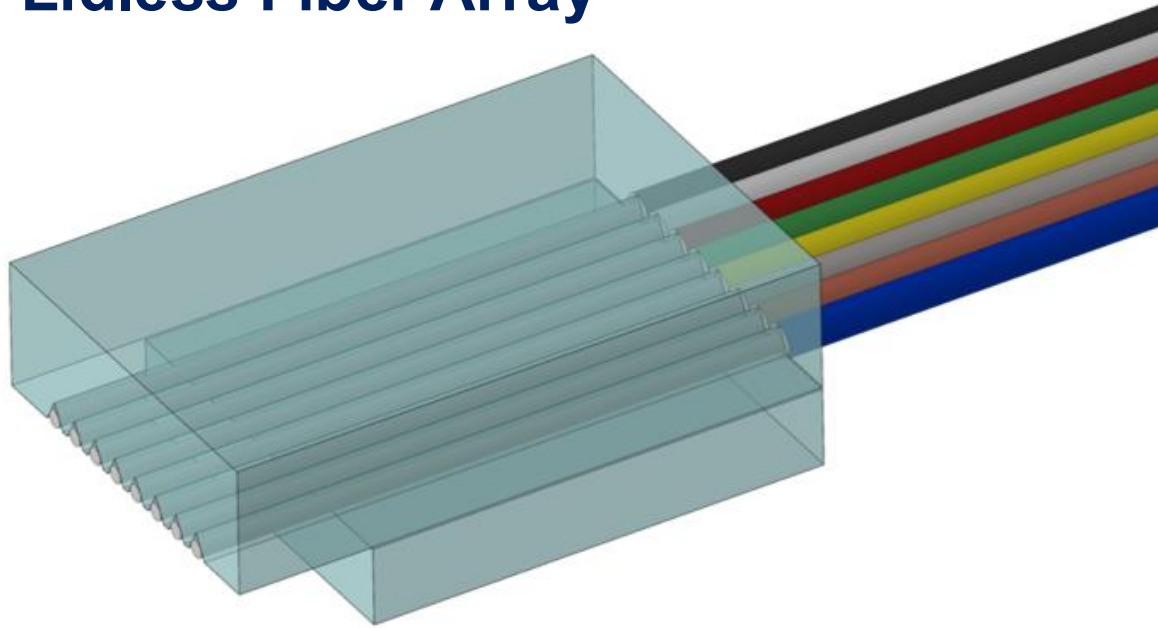
Fiber Optic Packaging (grating coupled)



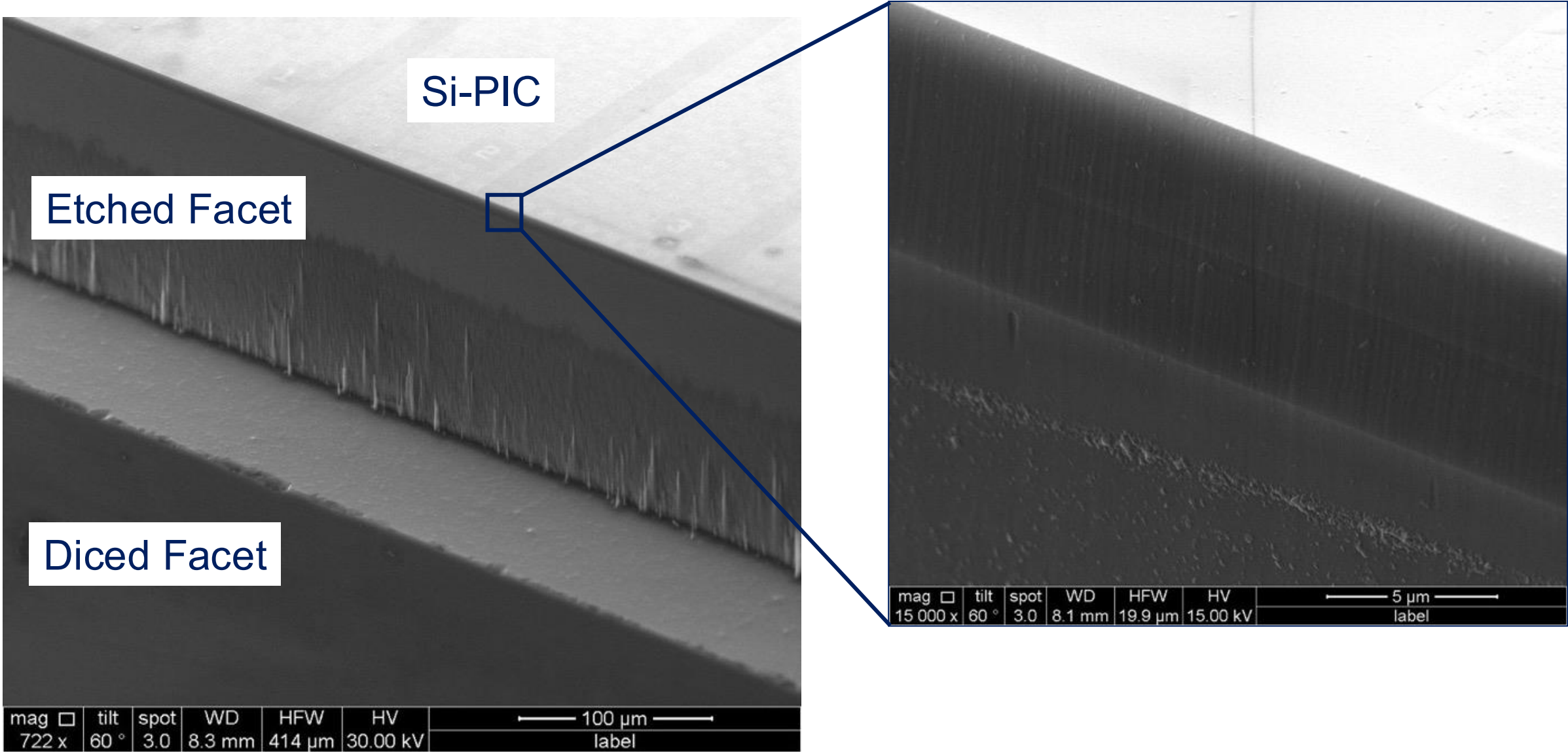
Fiber Optic Packaging (edge coupled)



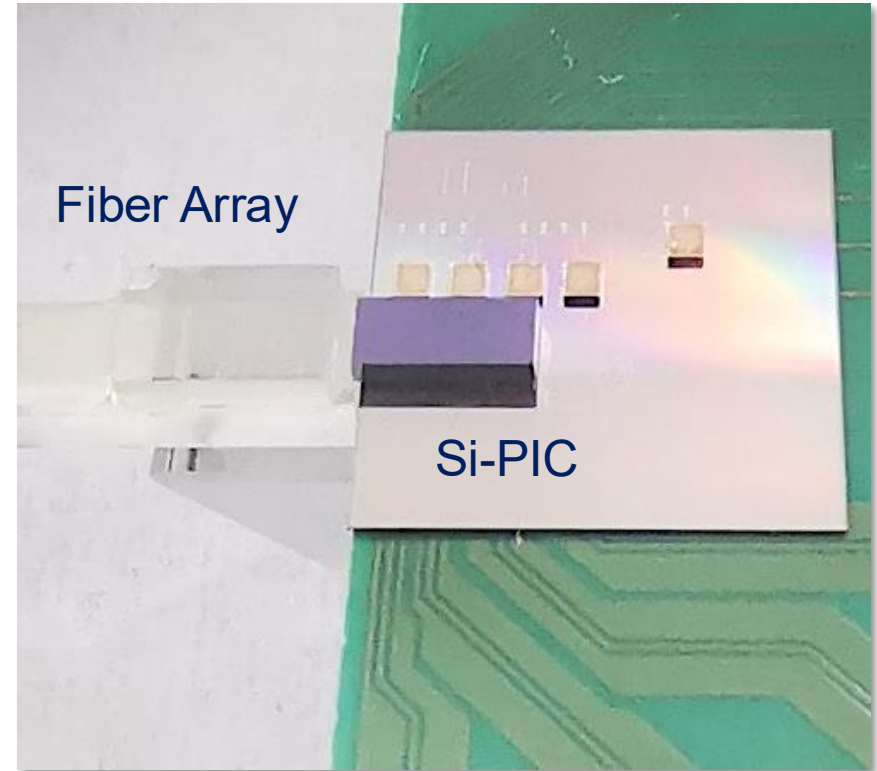
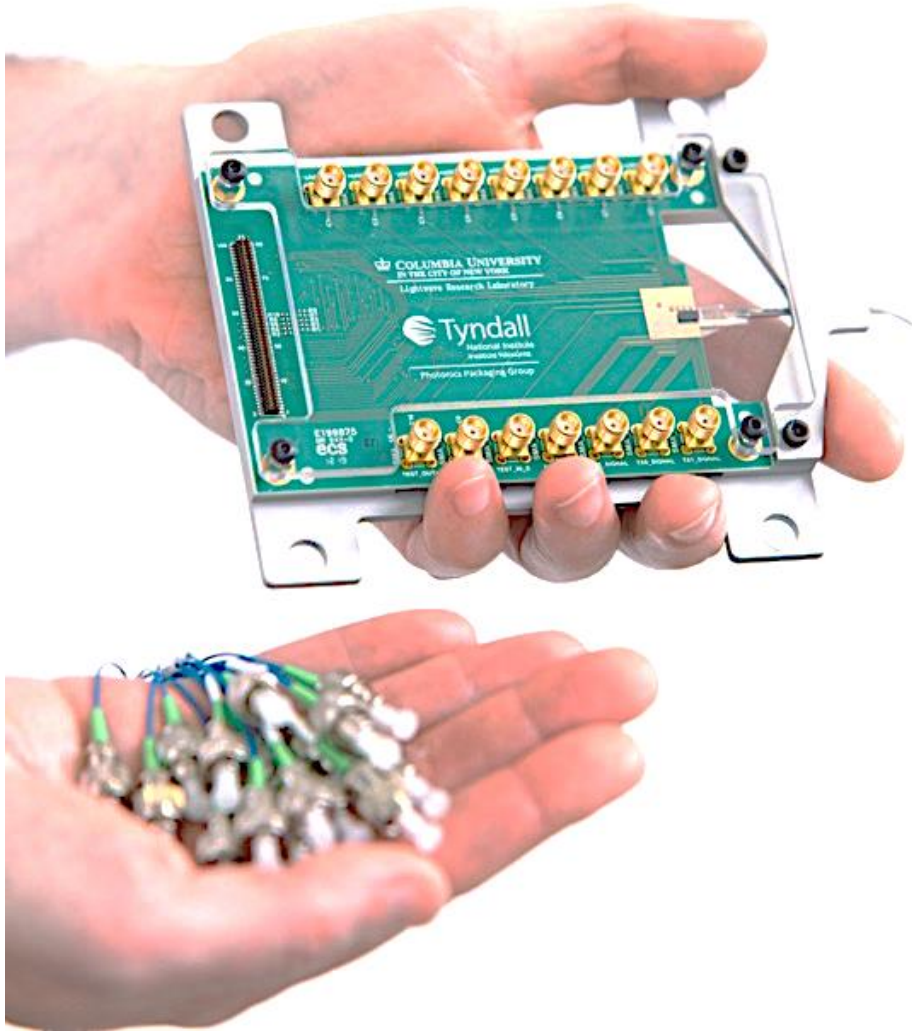
Lidless Fiber Array



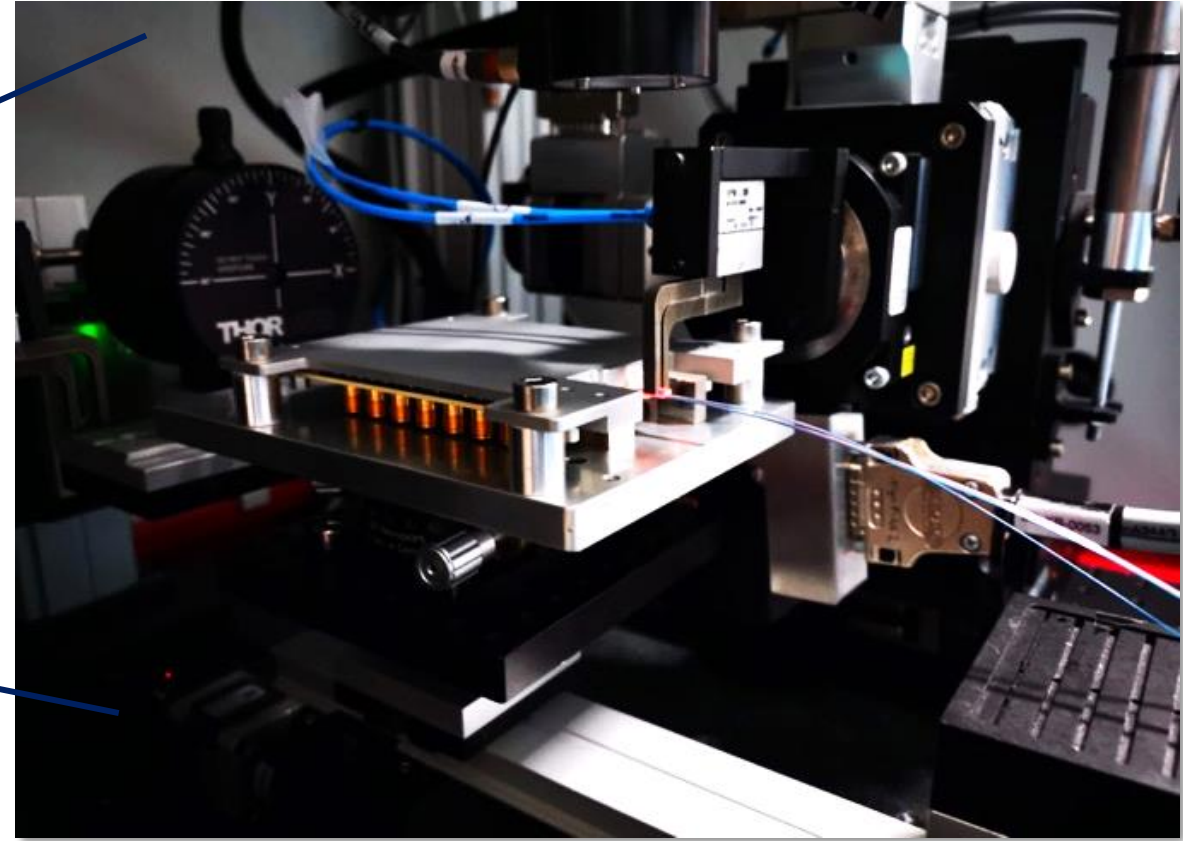
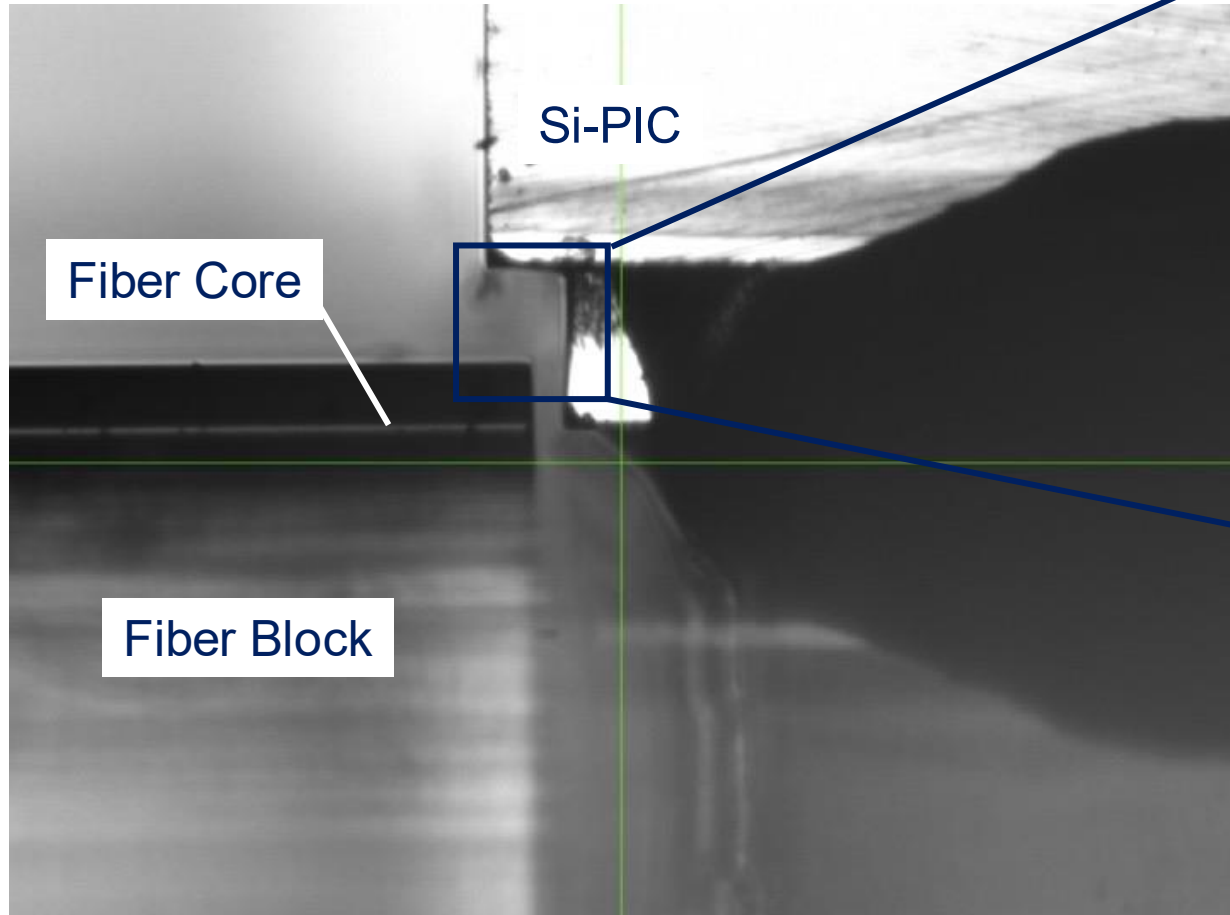
Fiber Optic Packaging (edge coupled)



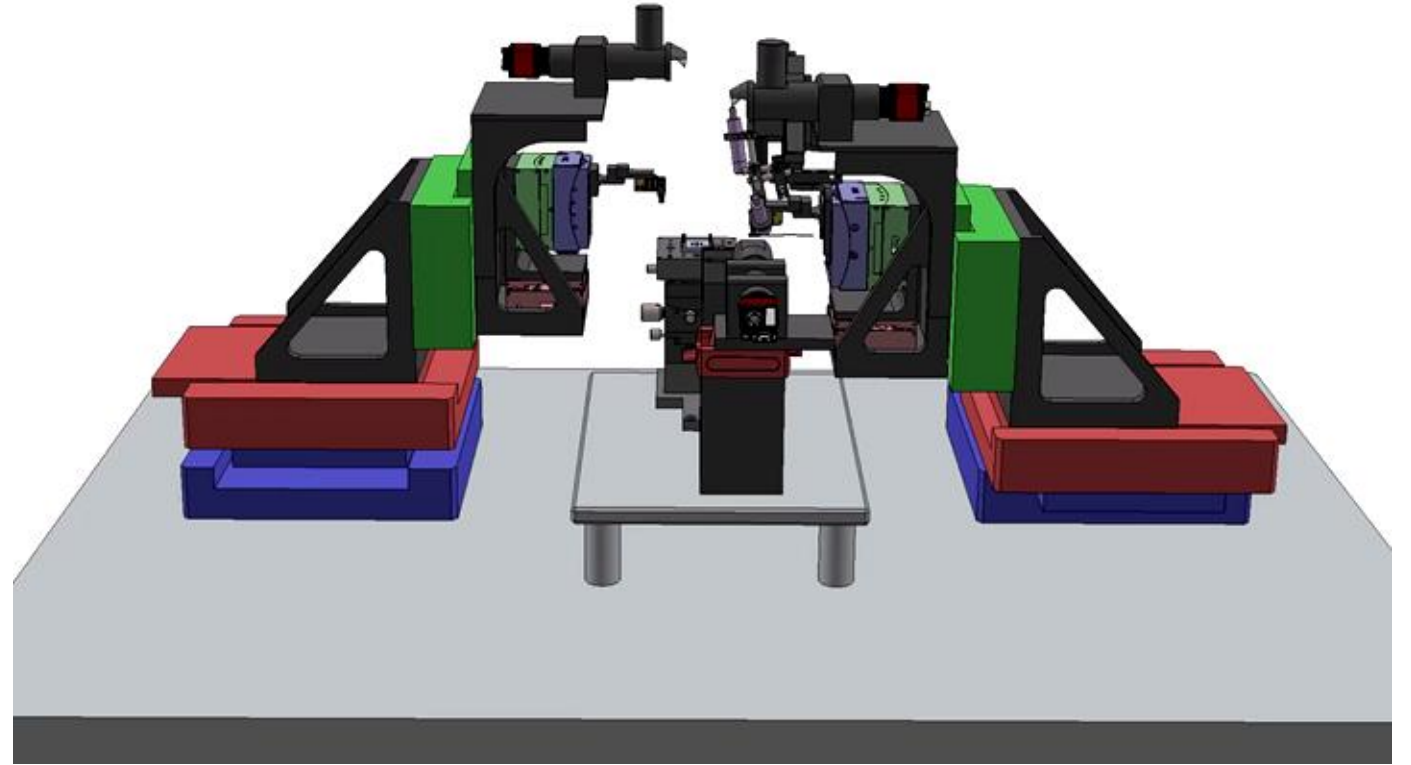
Fiber Optic Packaging (edge coupled)



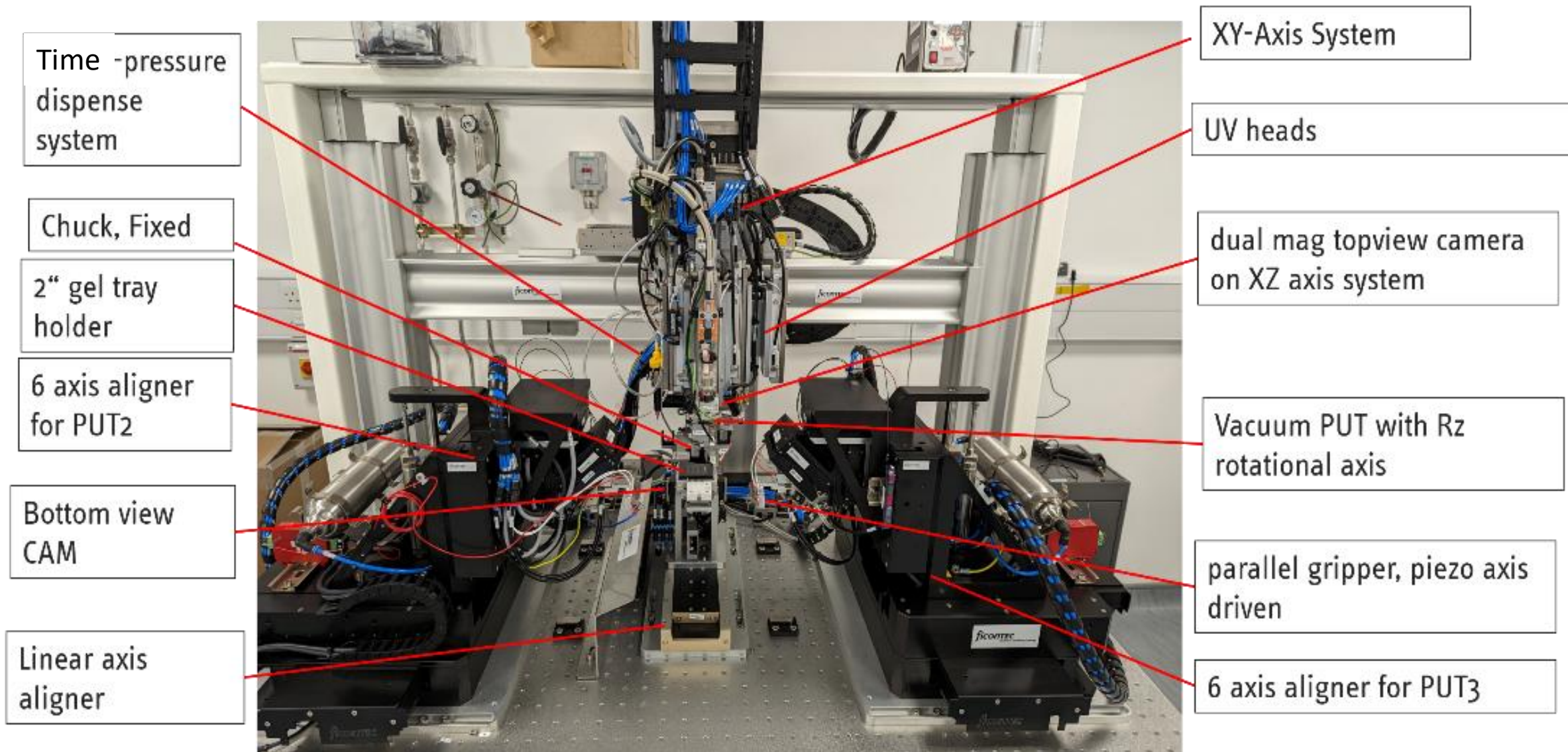
Fiber Optic Packaging (edge coupled)



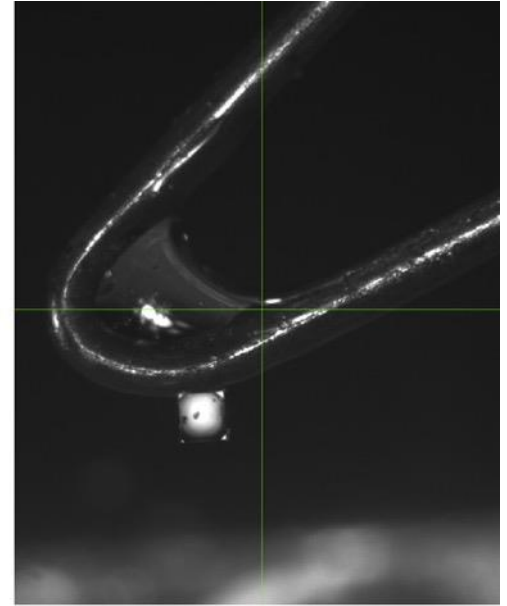
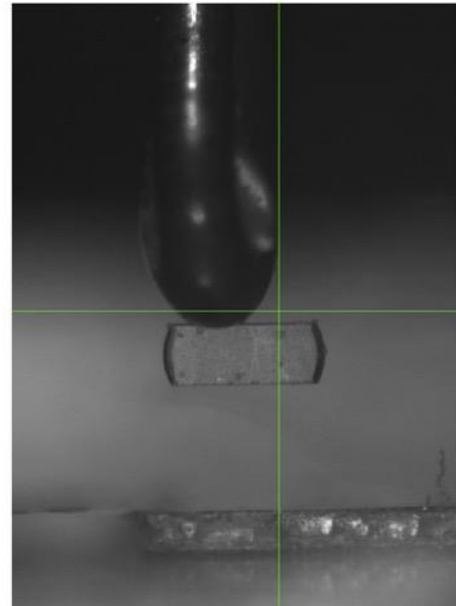
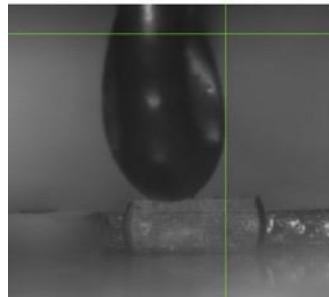
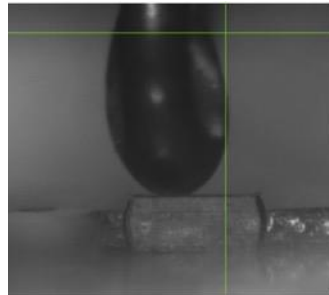
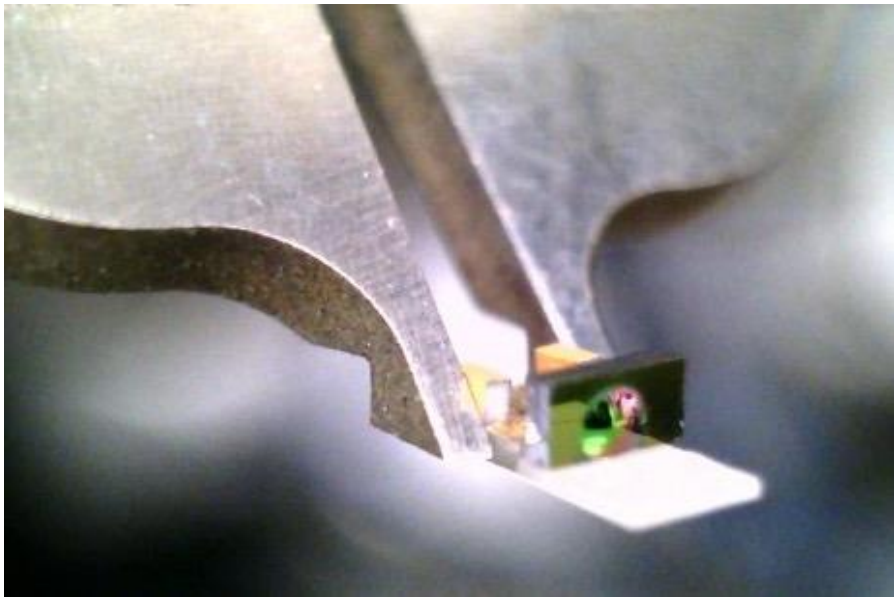
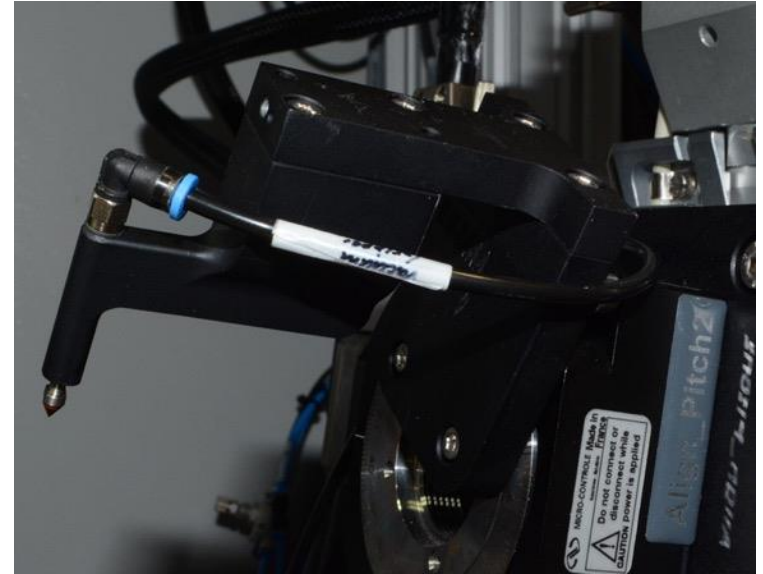
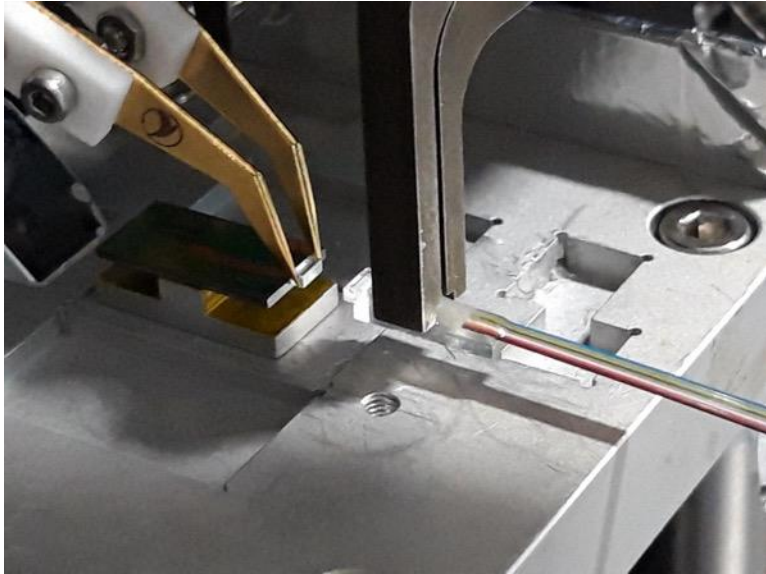
Fiber Optic Packaging (edge coupled)



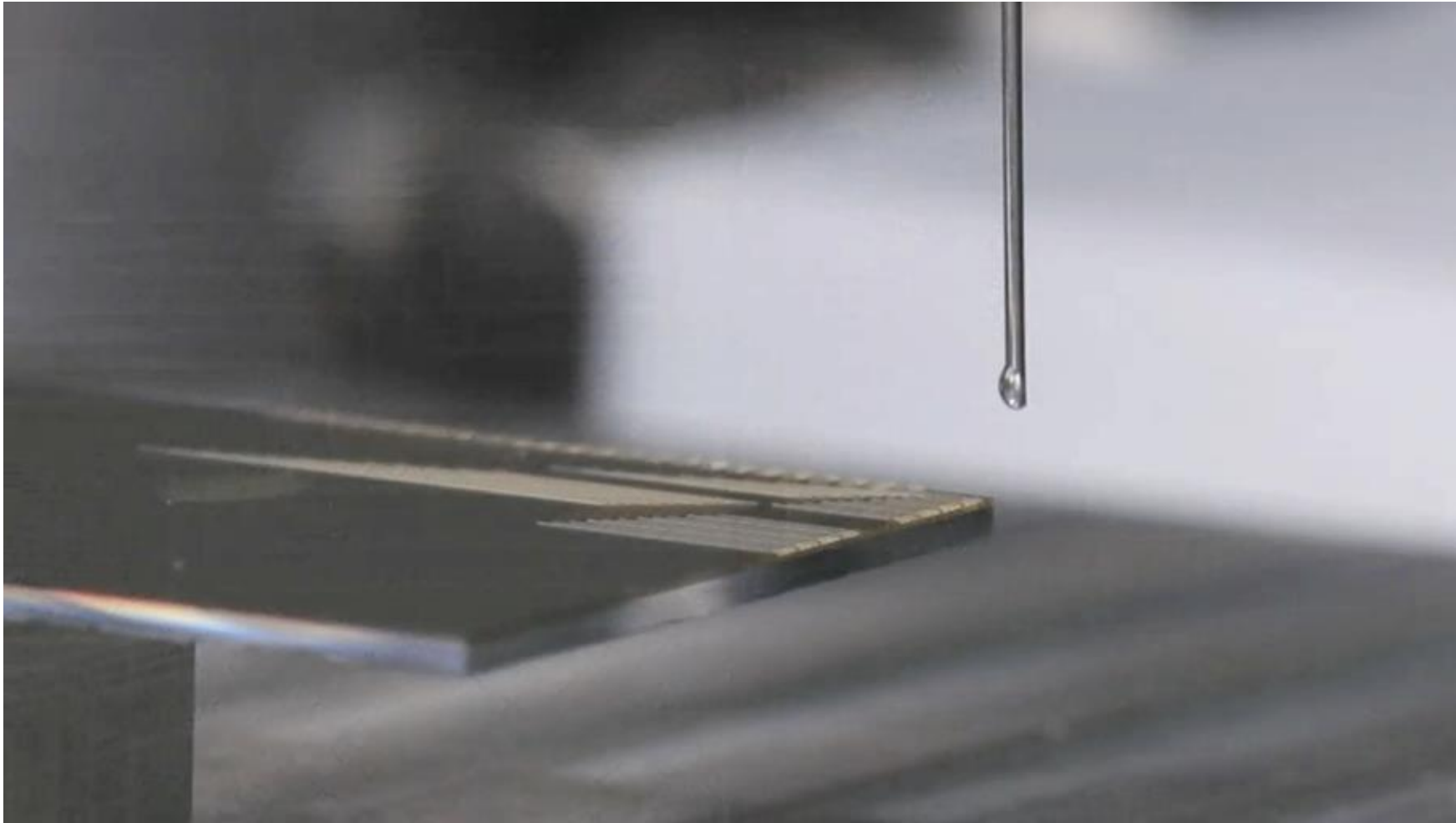
Fiber Optic Packaging (edge coupled)



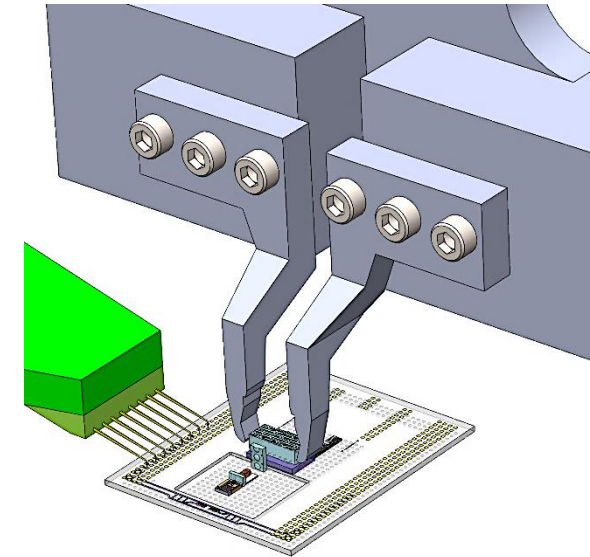
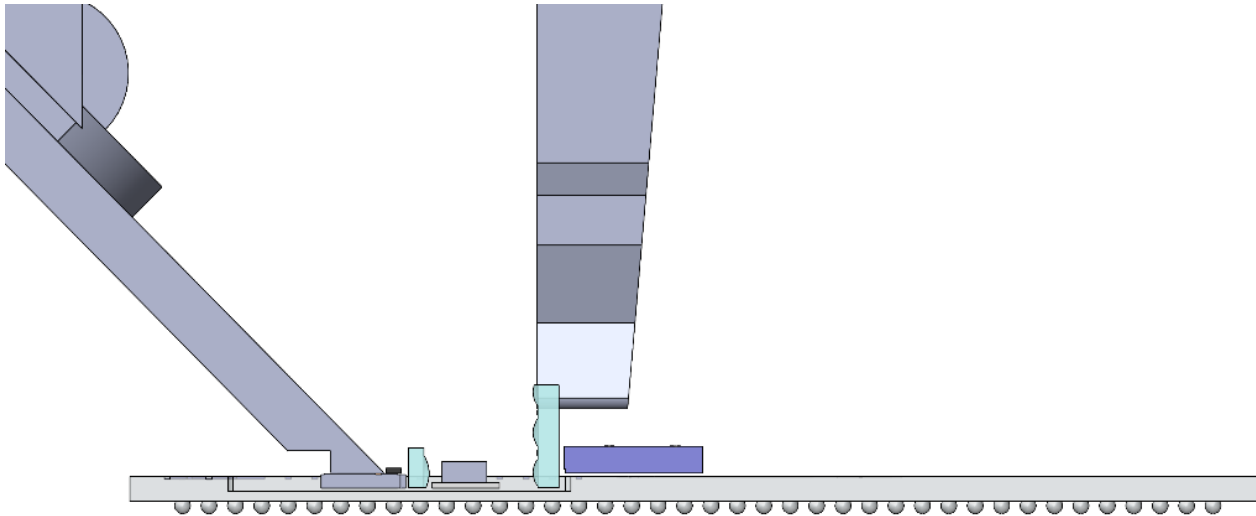
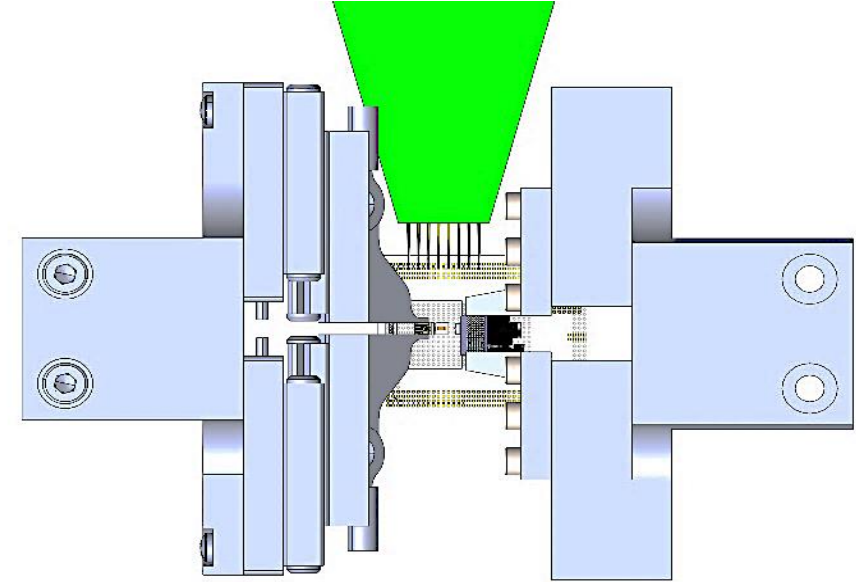
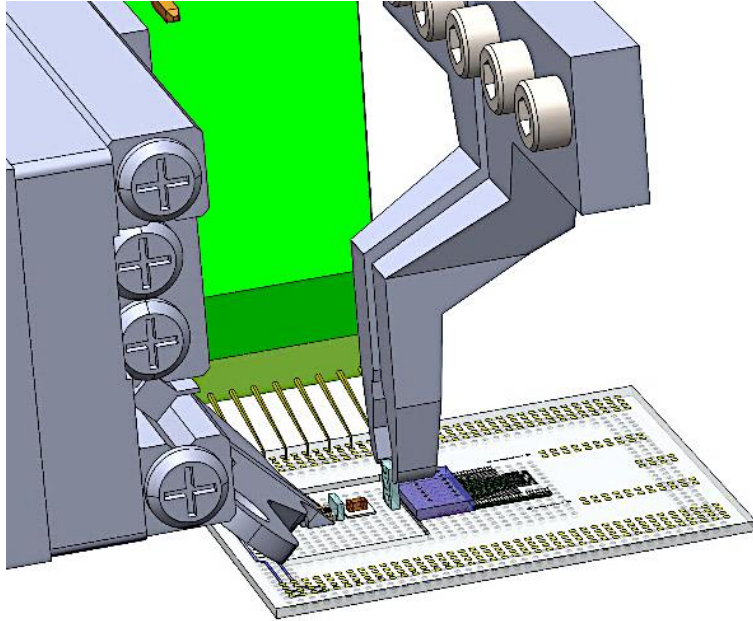
Fiber Optic Packaging (edge coupled)



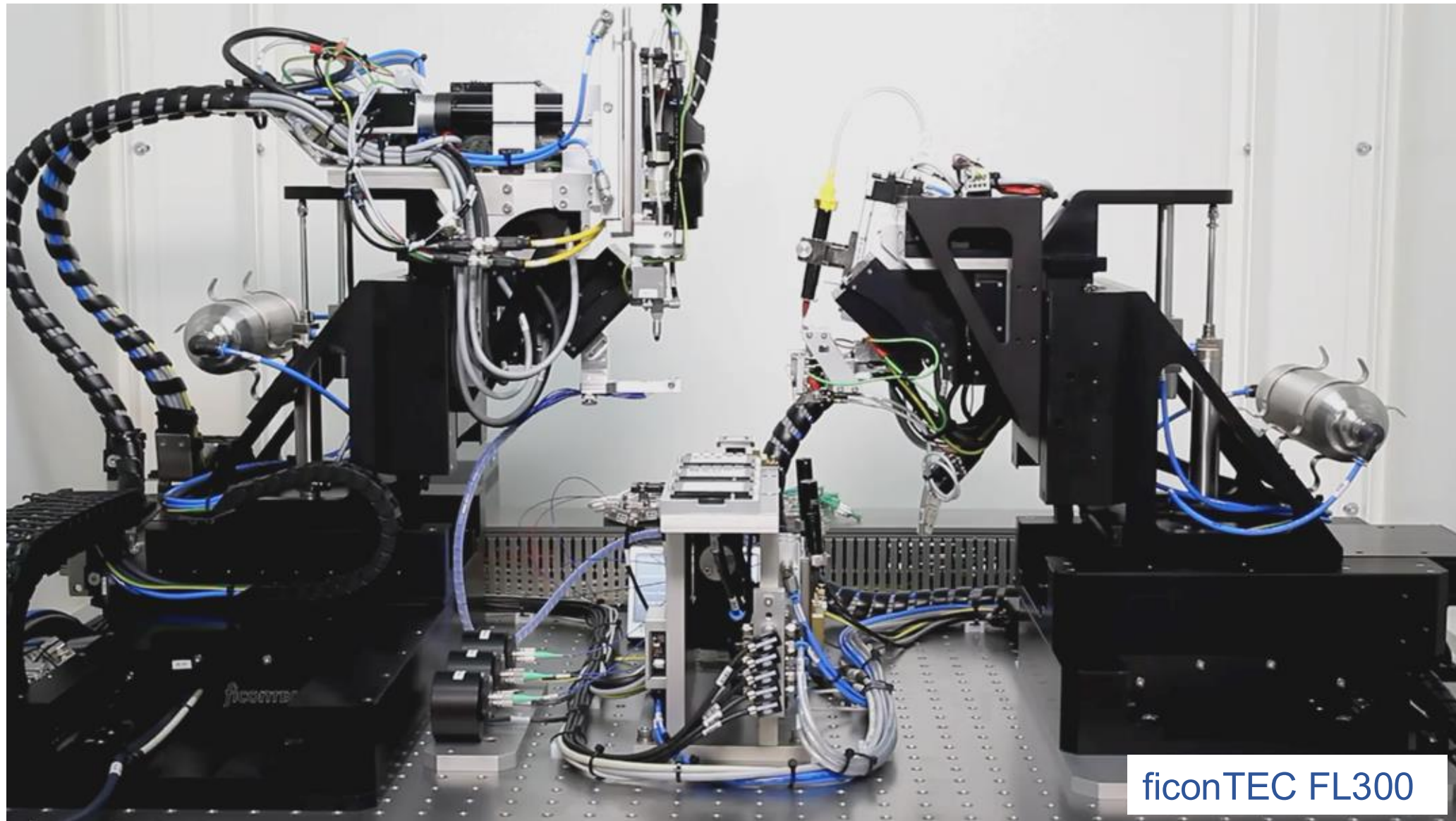
Fiber Optic Packaging (edge coupled)



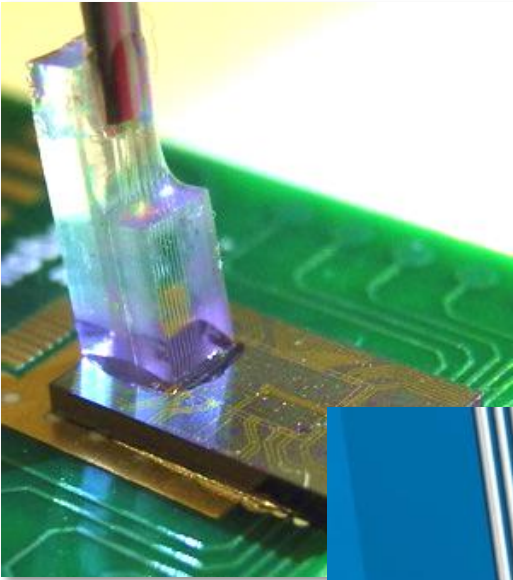
Fiber Optic Packaging (edge coupled)



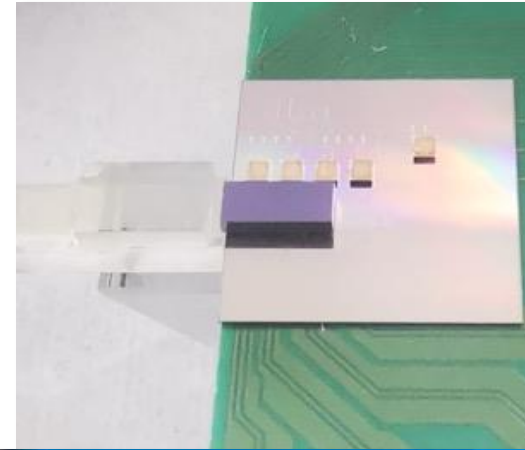
Fiber Optic Packaging (edge coupled)



Micro Optic Packaging (expanded beam coupling)

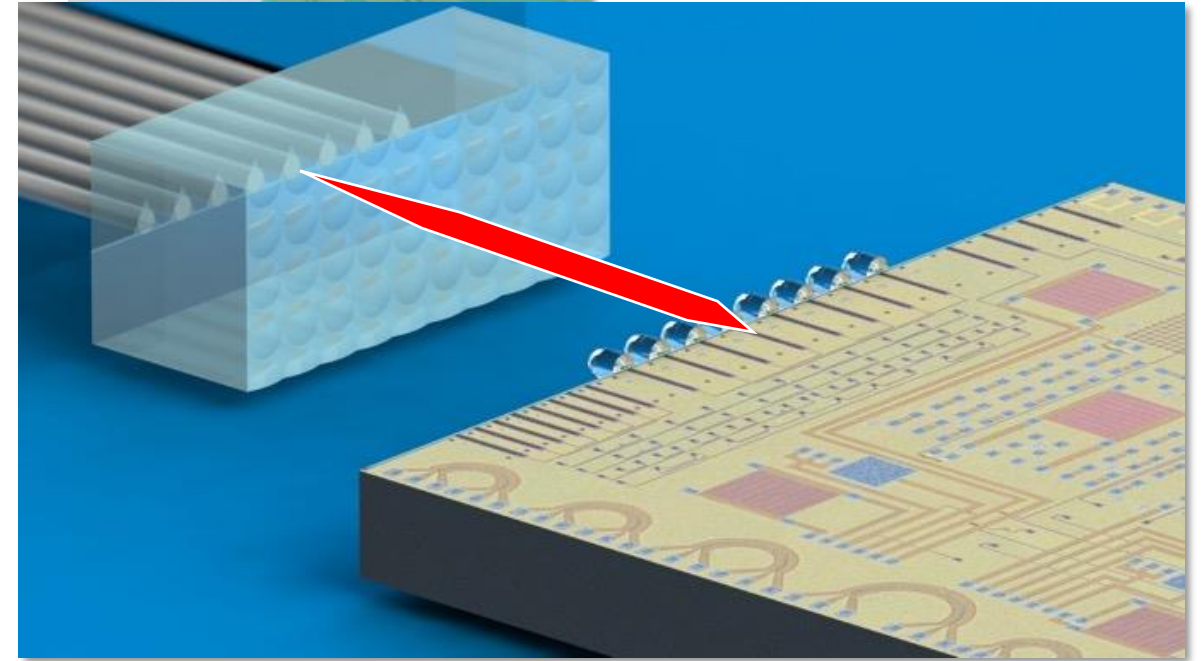
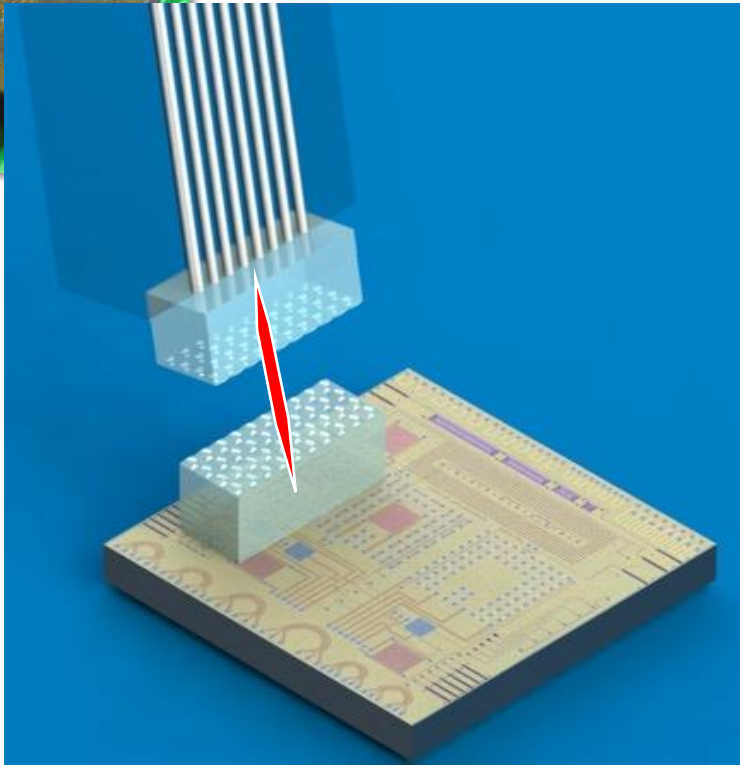


**Grating Couplers
(Fixed)**

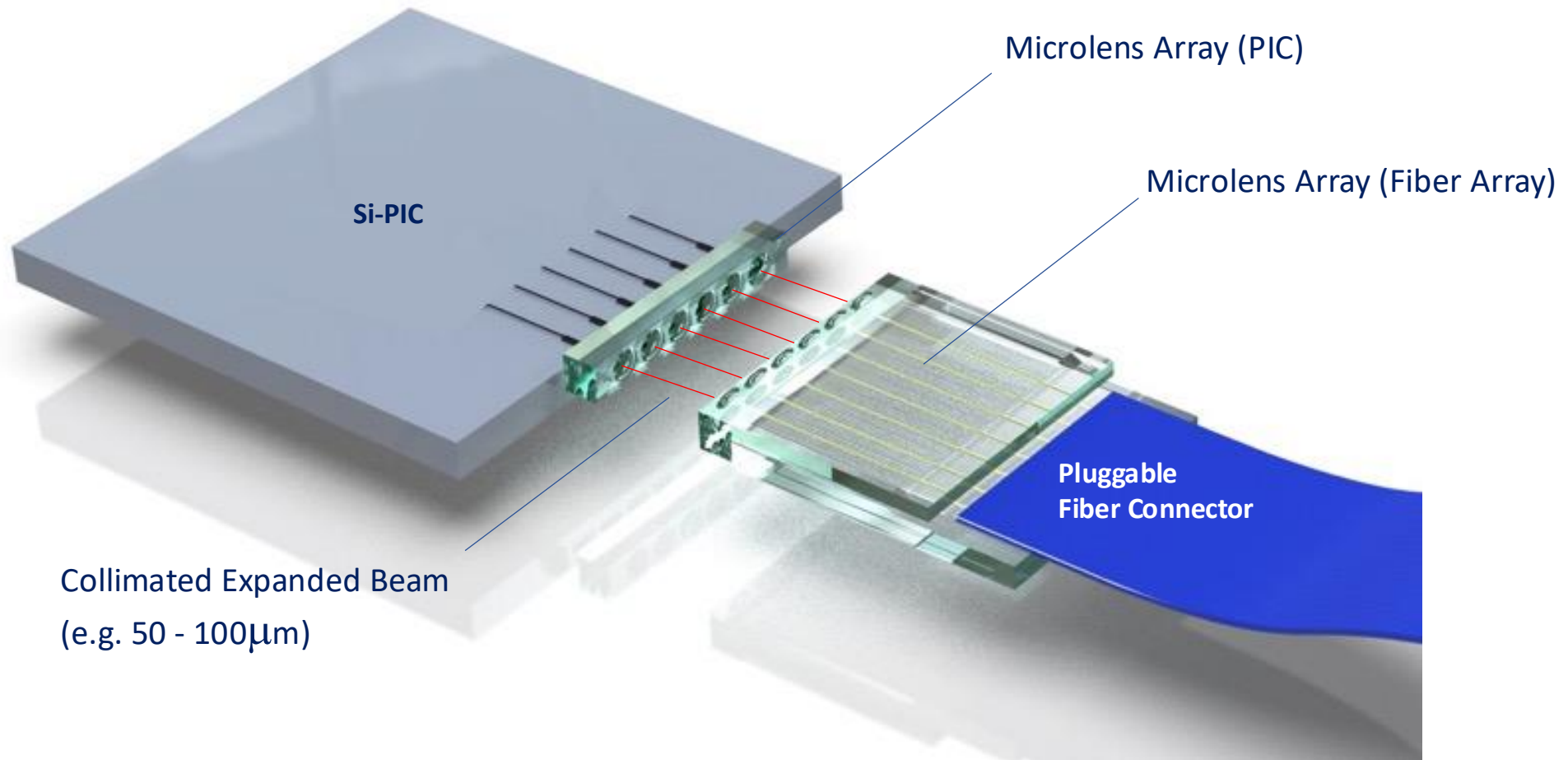


**Edge Couplers
(Fixed)**

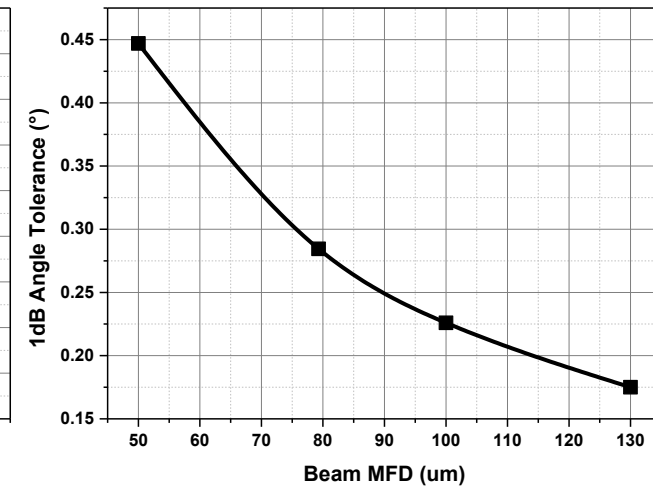
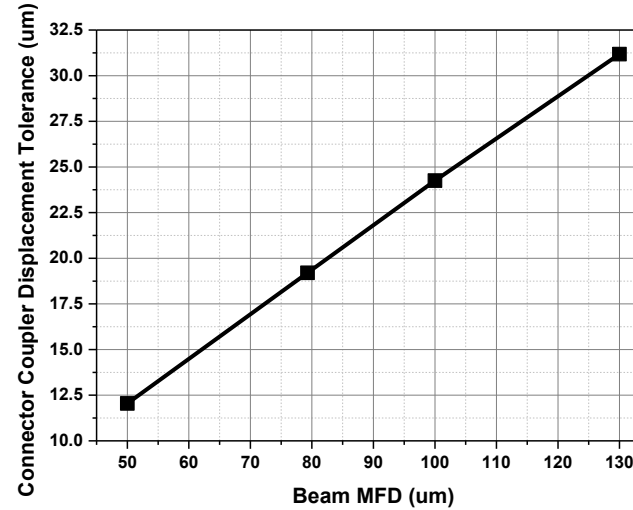
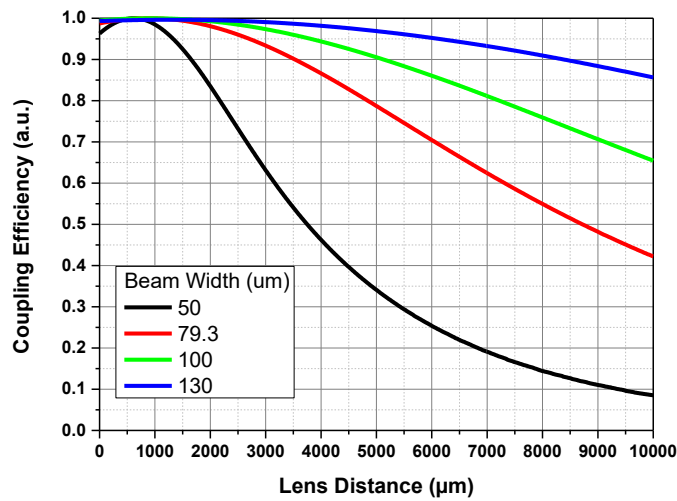
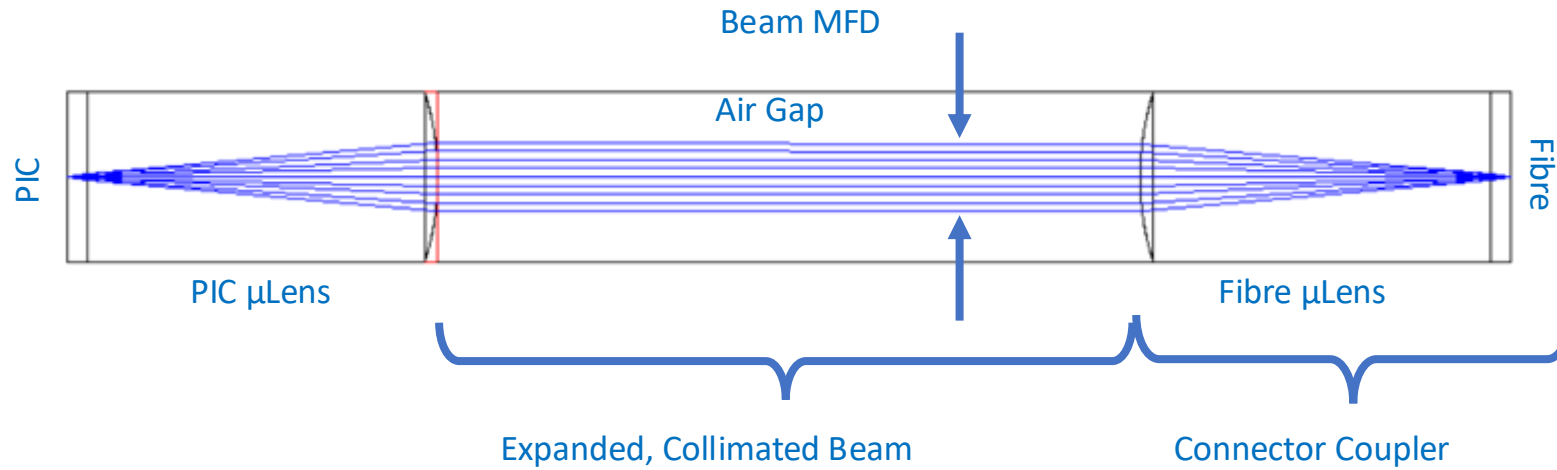
**Micro Optics
(Pluggable)**



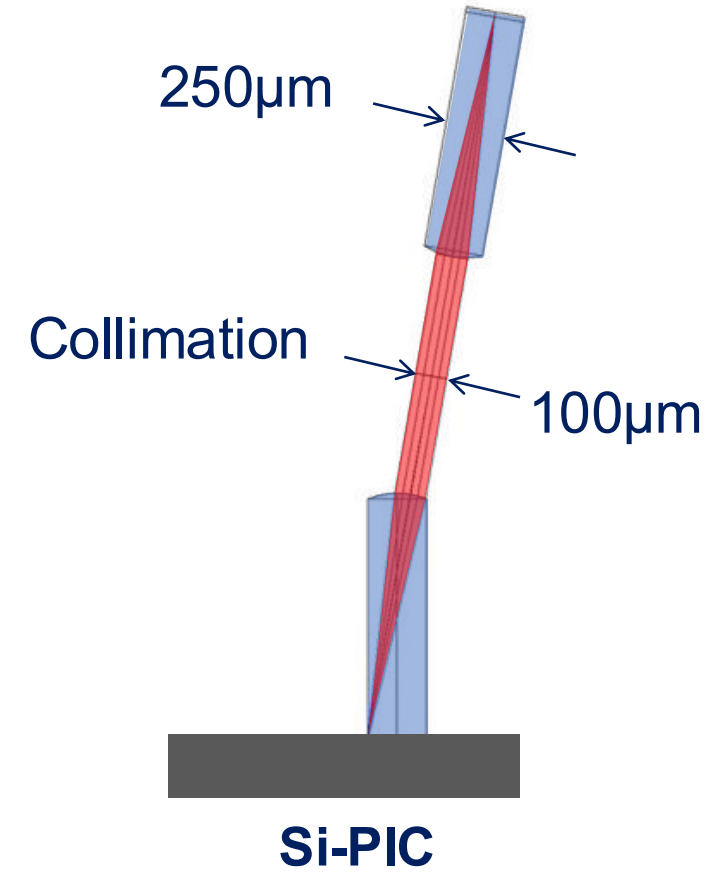
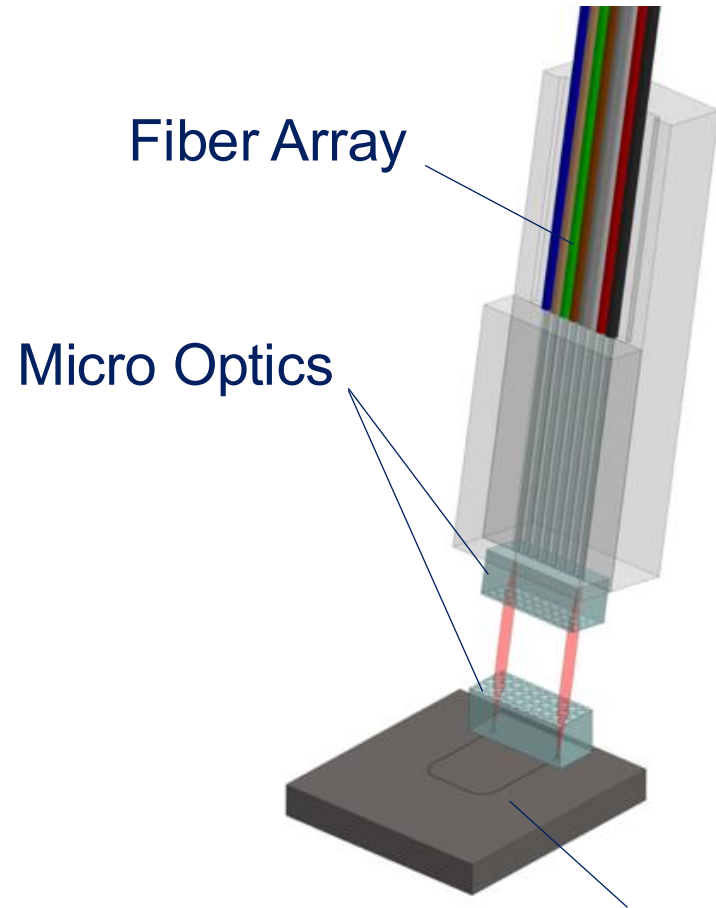
Micro Optic Packaging (expanded beam coupling)



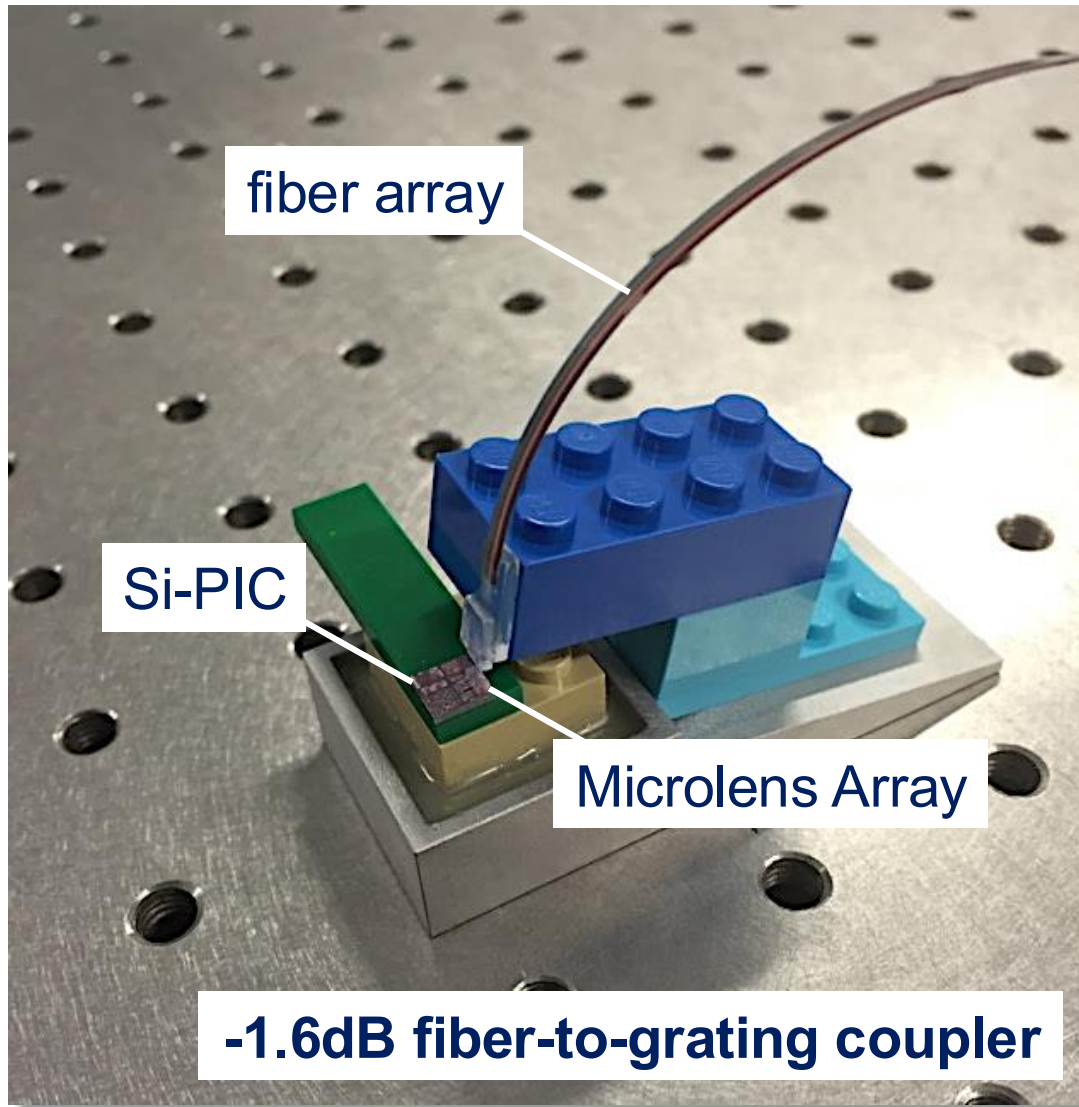
Micro Optic Packaging (expanded beam coupling)



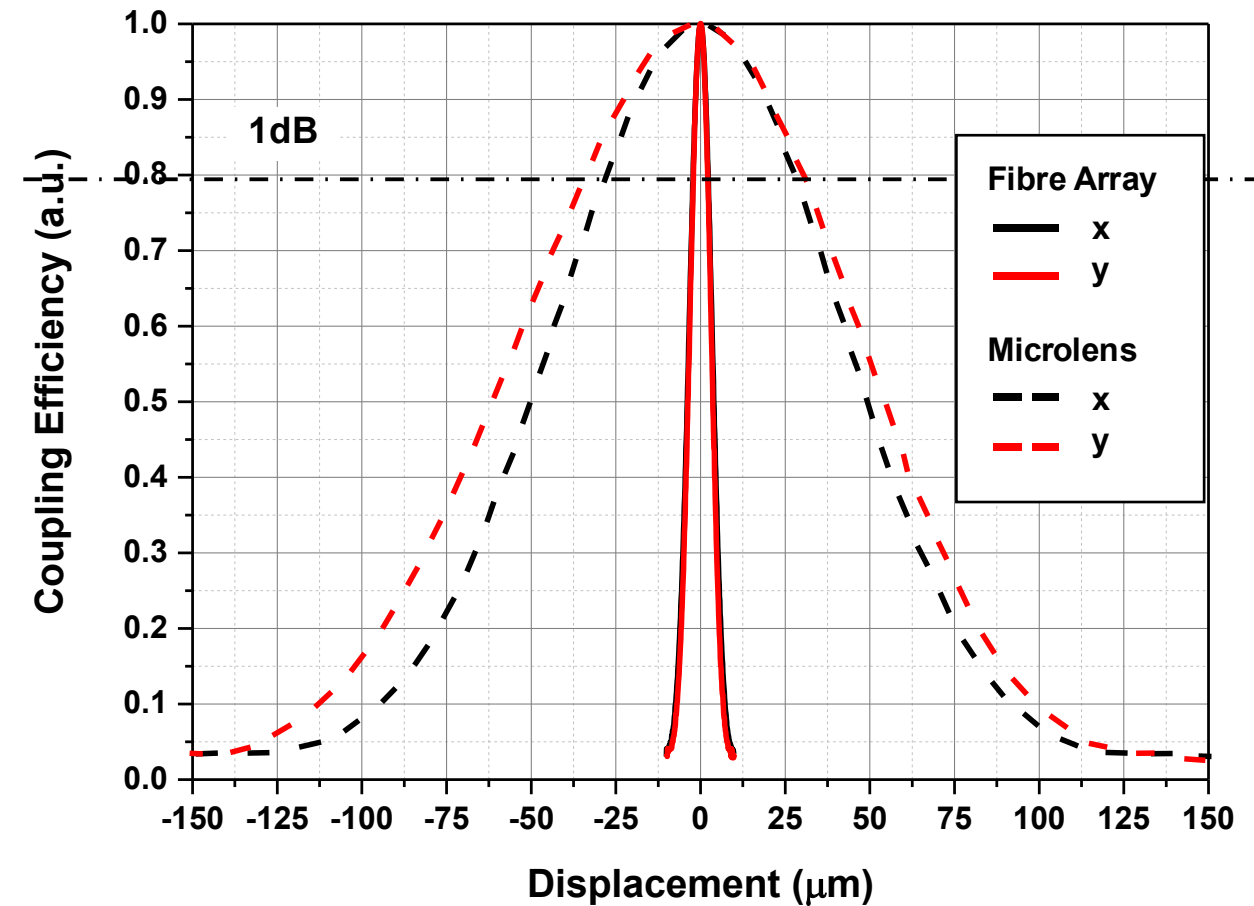
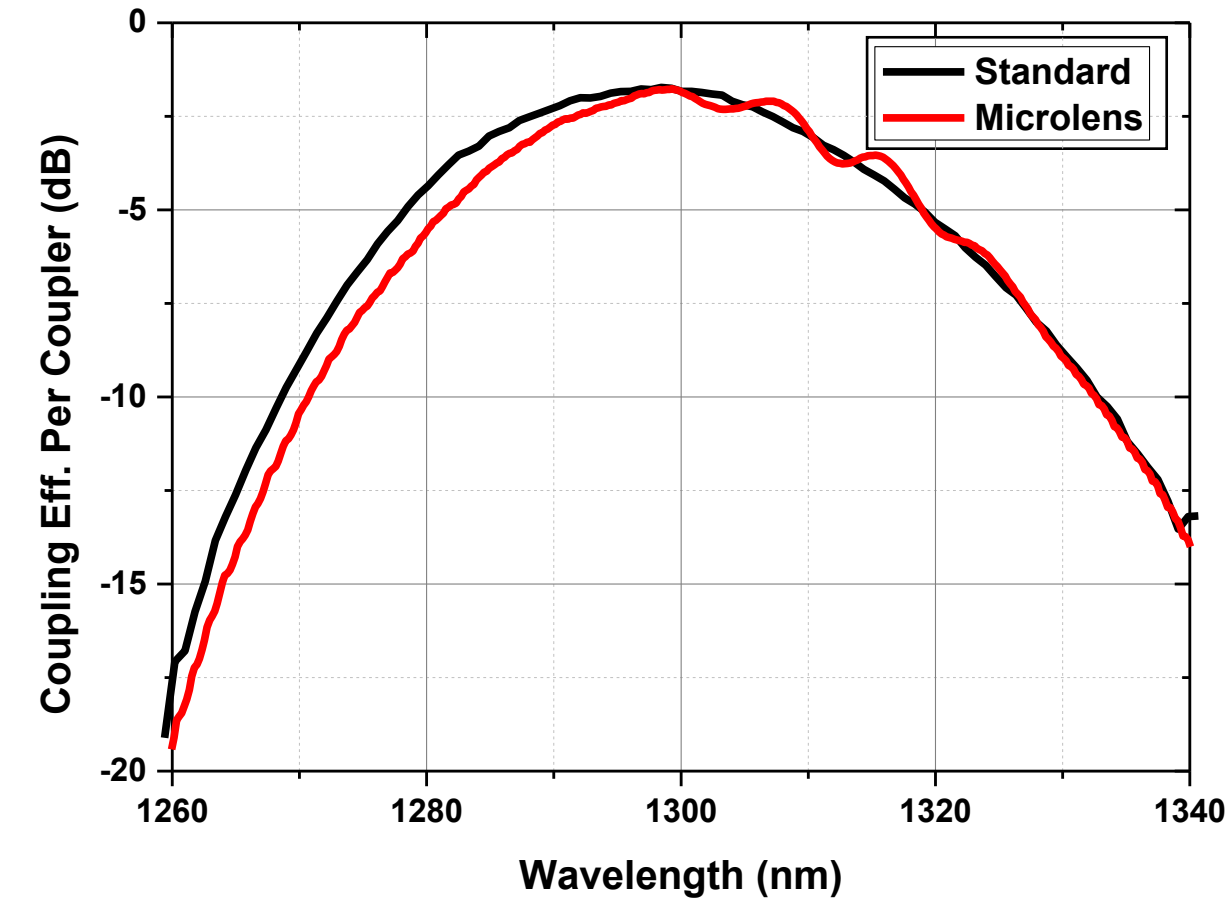
Micro Optic Packaging (expanded beam coupling)



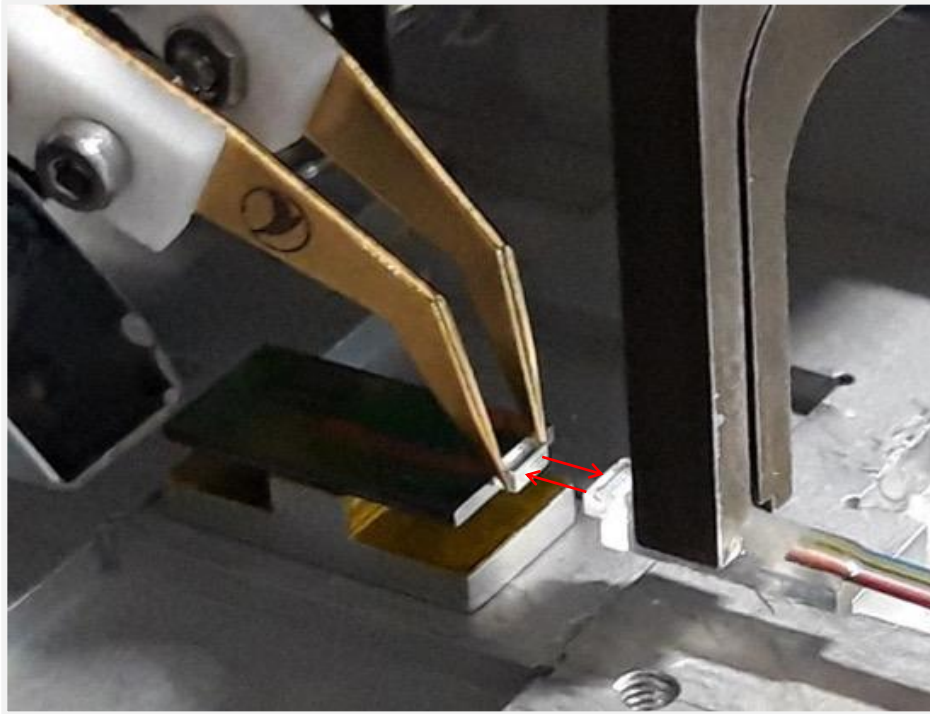
Micro Optic Packaging (expanded beam coupling)



Micro Optic Packaging (expanded beam coupling)

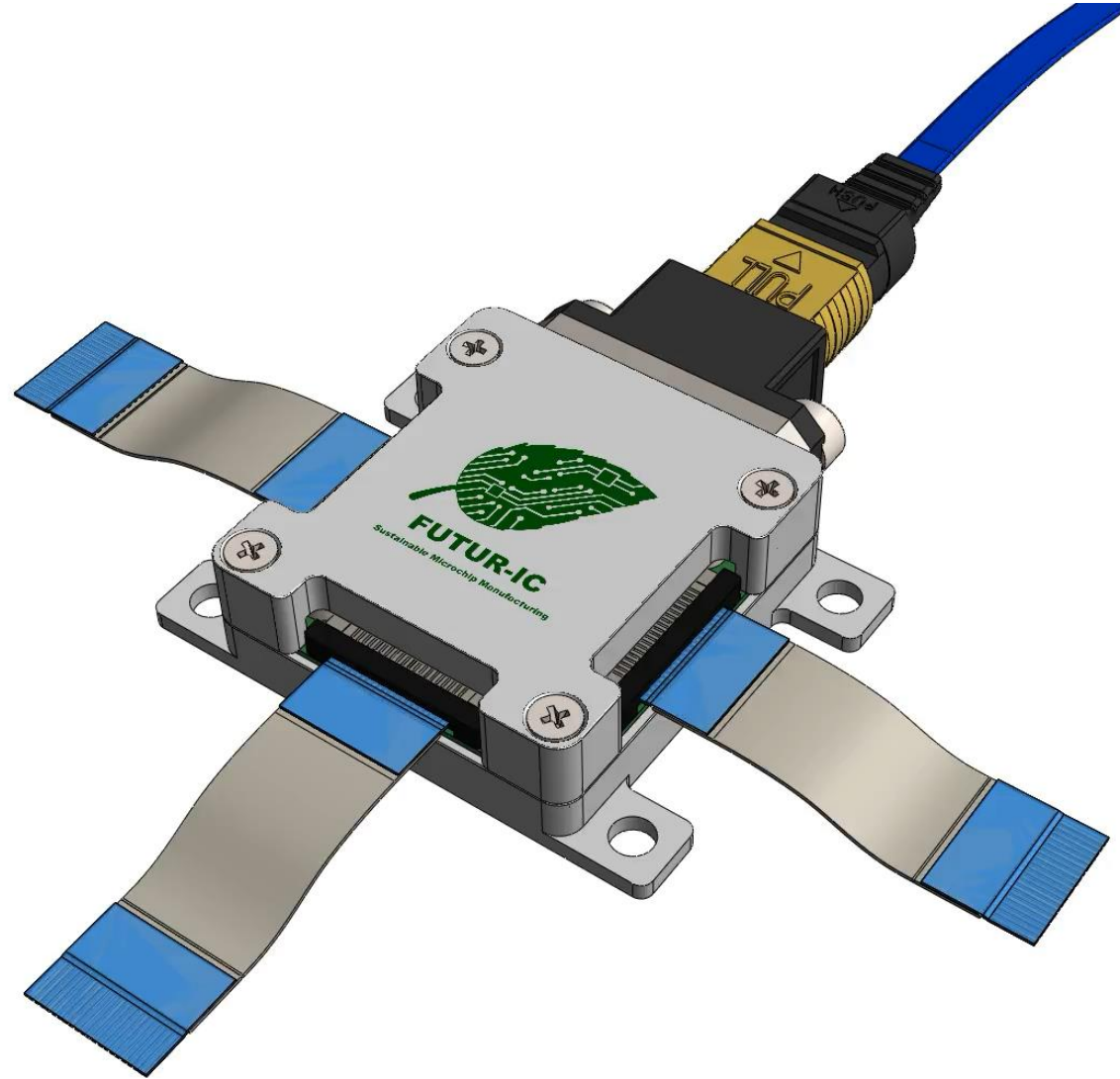


Micro Optic Packaging (expanded beam coupling)

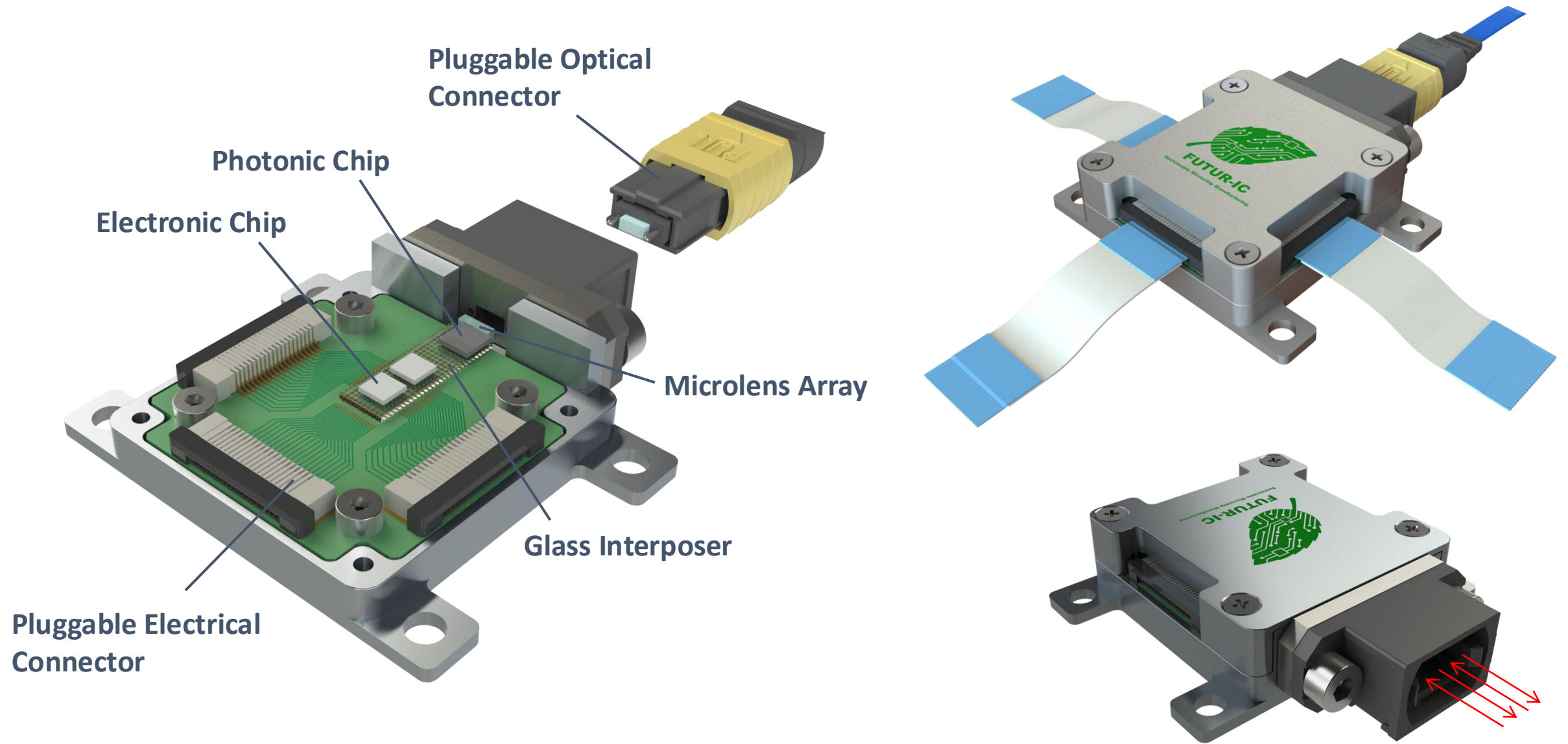


'Demonstration of Single-Mode Expanded Beam Connectorised Module for Photonic Integrated Circuits'
IEEE, Journal of Lightwave Technology,
February 2023.

Micro Optic Packaging (expanded beam coupling)



Micro Optic Packaging (expanded beam coupling)



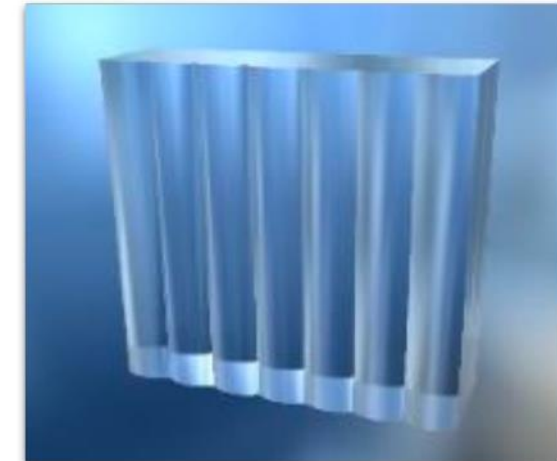
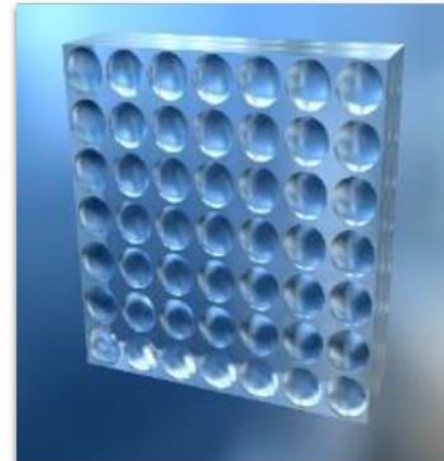
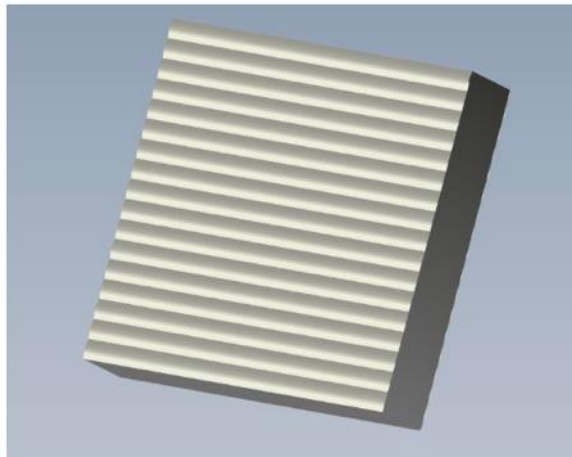
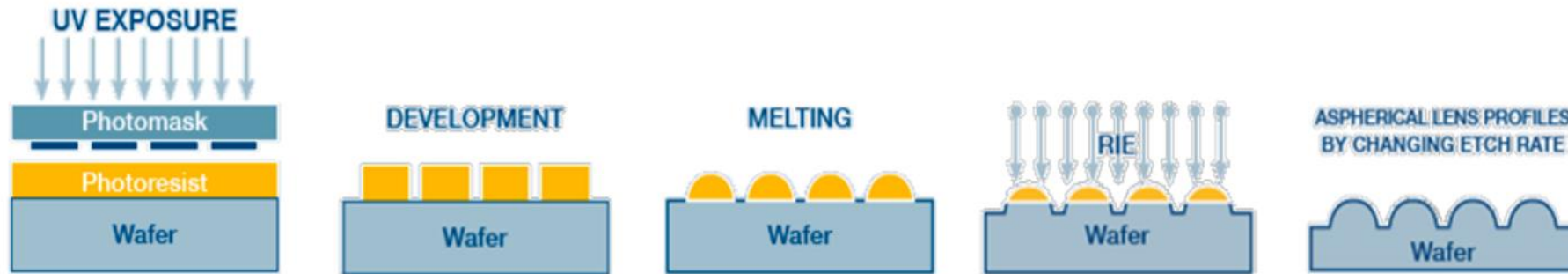
Micro Optic Packaging

Etched Monolithic Micro-Optics



FOCUSLIGHT
Never stop exploring

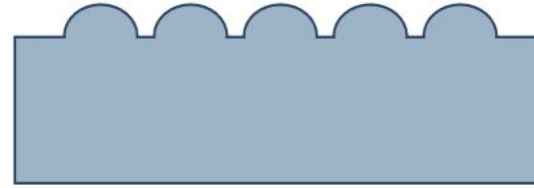
- Etched & monolithic
- For high optical power, harsh environments, high performance applications
- Materials: Fused silica and silicon, 200 mm wafers



Micro Optic Packaging

Protruding Lenses

- Most economic options
- Single- and double-side



Recessed Lenses

- For stacking with other micro-optical elements



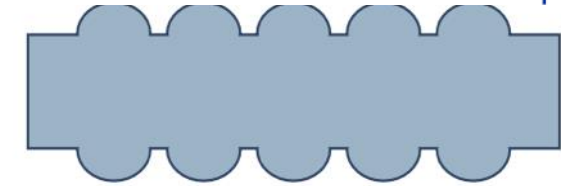
Advanced Recessed Lenses

- Fiducials and backside cavity
- Best for large volume packaging



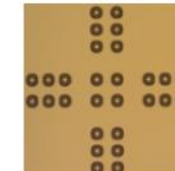
FOCUSLIGHT

Never stop exploring



**And the combination
of all these options!**

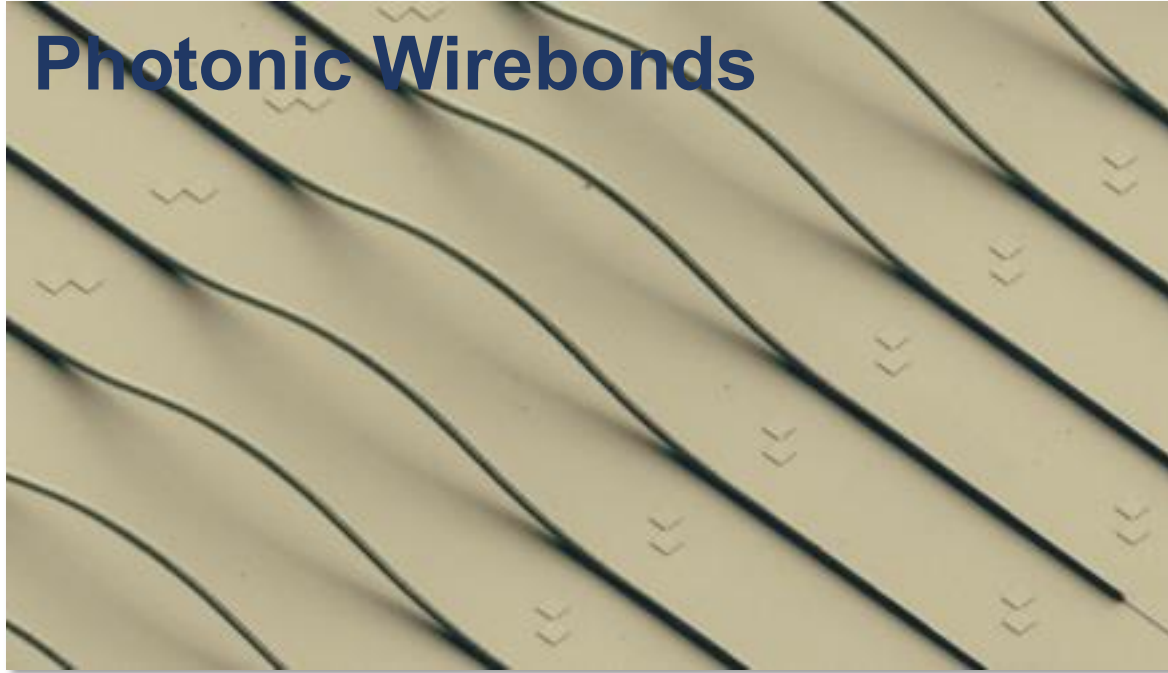
Fiducials for vision systems



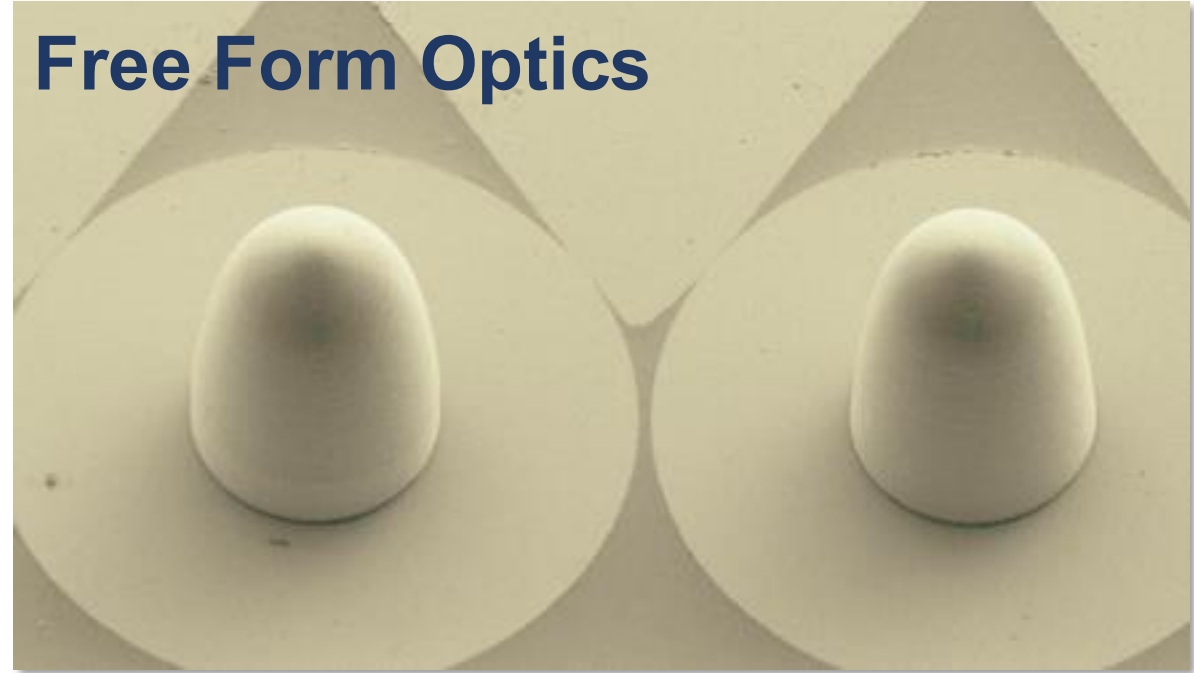
trenches & cavities

Micro Optic Packaging (3D Printing)

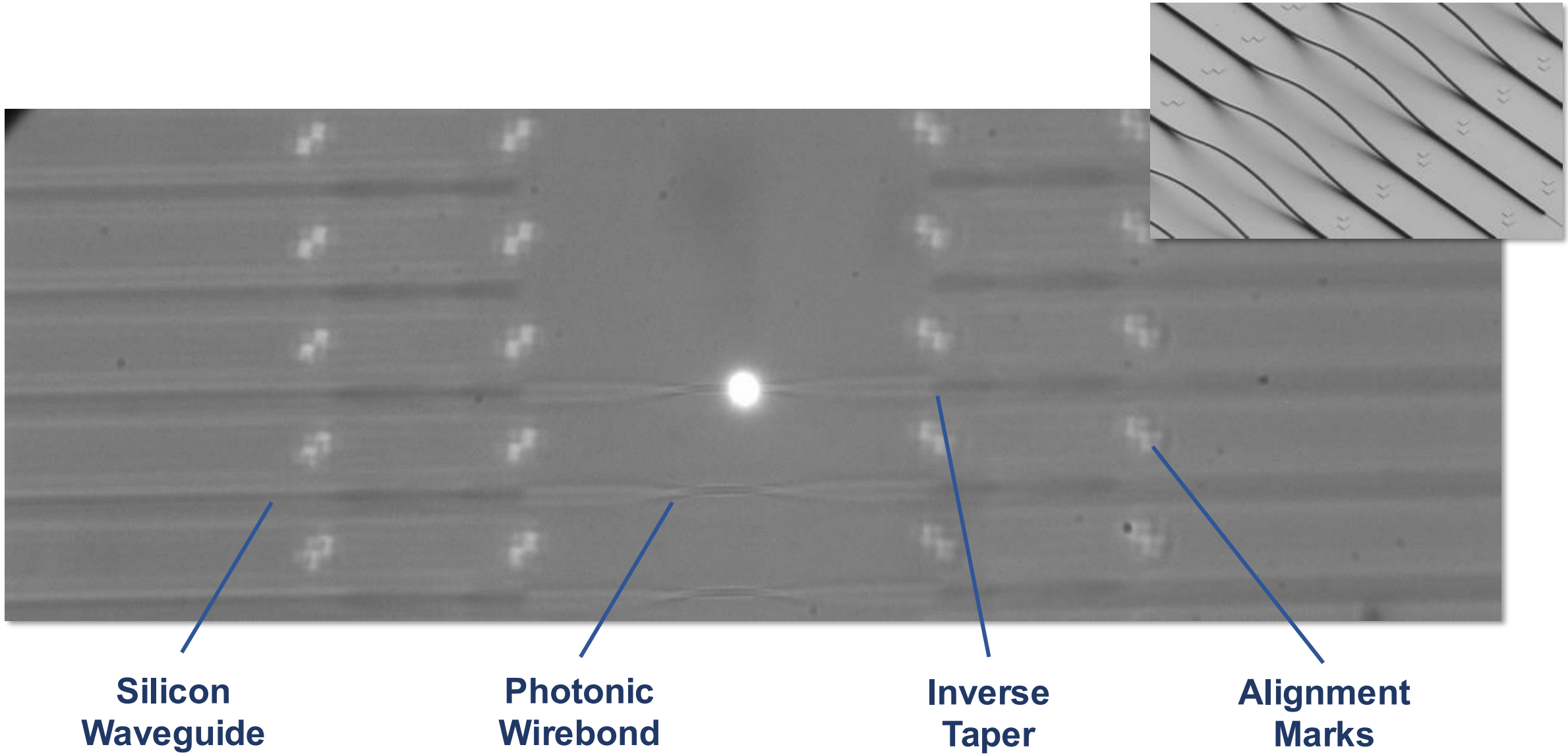
Photonic Wirebonds



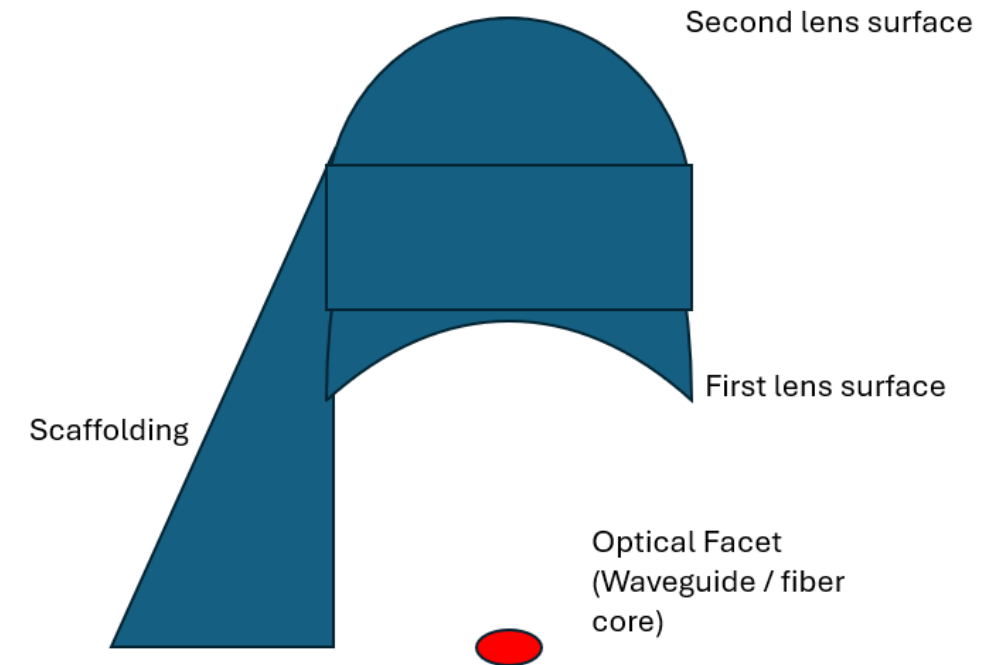
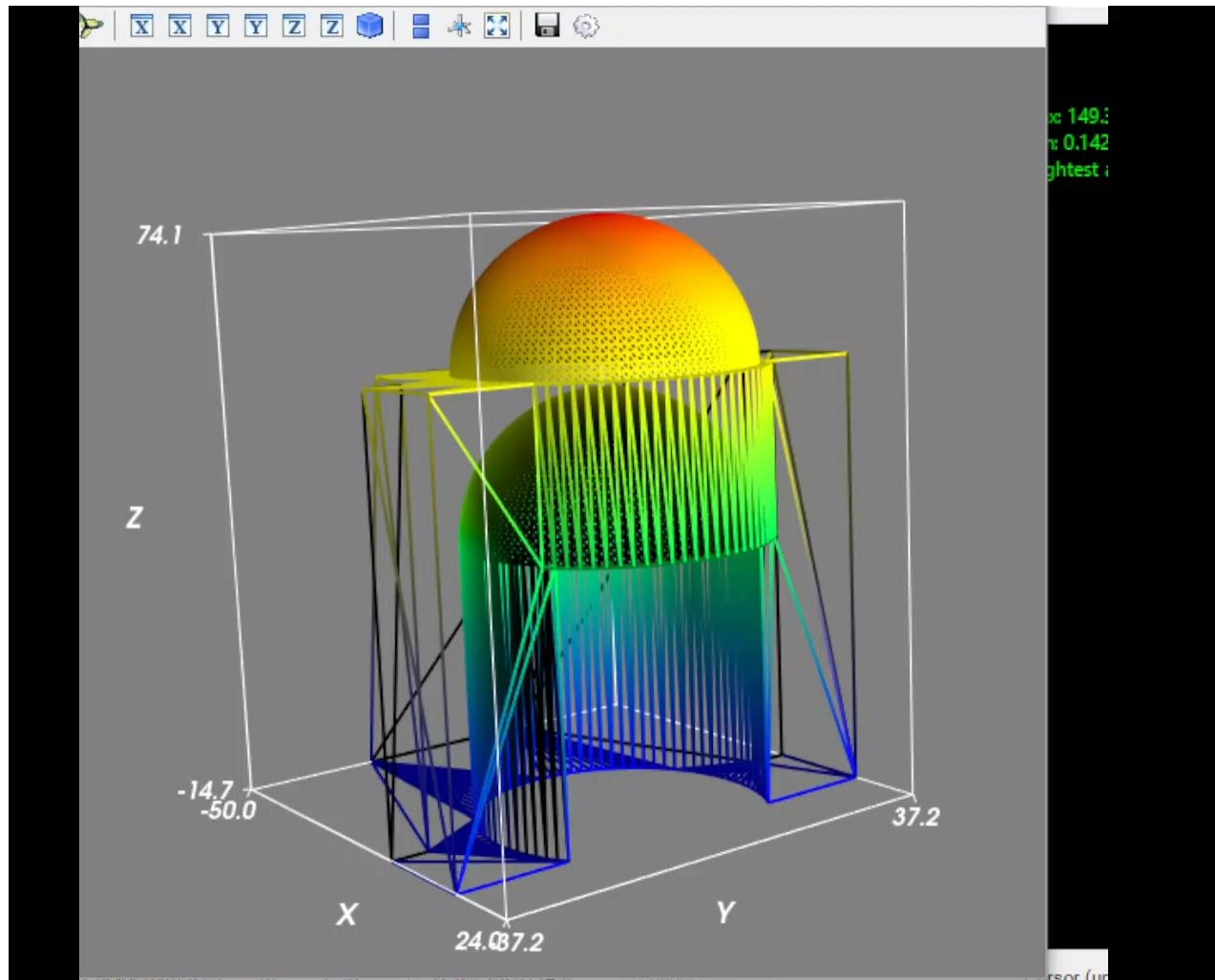
Free Form Optics



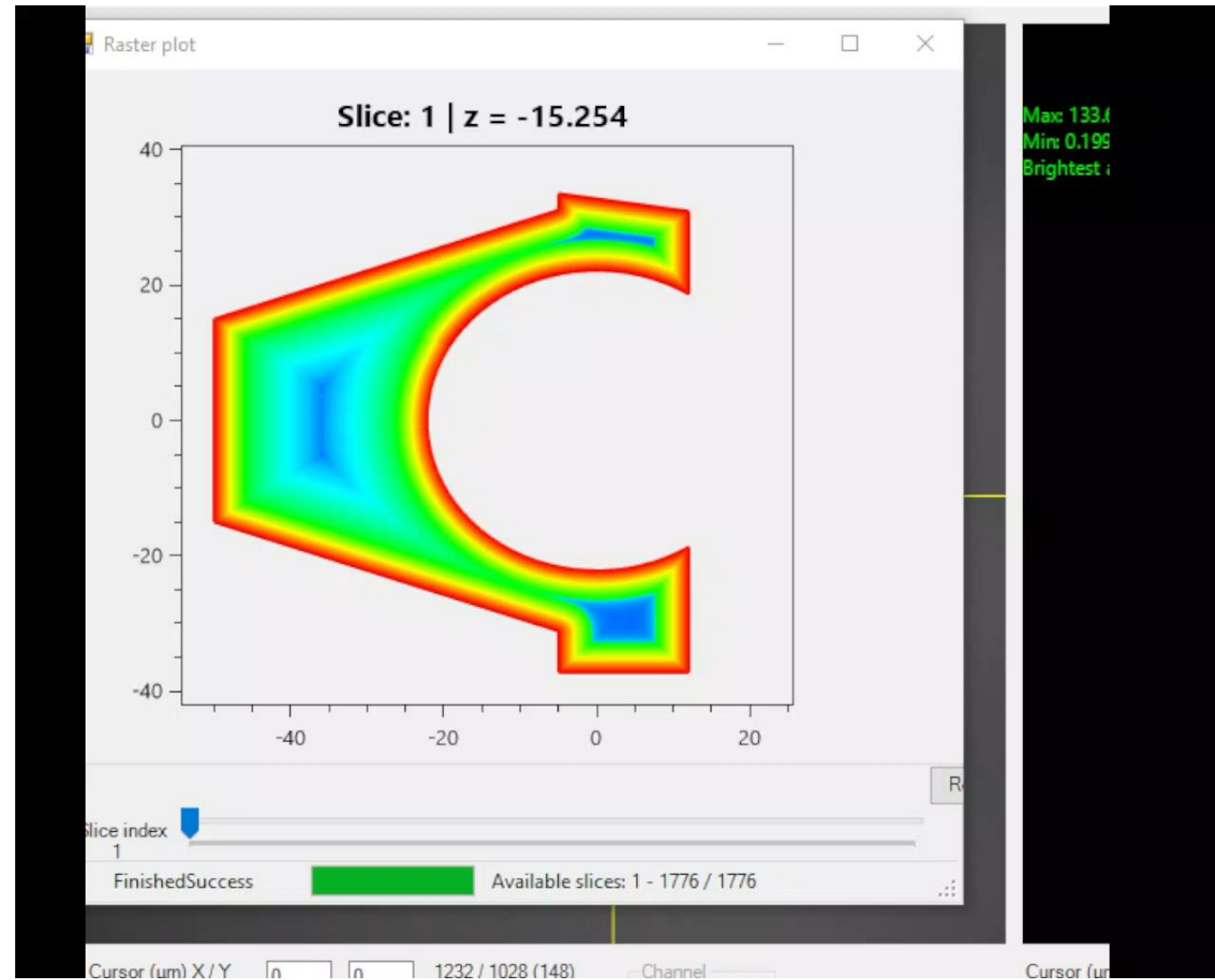
Micro Optic Packaging (3D Printing)



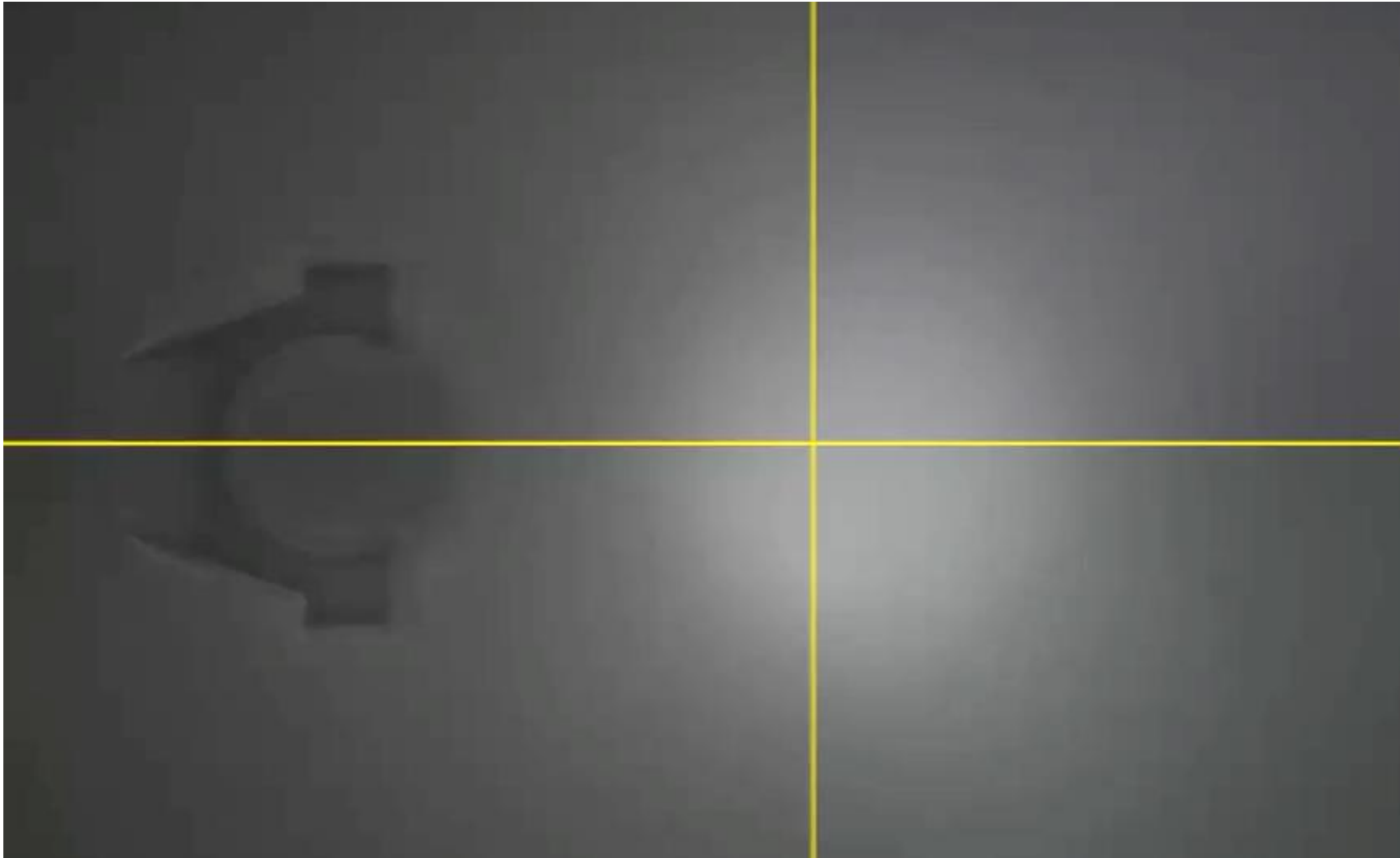
Micro Optic Packaging (3D Printing)



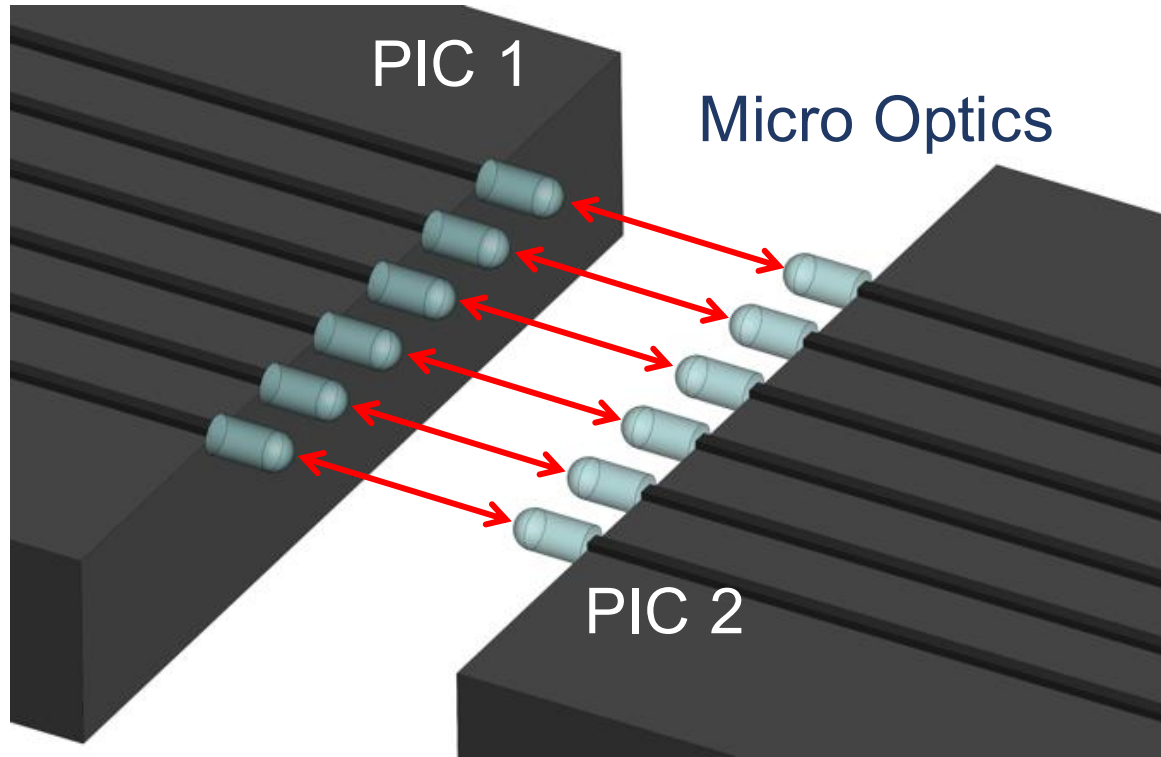
Micro Optic Packaging (3D Printing)



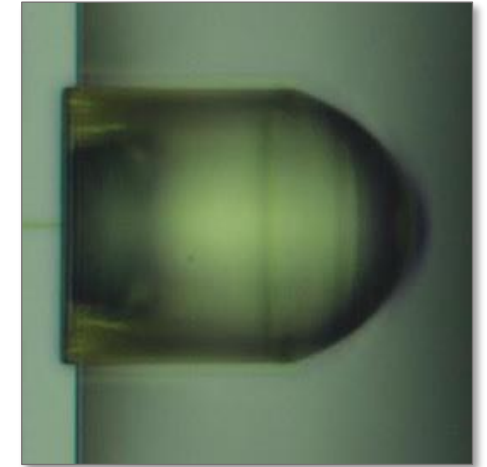
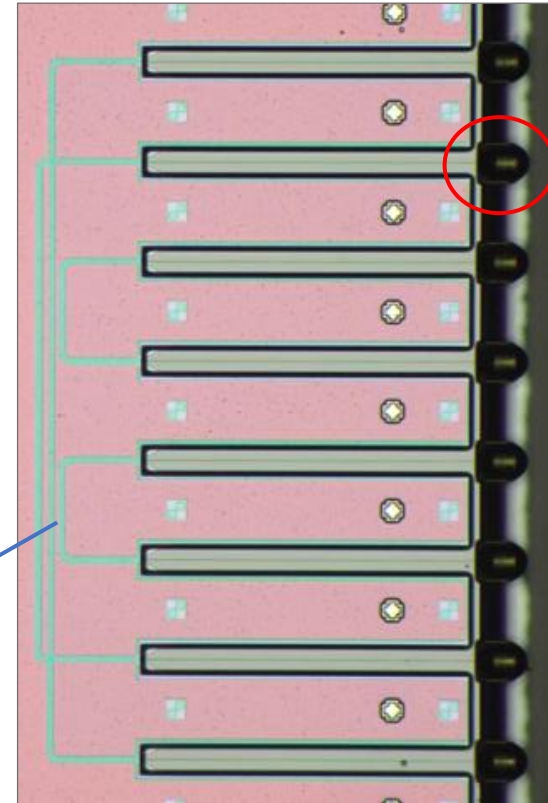
Micro Optic Packaging (3D Printing)



Micro Optic Packaging (3D Printing)



Silicon Photonic Device
(edge coupling)

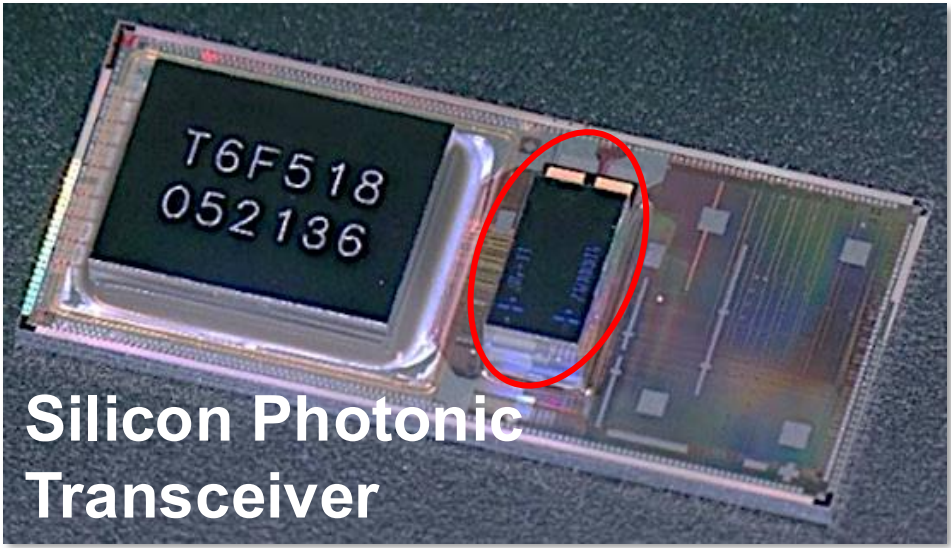
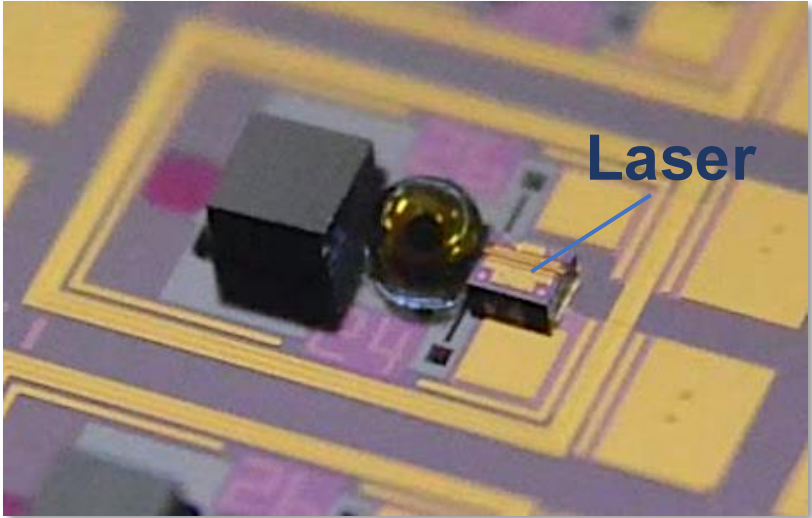
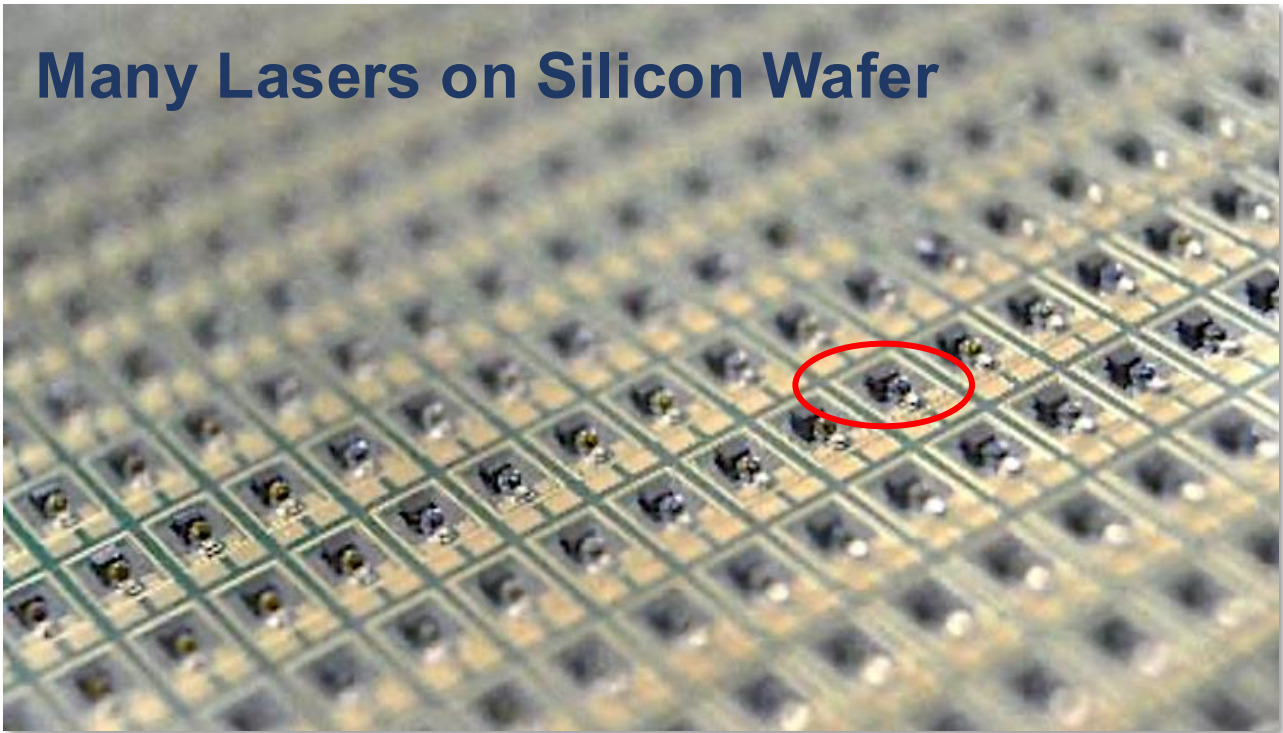


Expanded Beam
(25 μ m MFD)

PIC to Fiber Array
(1.9dB)

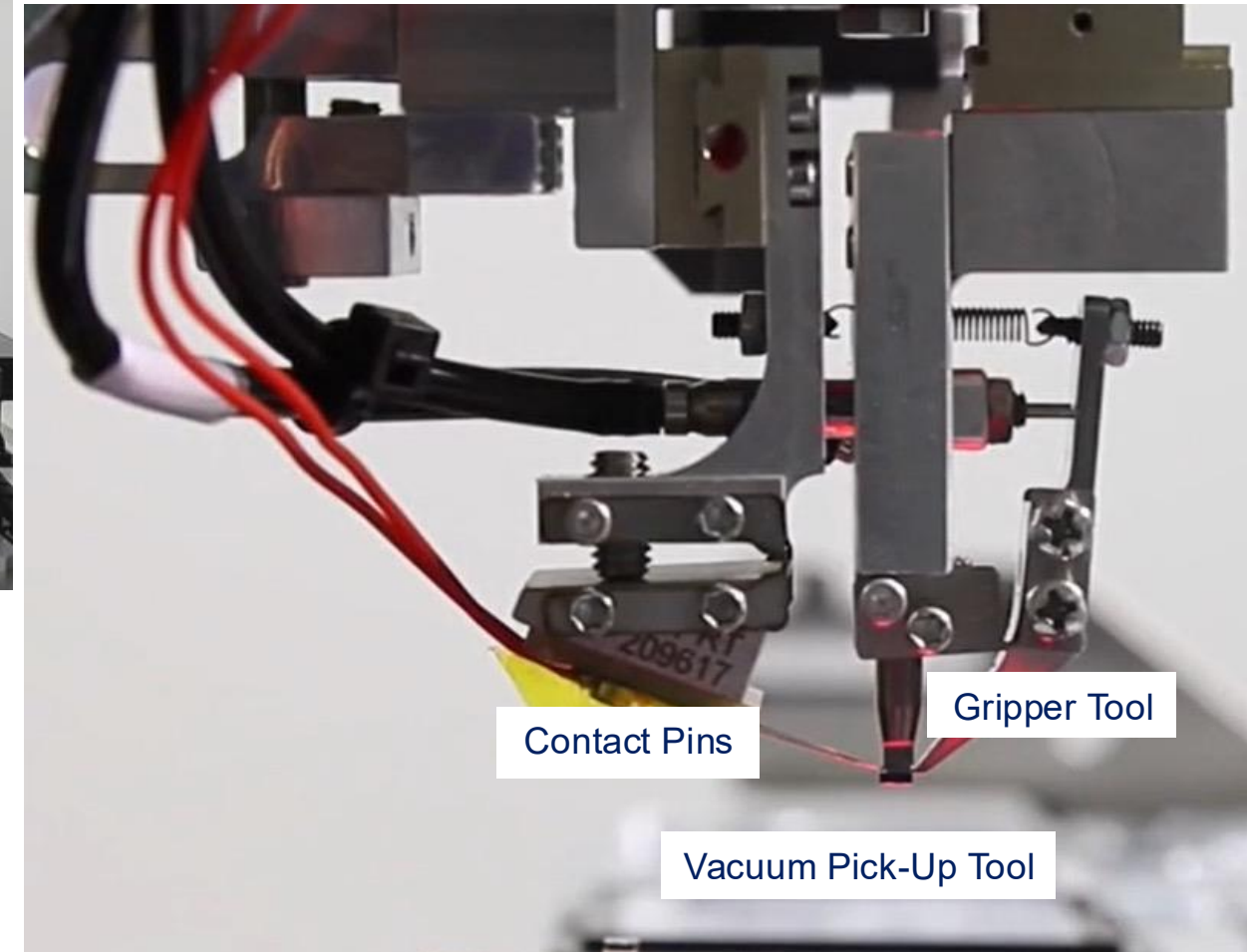
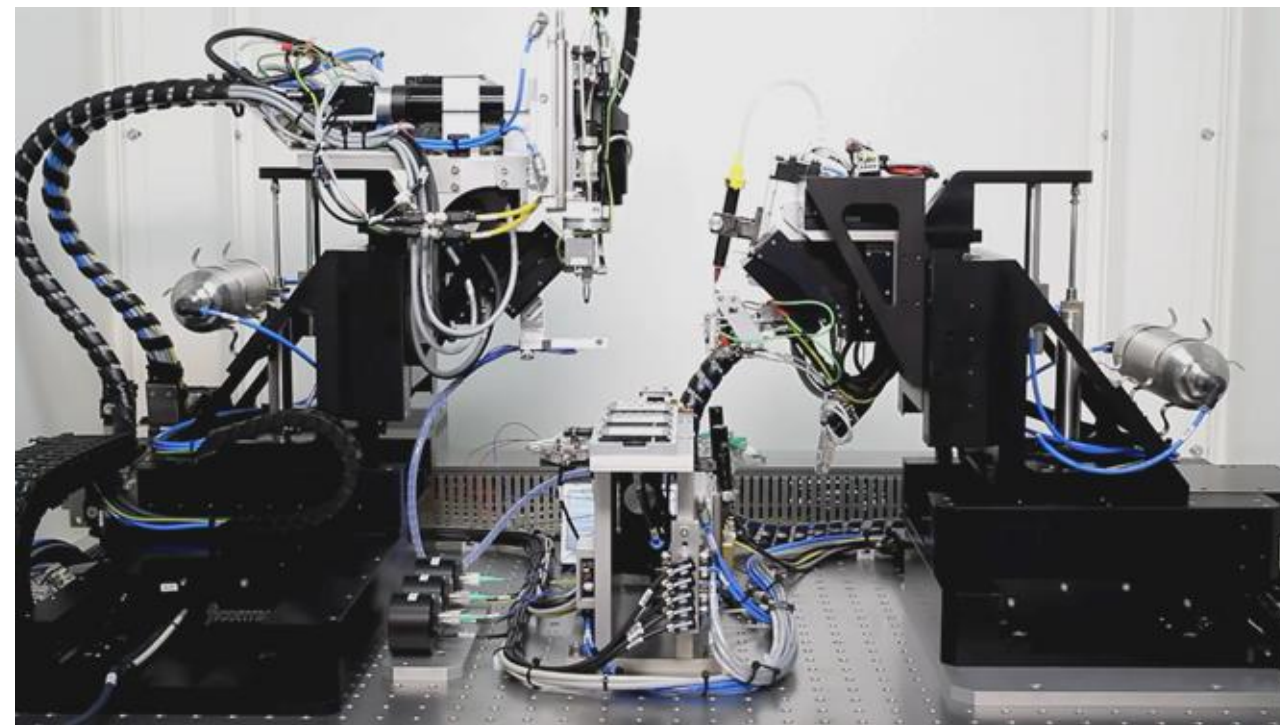
Active Device Integration (hybrid laser integration)

Many Lasers on Silicon Wafer



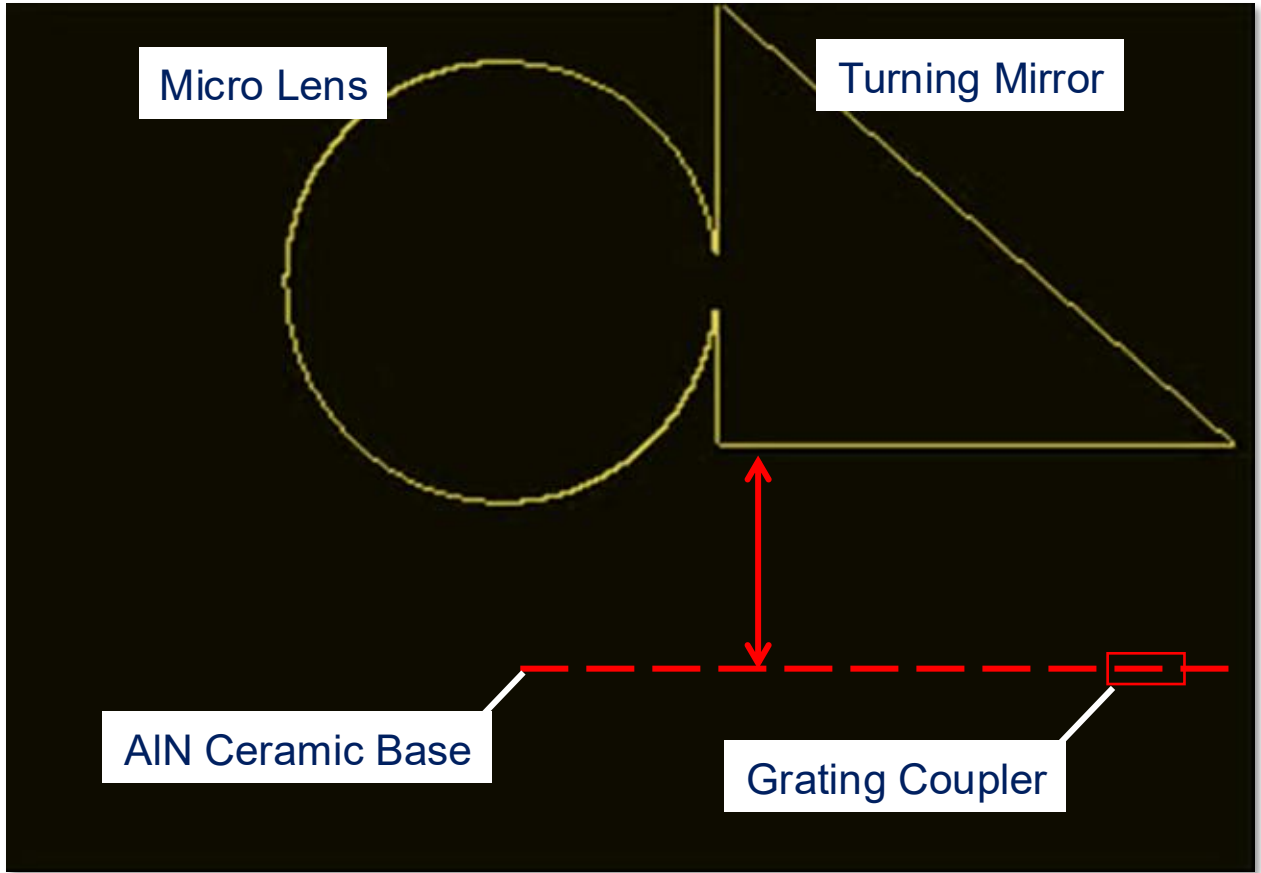
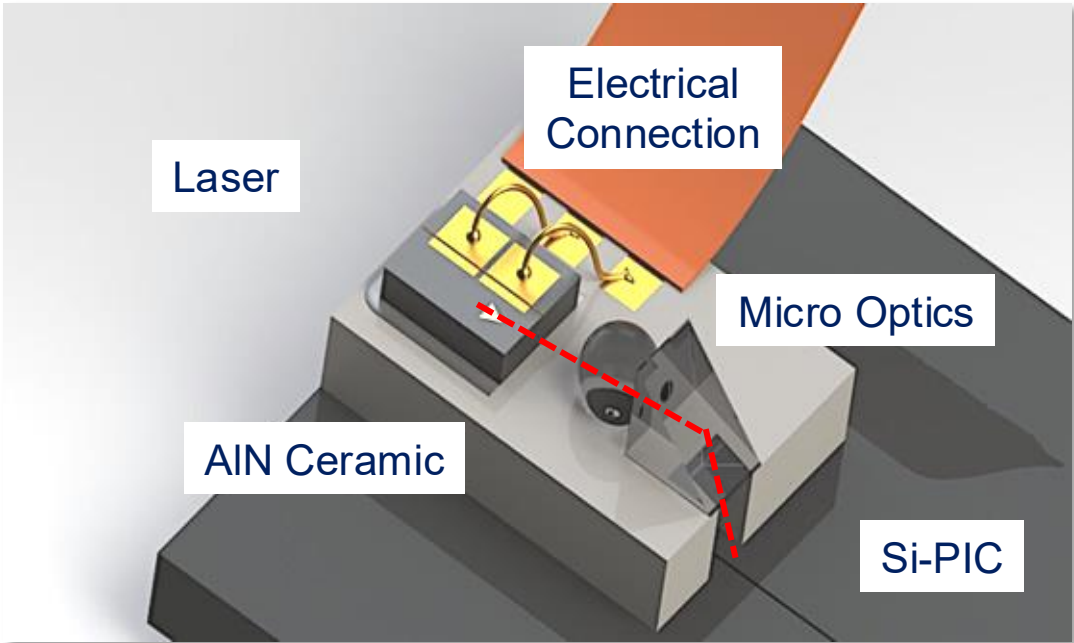
Silicon Photonic Transceiver

Active Device Integration (hybrid laser integration)



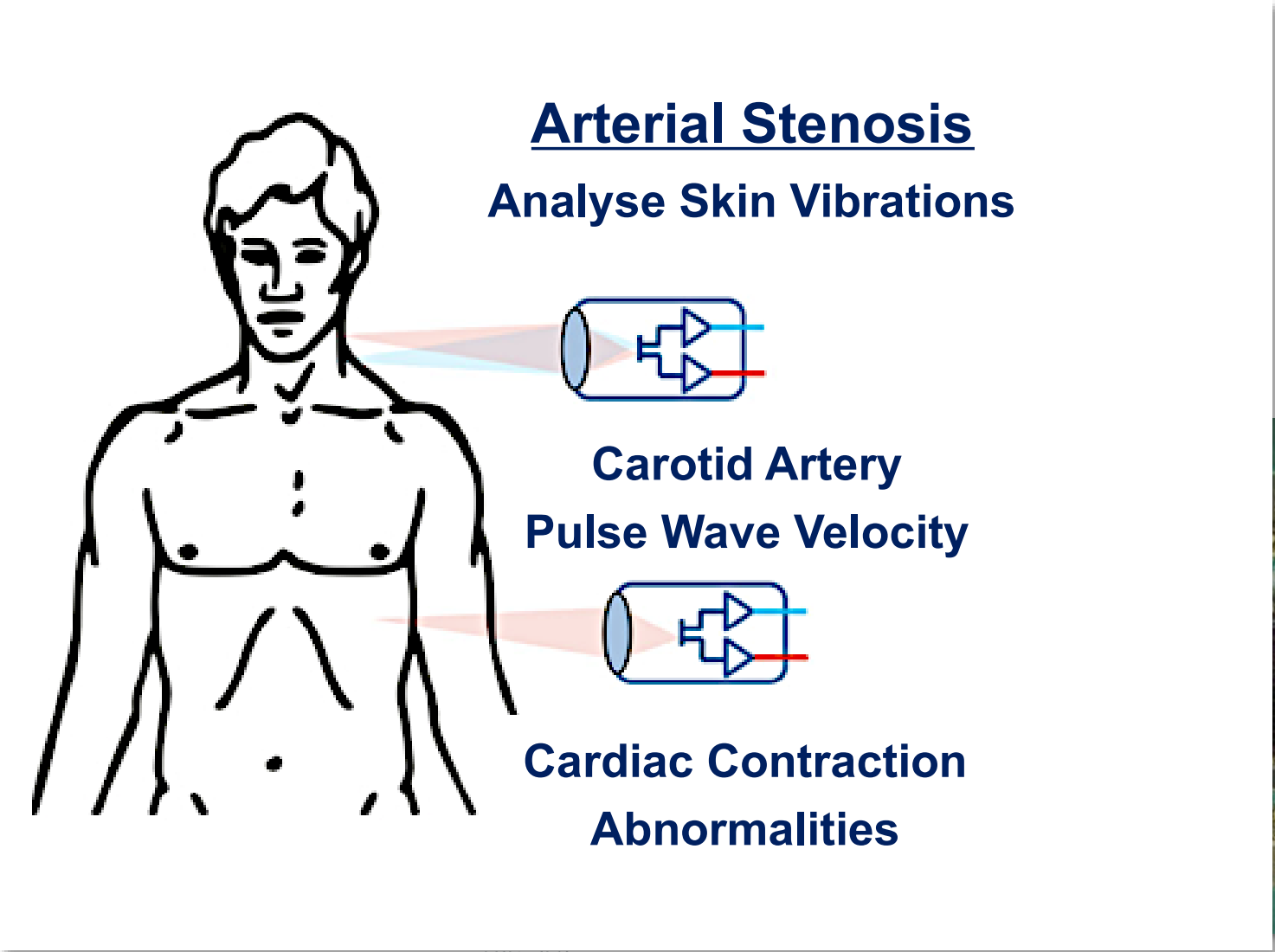
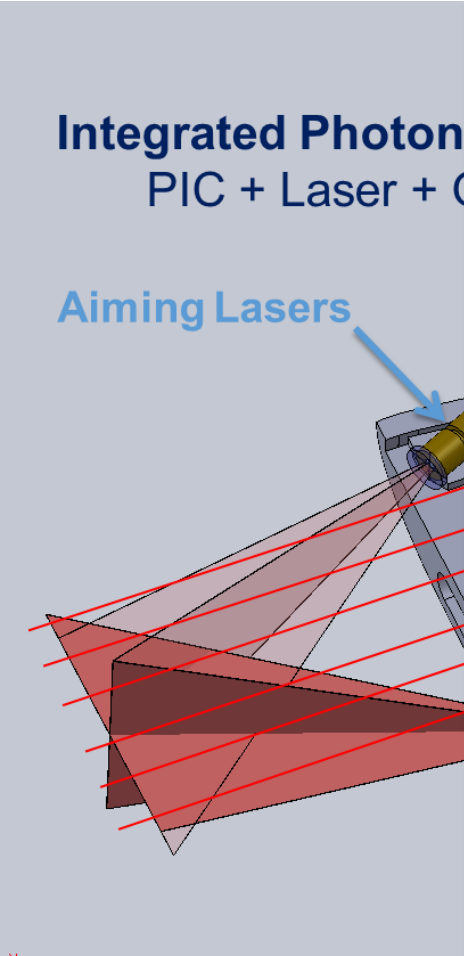
Active Device Integration (hybrid laser integration)

Device & Package Simulation (Hybrid Laser Integration)

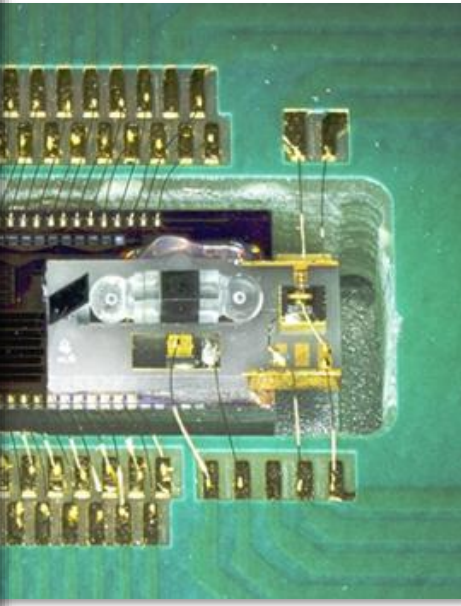


- 50% Power Transfer to Grating

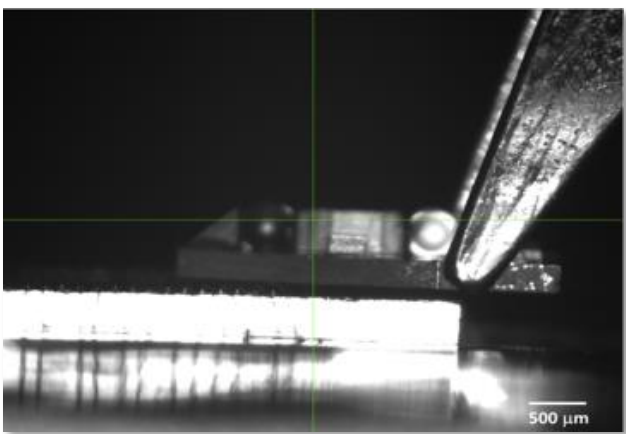
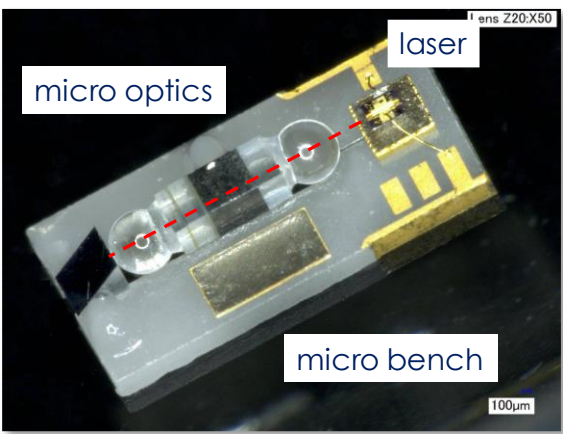
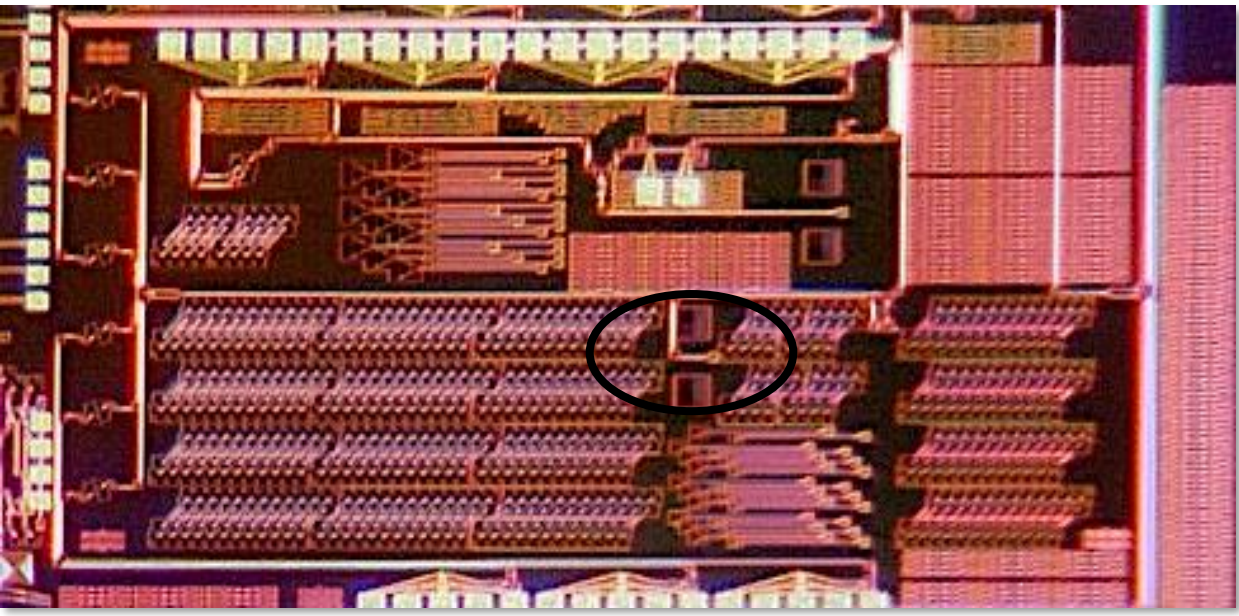
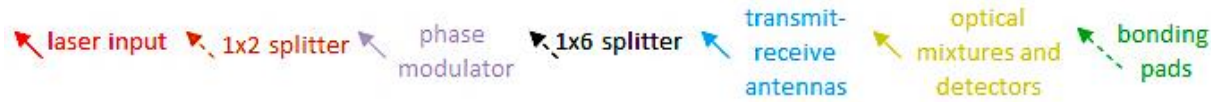
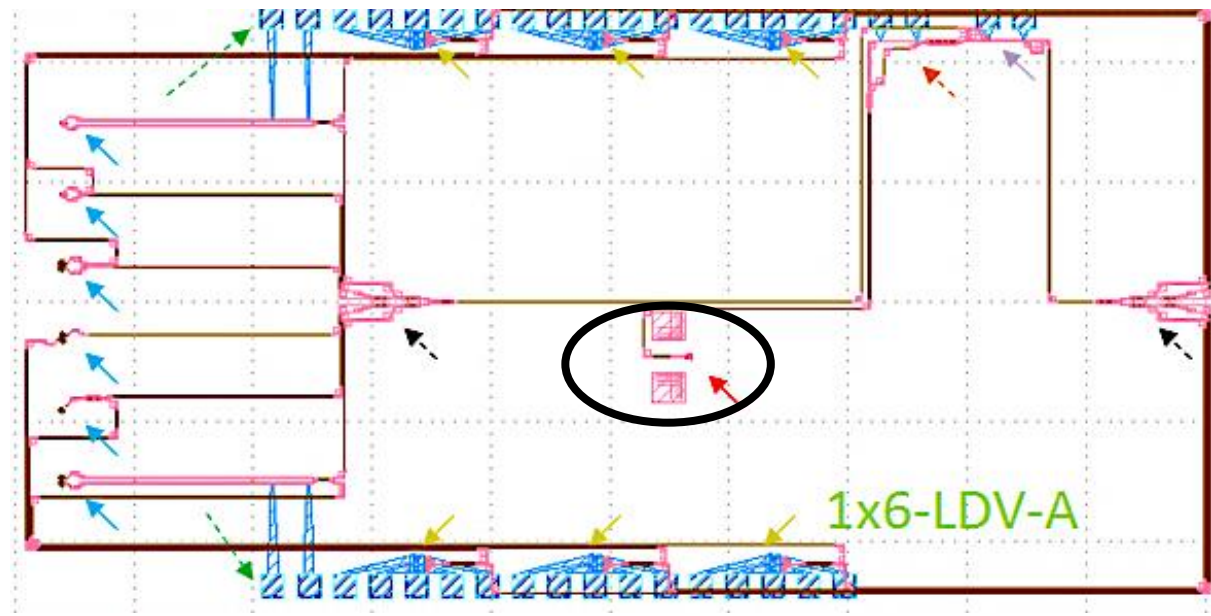
Active Device Integration (hybrid laser integration)



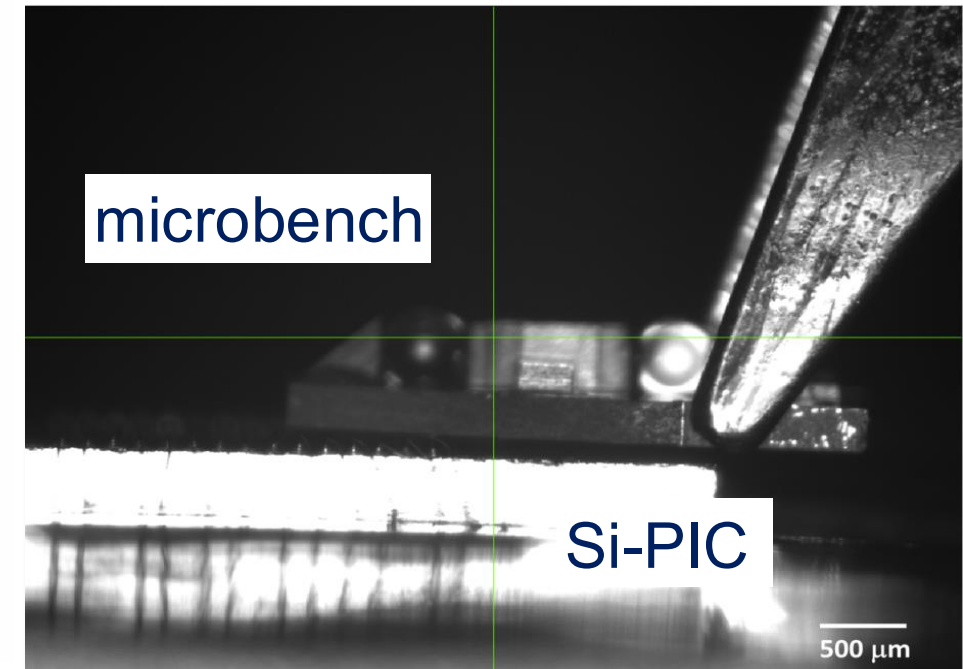
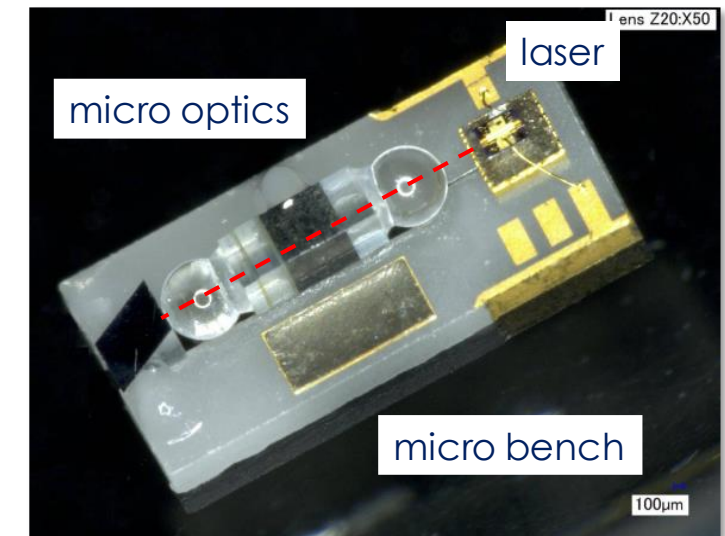
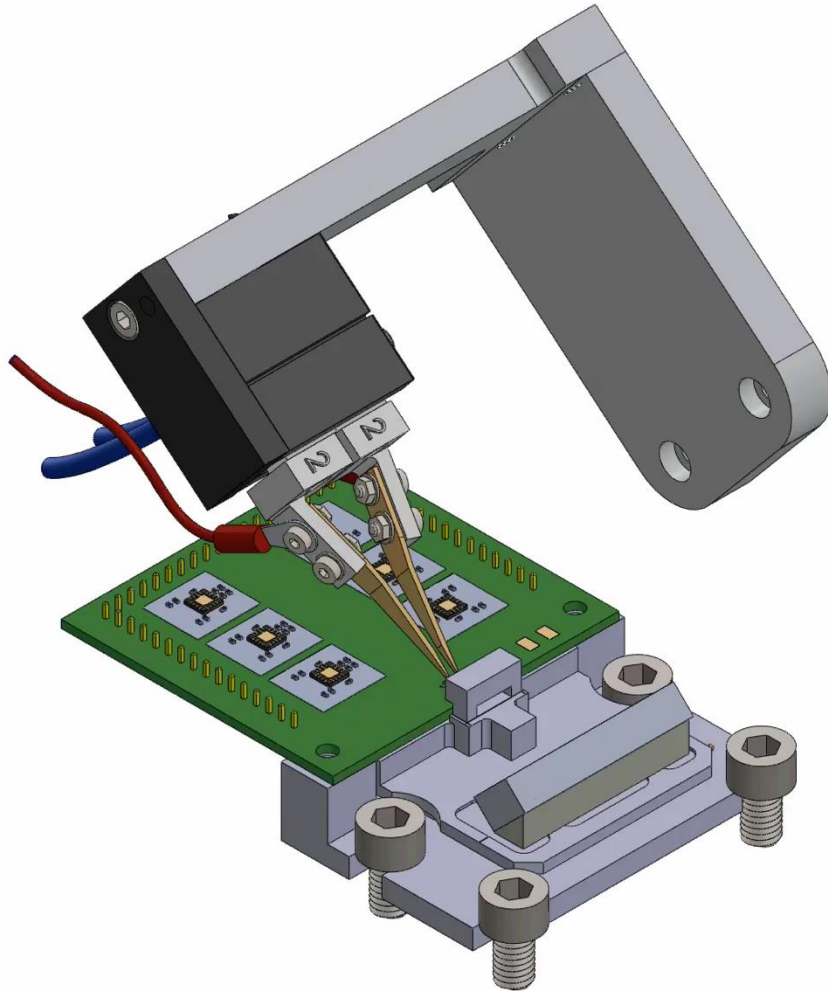
Laser on Si-PIC



Active Device Integration (hybrid laser integration)



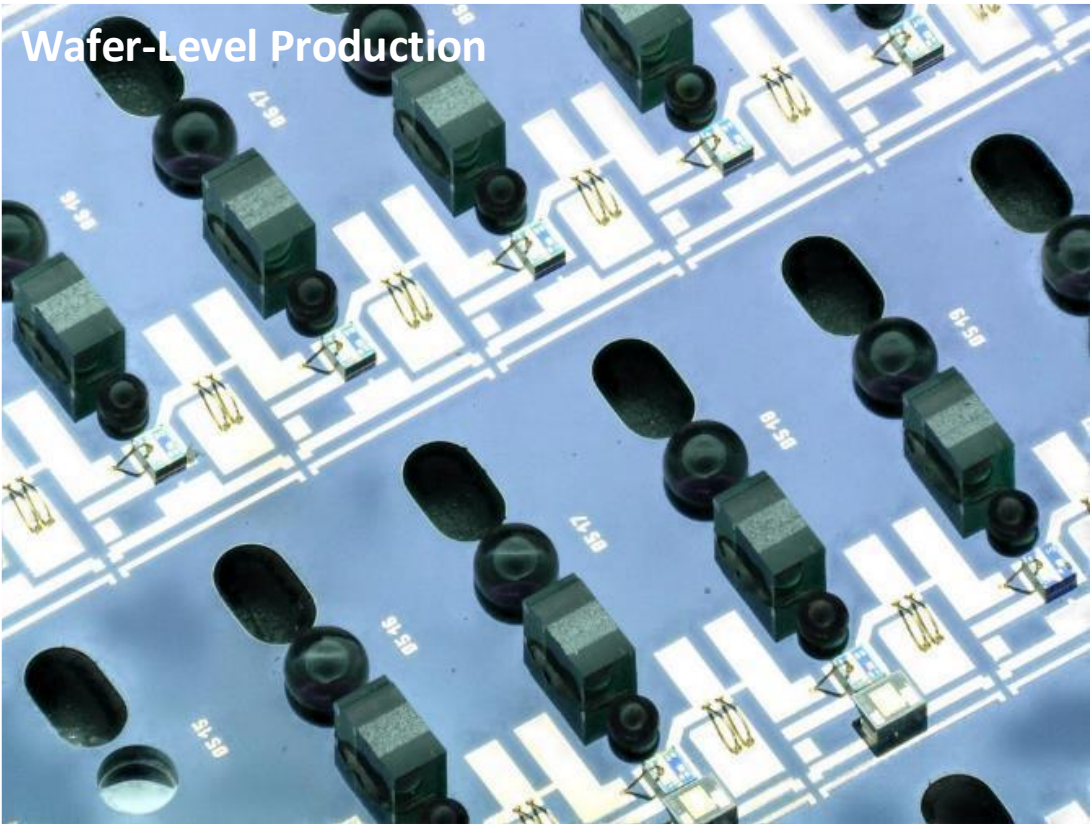
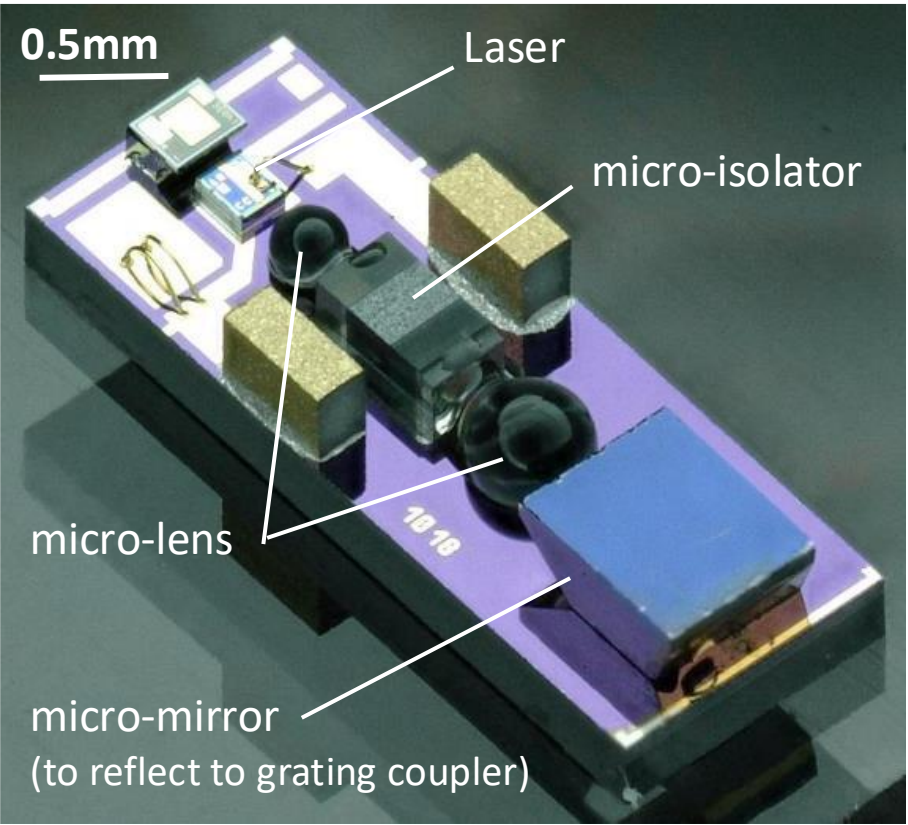
Active Device Integration (hybrid laser integration)



Active Device Integration (hybrid laser integration)

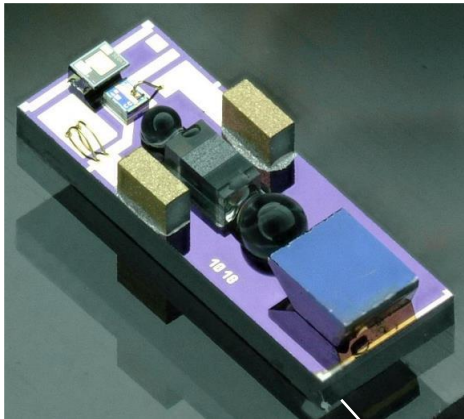


Active Device Integration (hybrid laser integration)

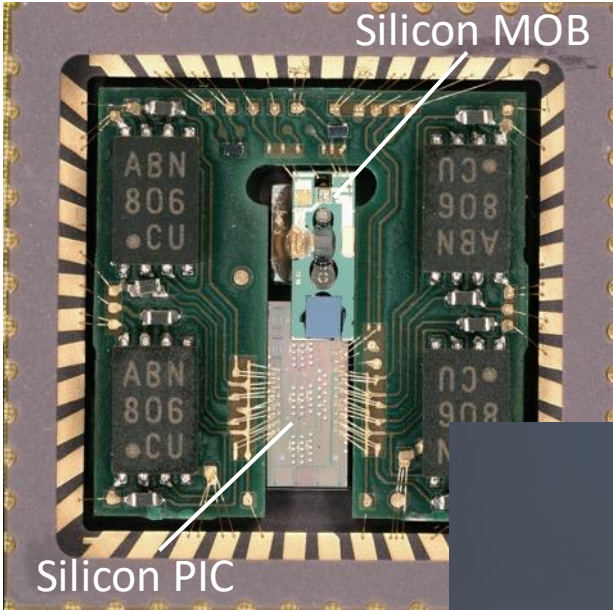
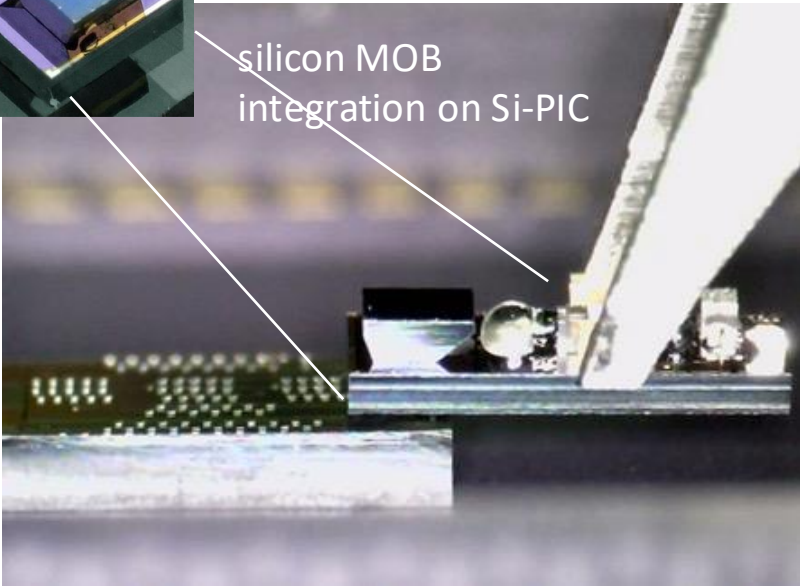


**CARDIOVASCULAR SCREENING DEVICE
BASED ON SILICON PHOTONICS**

Active Device Integration (hybrid laser integration)



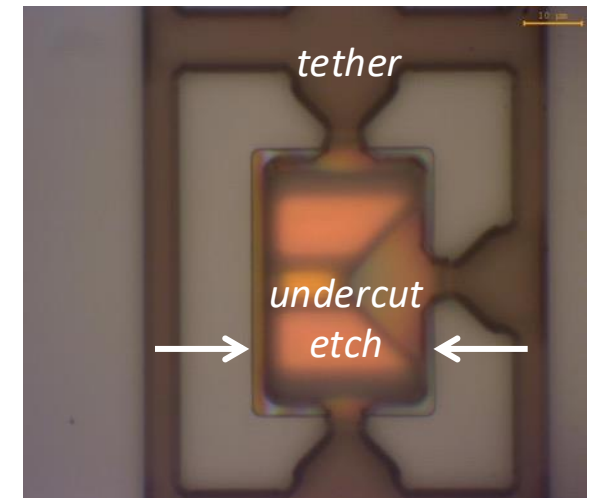
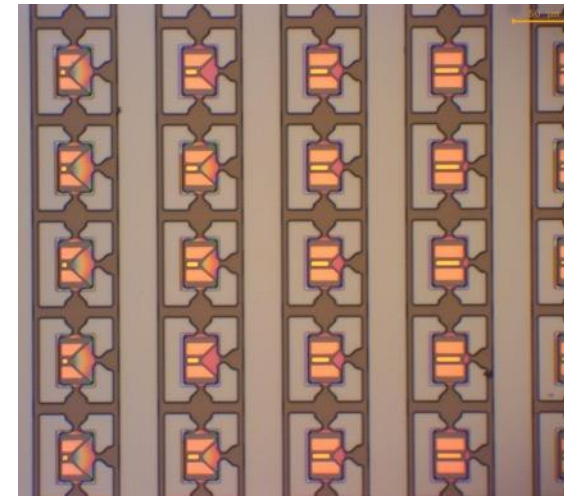
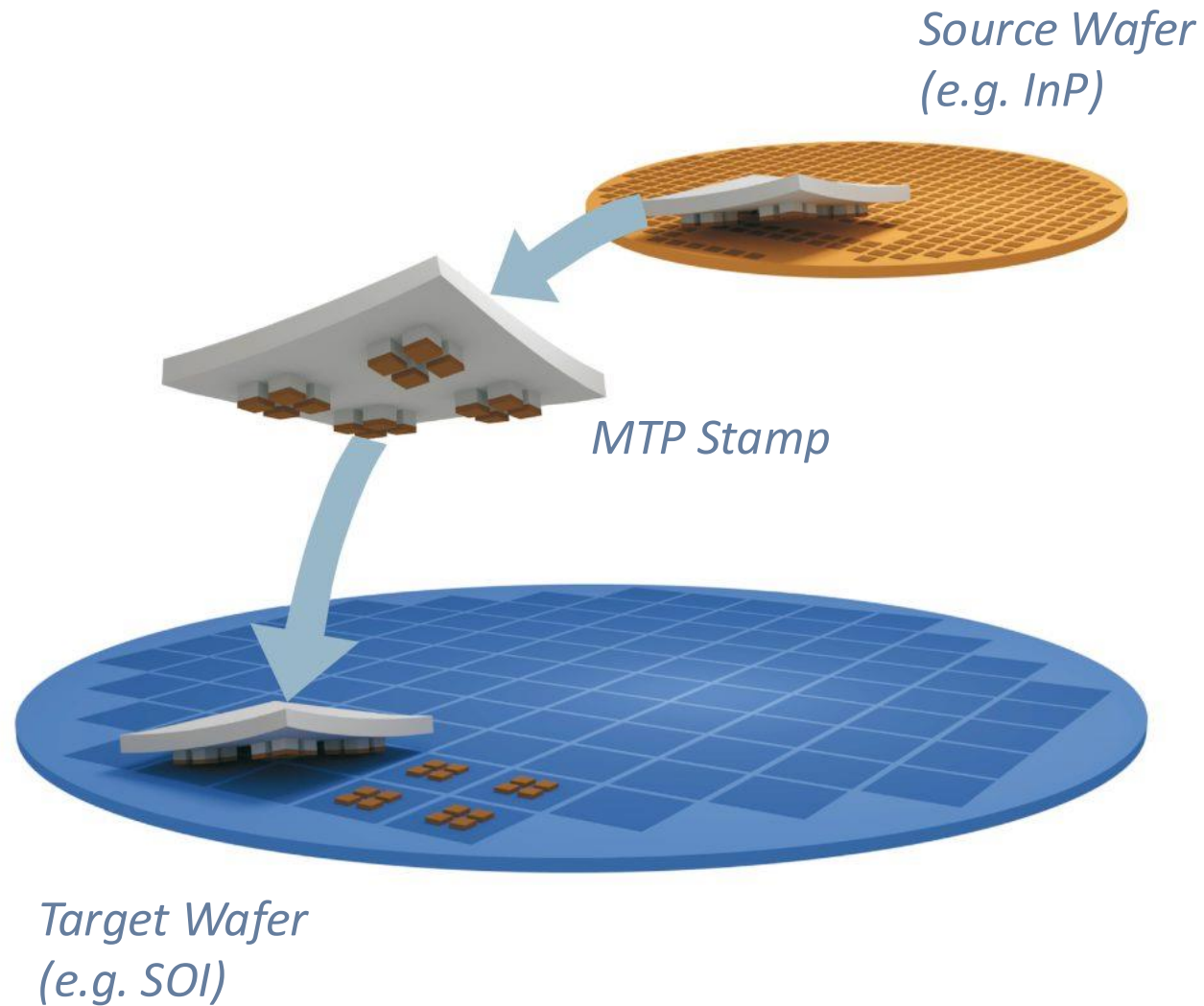
silicon MOB
integration on Si-PIC



10 Minute Break

Micro Transfer printing – Fundamentals, applications, and directions

Micro Transfer Printing



Micro Transfer Printing

Cost-saving

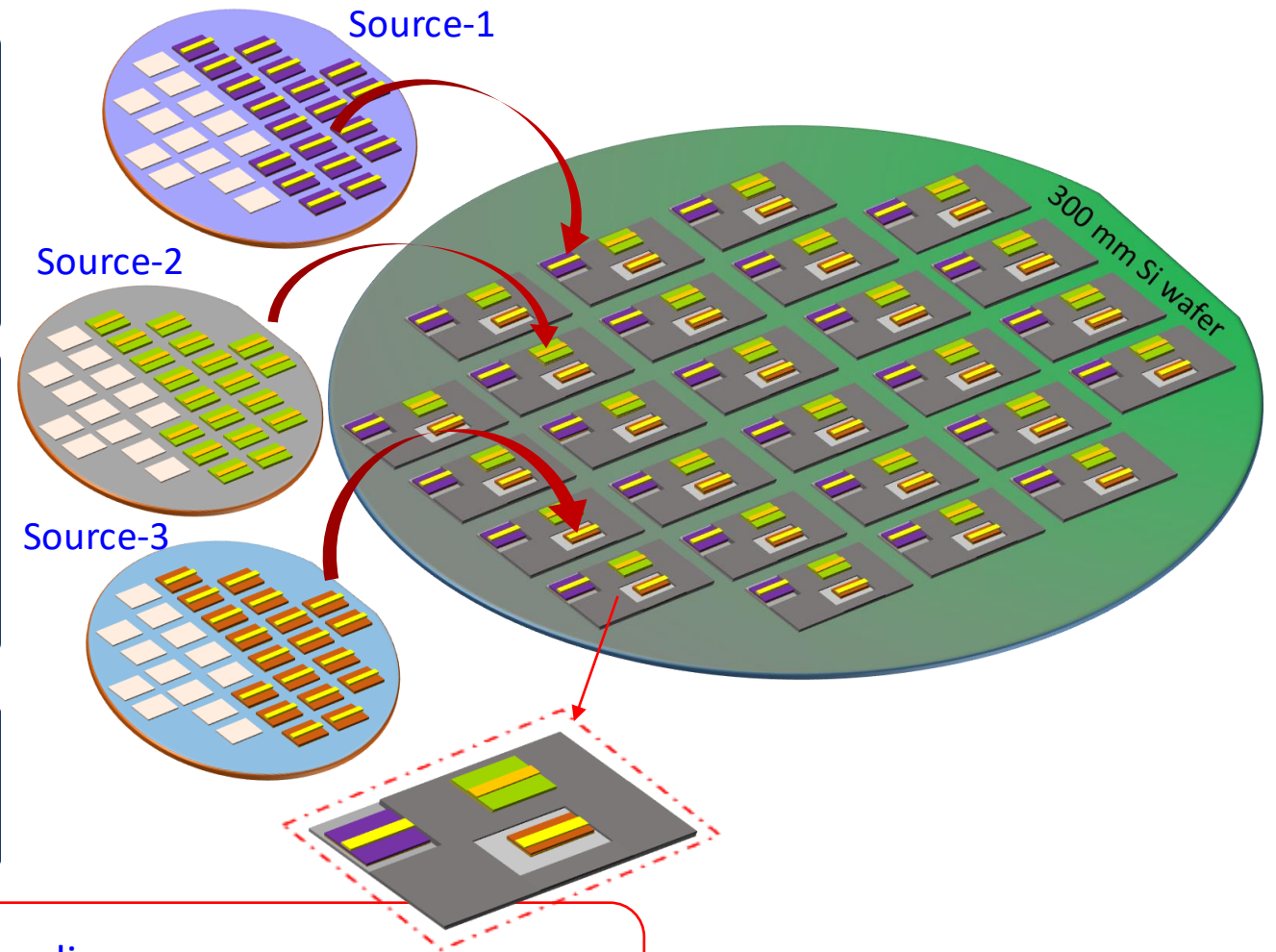
- Massively parallel processing
- High-volume production
- Effective usage of expensive epitaxial materials

Flexibility

- Epi with varying thicknesses, compositions can be placed on the same target
- Both edge-coupling and evanescent-coupling options are available

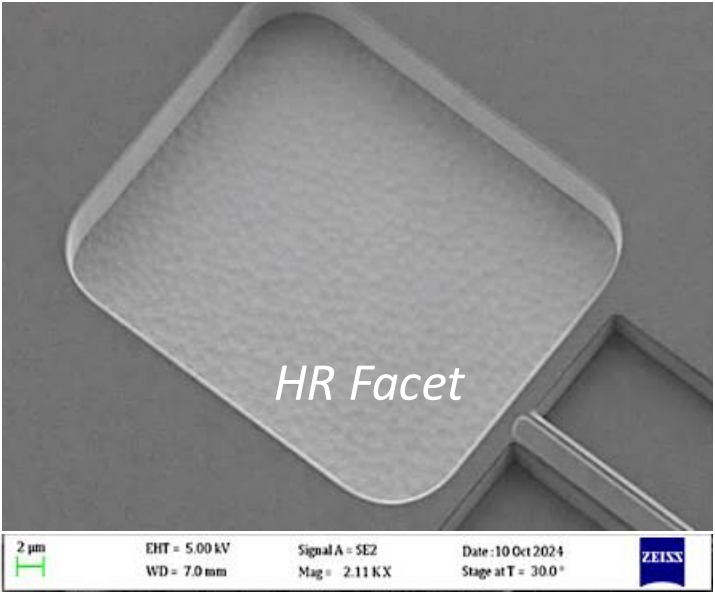
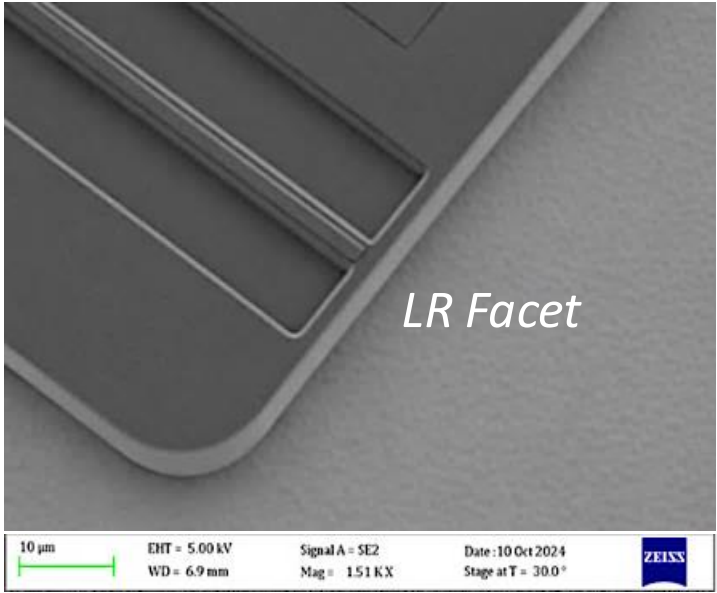
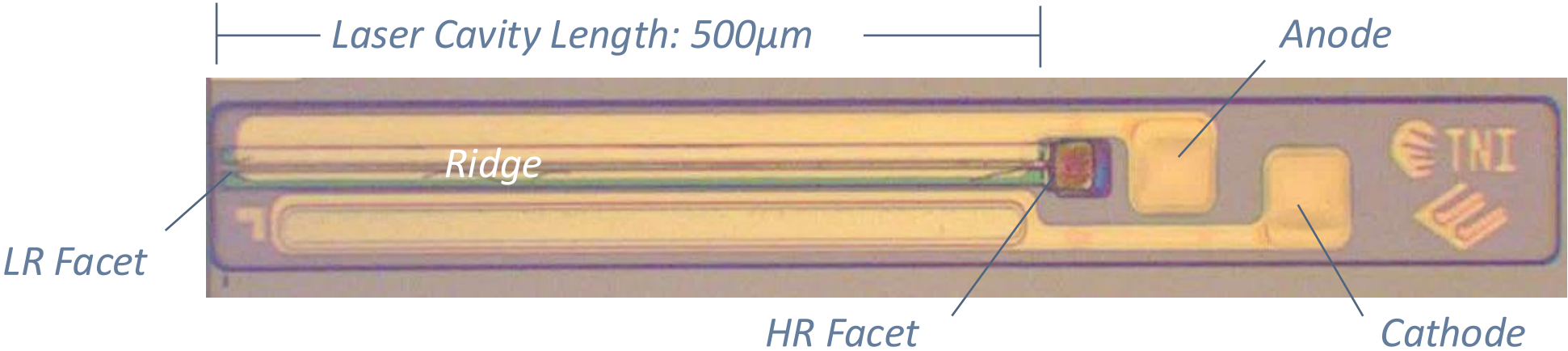
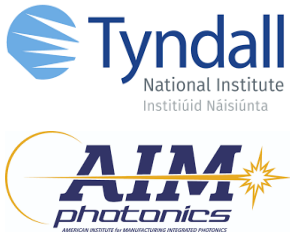
Sustainability

- Recycling of epi-substrate

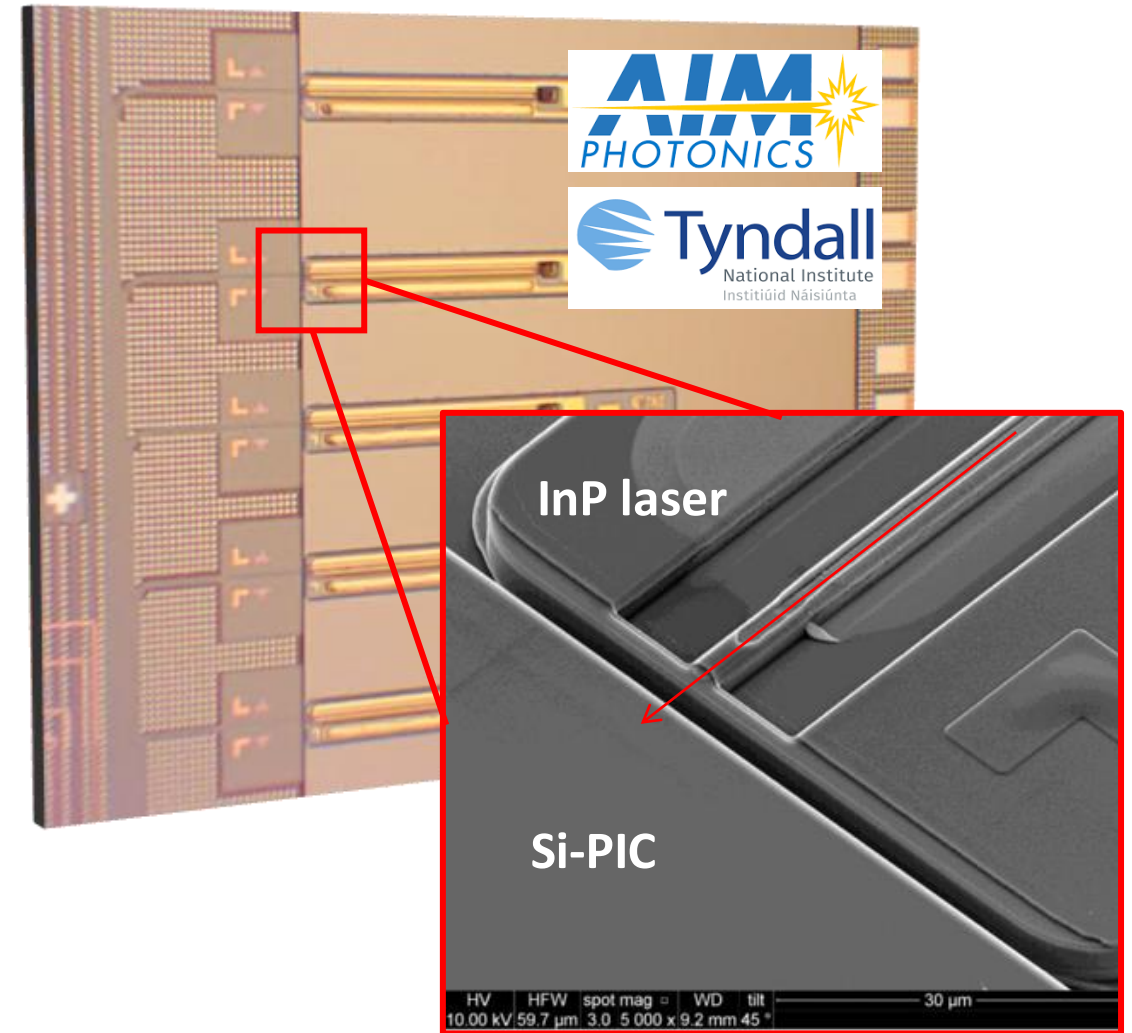


Evanescent coupling, Edge coupling
Multiple wavelength sources on same target
Multiple function (laser/detector/modulator) on same target

Micro Transfer Printing (InP on SOI)

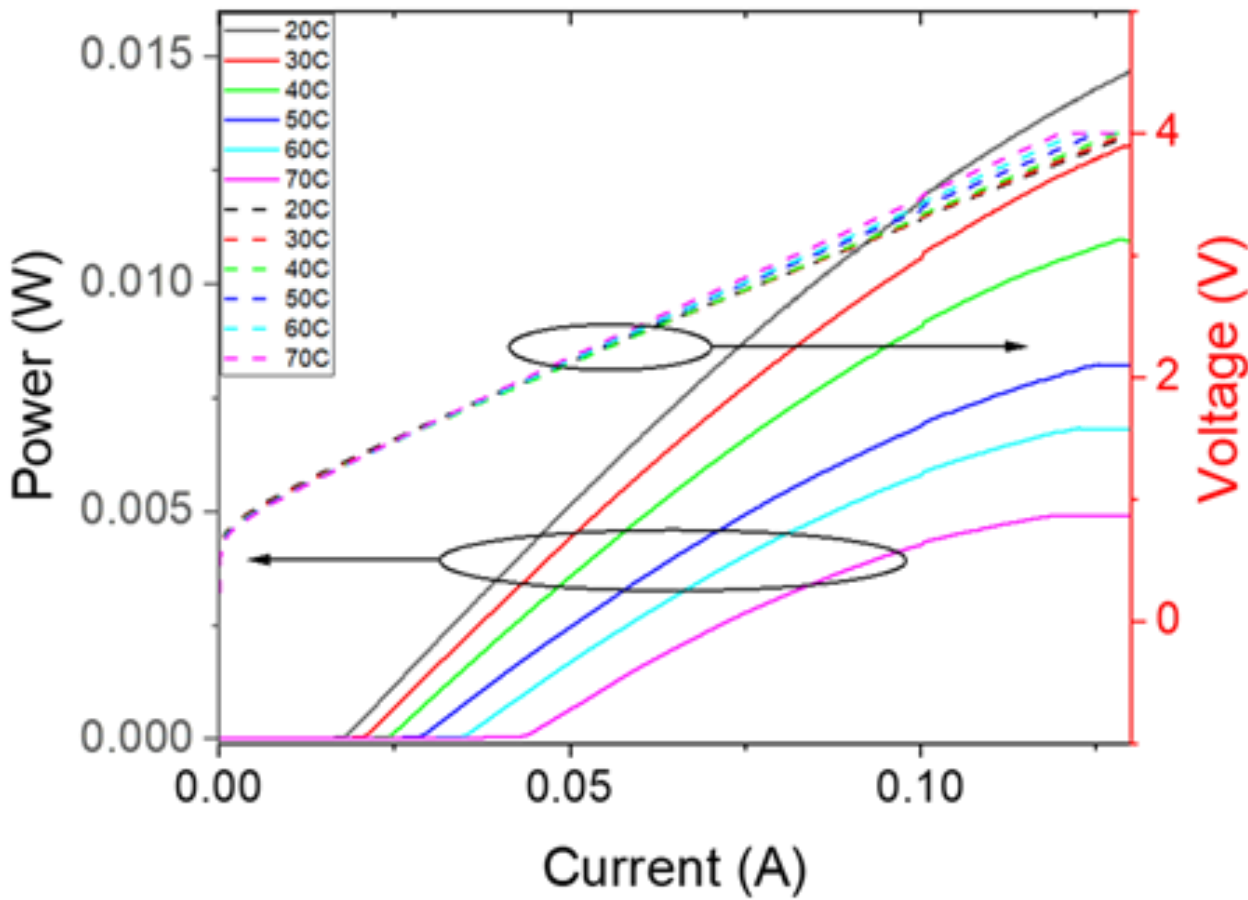
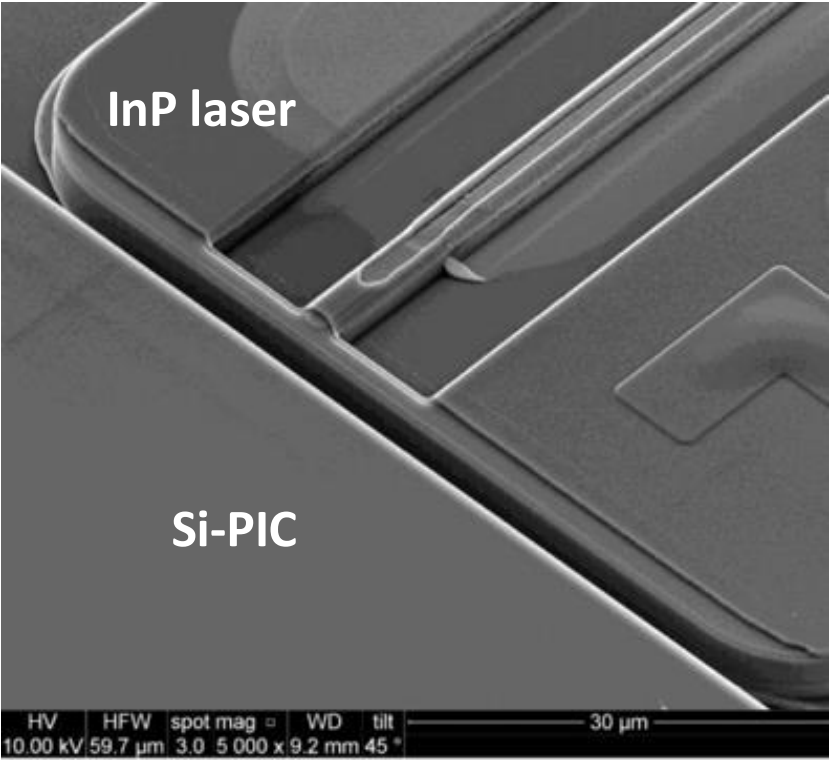


Micro Transfer Printing (InP on SOI)

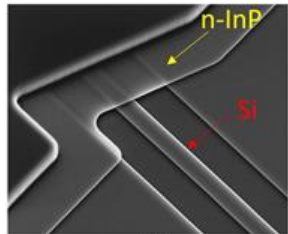
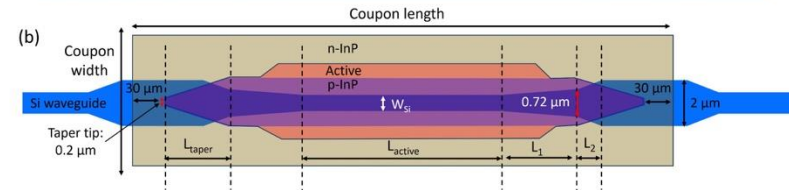
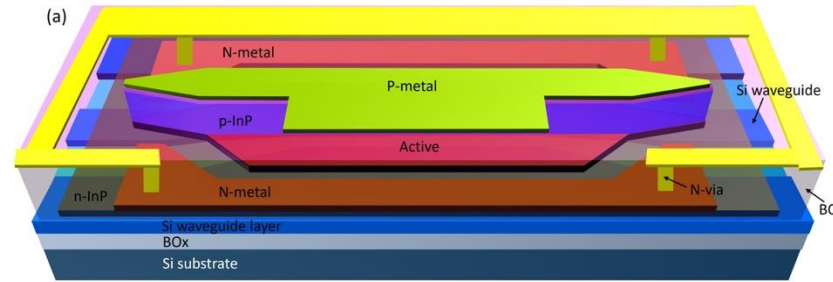
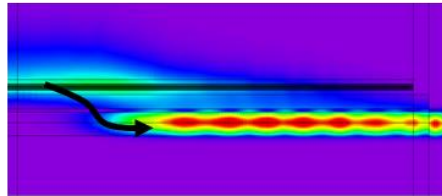
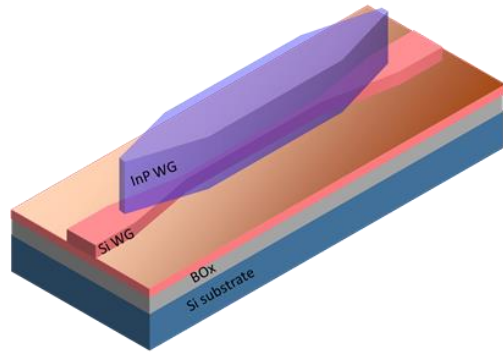


*Development of Transfer-Printed III-V C-Band Lasers
on Silicon Photonic Integrated Circuits for Multi-Project Wafer Offering
IEEE Electronic Components and Technology Conference (ECTC), May 2025.*

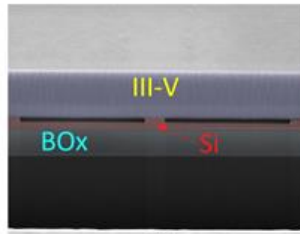
Micro Transfer Printing (InP on SOI)



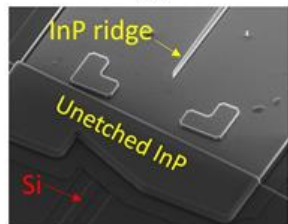
Micro Transfer Printing (evanescent coupling)



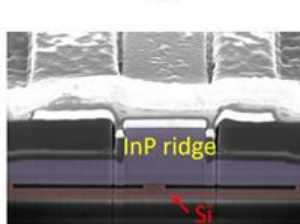
(a)



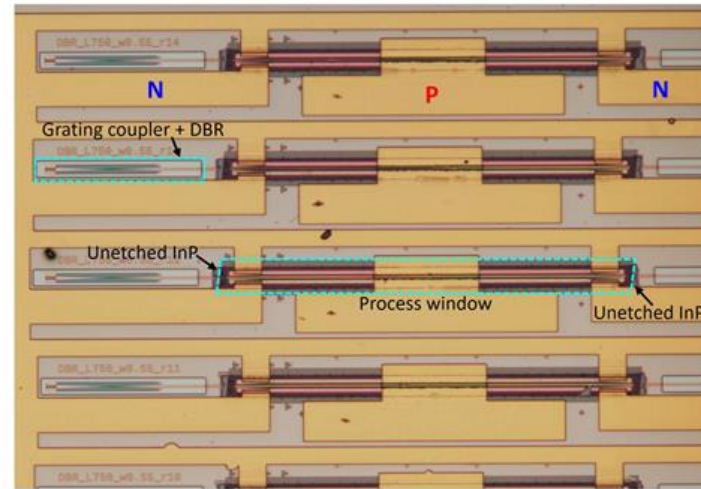
(b)



(c)



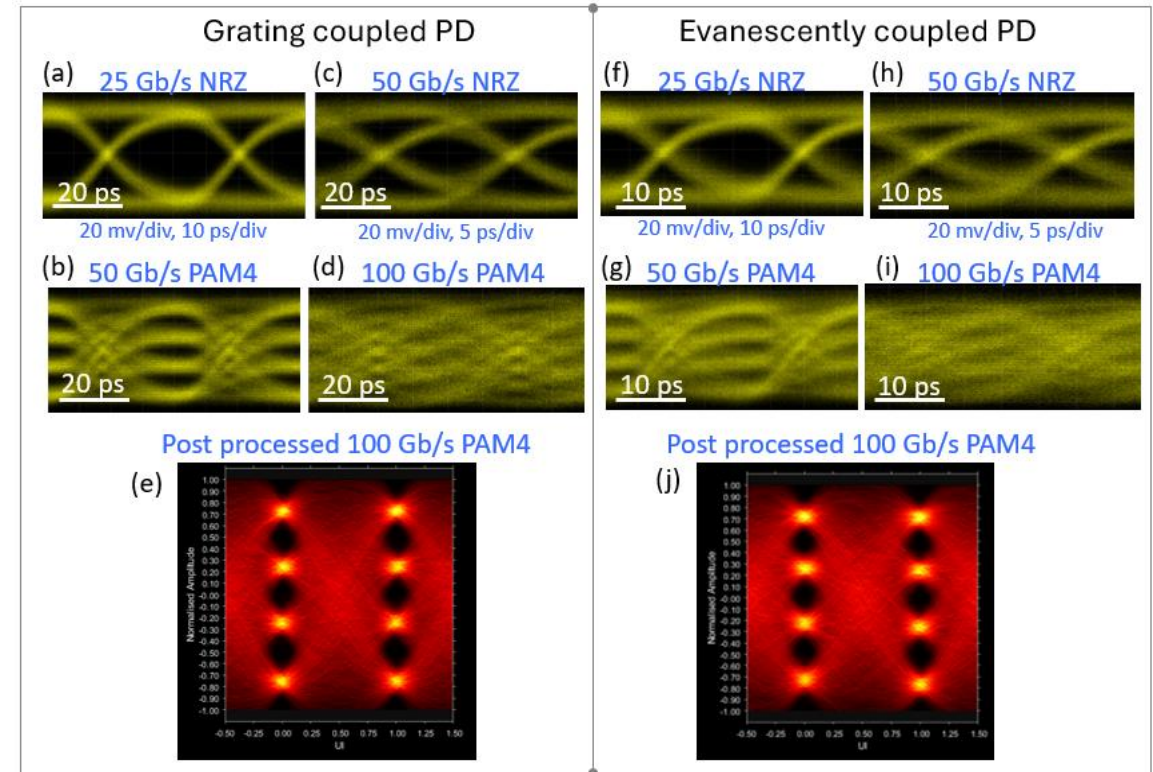
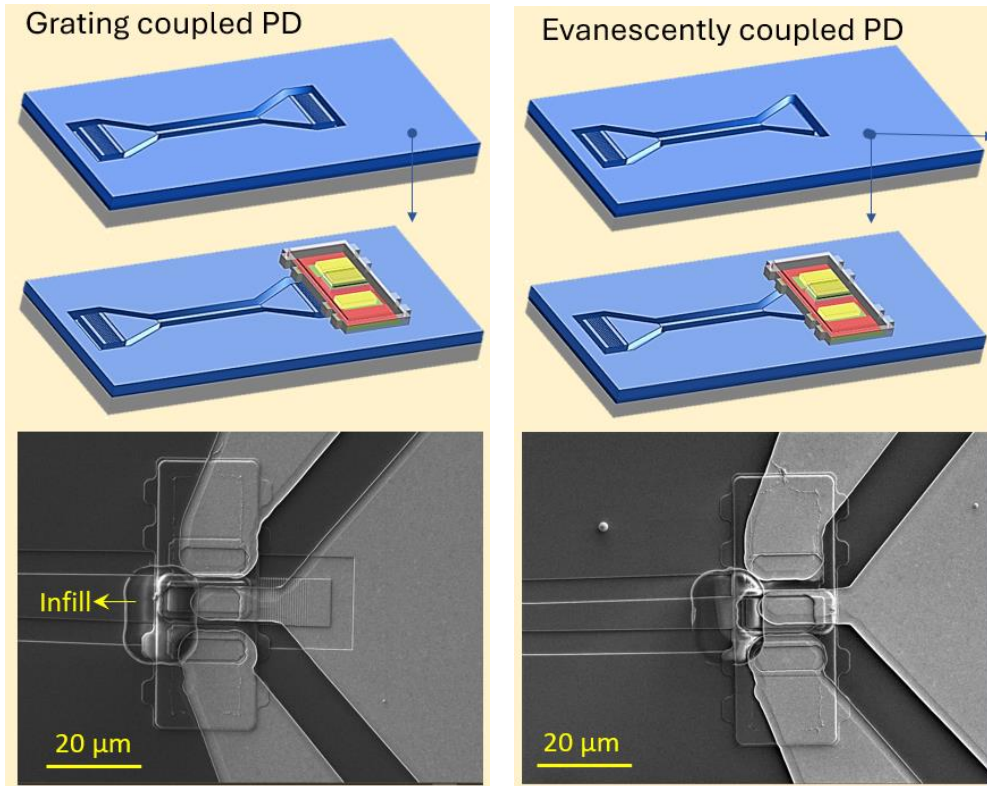
(d)



(e)

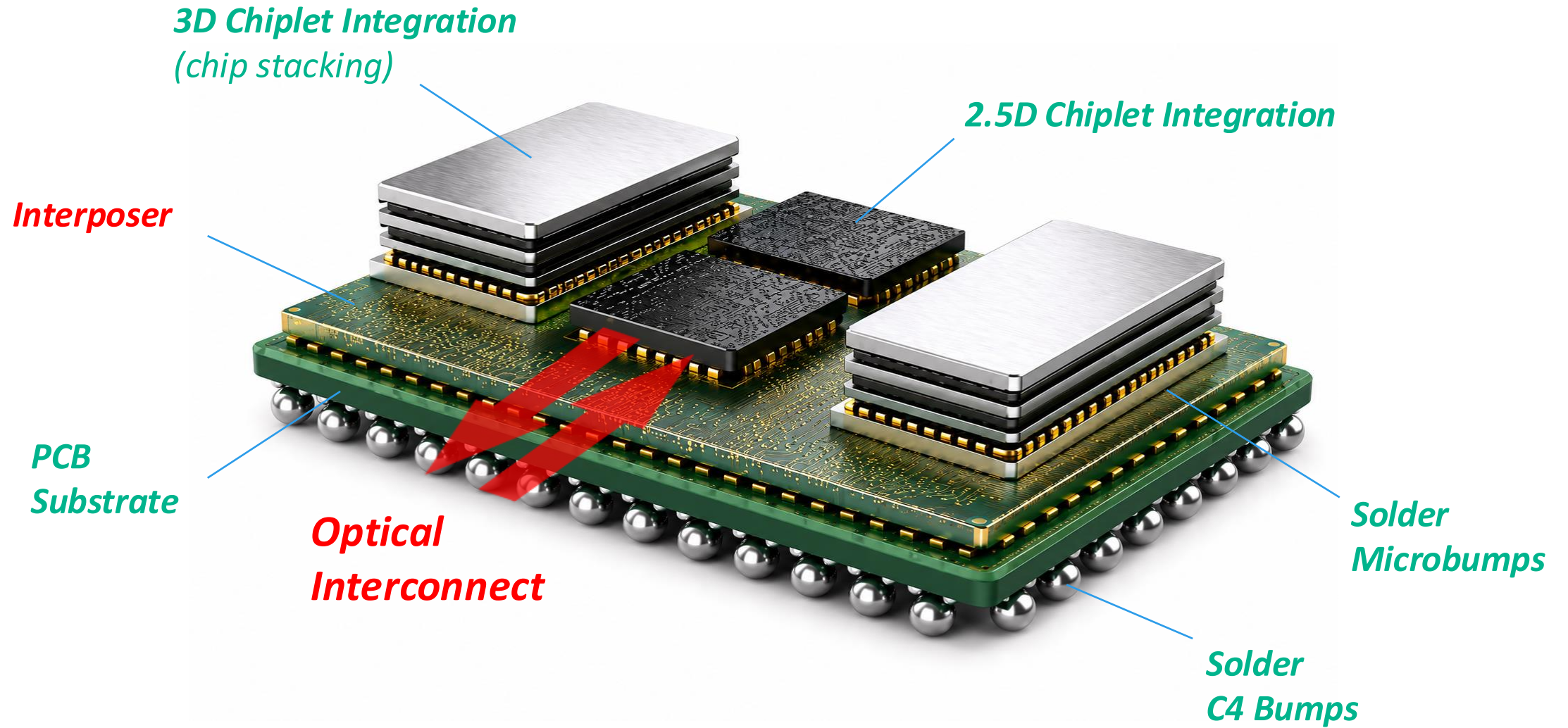
- Evanescently coupled lasers rely on a two waveguide approach to couple light between waveguides. The taper “squeezes the light from the top (active)WG InP to the bottom (passive)WG (Si)
- Mode control is achieved via grating structures in the Si WG
- Alignment precision between the waveguides is critical so the material is processed post print

Micro Transfer Printing (high speed photodiodes)

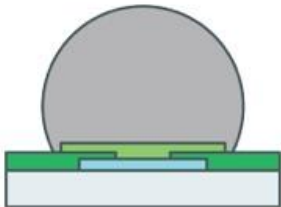
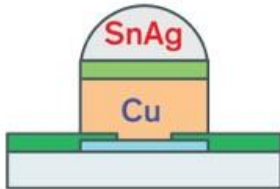
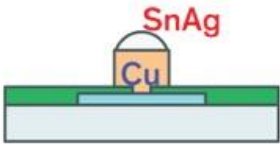


- 100 Gbps PAM4 ultra-thin photodetectors integrated on SOI platform
- Devices are coupled to the Si waveguides via butt, grating and evanescent coupling schemes with responsivities of 0.13, 0.3 and 0.6 A/W respectively

Future Developments



Electrical Packaging (flipchip)

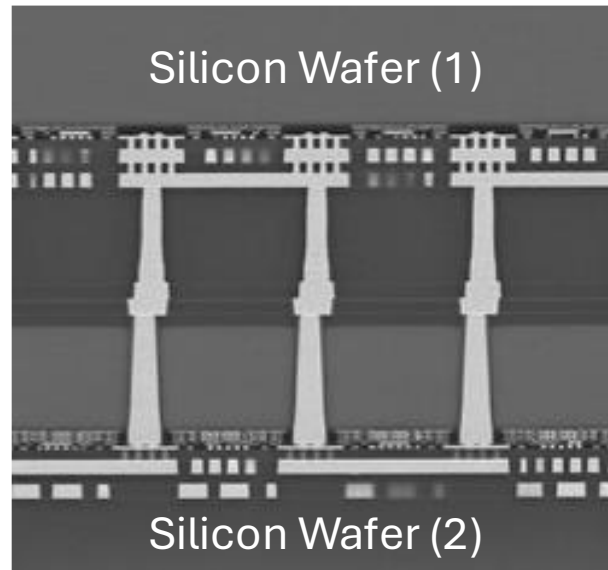
	SnPb C4 Bump	Pb-Free C4 Bump	Cu Pillar + Pb-free Cap	Cu μ -Pillar + Pb-free Cap
Structure				
Diameter	75 – 200 μm	75 – 150 μm	50 – 100 μm	10 – 30 μm



Electrical Packaging (micro-bumps)

Aspect	Details
Definition	Fine-pitch solder interconnects for die-to-die or die-to-interposer connections
Pitch range	Typically ~40 μm down to ~20 μm ; scaling below this is challenging
Materials	Sn-based solders with under-bump metallization (UBM) stacks
Use cases	Widely used in 2.5D interposers and early 3D ICs
Electrical performance	Limited by bump resistance and parasitic inductance/capacitance
Mechanical role	Provides electrical connection and mechanical standoff
Reliability concern	Solder fatigue driven by thermal cycling and CTE mismatch
Electromigration	High current density can cause EM at fine pitch
Manufacturing impact	Yield and inspection complexity increase as pitch shrinks
Technology maturity	Mature, lower risk, and lower cost than hybrid bonding

Electrical Packaging (hybrid bonding)



**Surface
Preparation**



**Wafer-to-Wafer
Alignment**



**Wafer-to-Wafer
Bonding**

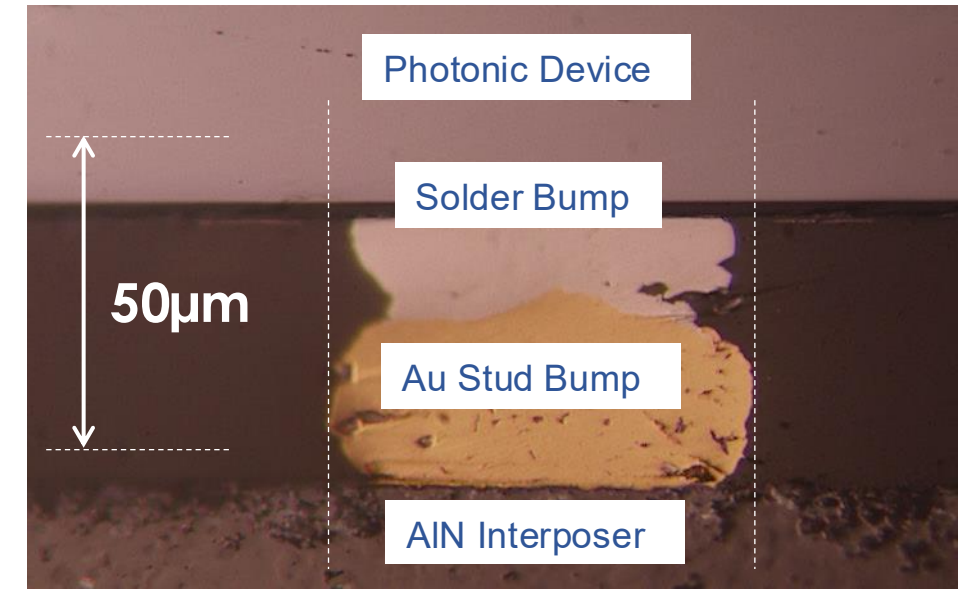
Electrical Packaging (hybrid bonding)

Aspect	Details
Basic concept	Direct copper-to-copper and dielectric bonding; no solder micro-bumps
Interconnect pitch	Ultra-fine pitch ($\leq 10\text{ }\mu\text{m}$ today, roadmap to sub- $5\text{ }\mu\text{m}$)
Interconnect density	Very high I/O density for wide die-to-die interfaces
Electrical performance	Lower resistance and parasitics; improved bandwidth and energy per bit
Integration style	Supports true 3D stacking (logic–logic, logic–memory)
Process requirements	Extreme surface flatness, cleanliness, and alignment accuracy required
Package form factor	Reduced stack height and improved thermal conduction paths
Reliability focus	Shifts from solder fatigue to interface adhesion and thermo-mechanical stress
Manufacturing impact	Requires advanced wafer-level metrology and inspection
Strategic role	Key enabler for AI, HPC, and next-generation chiplet architectures

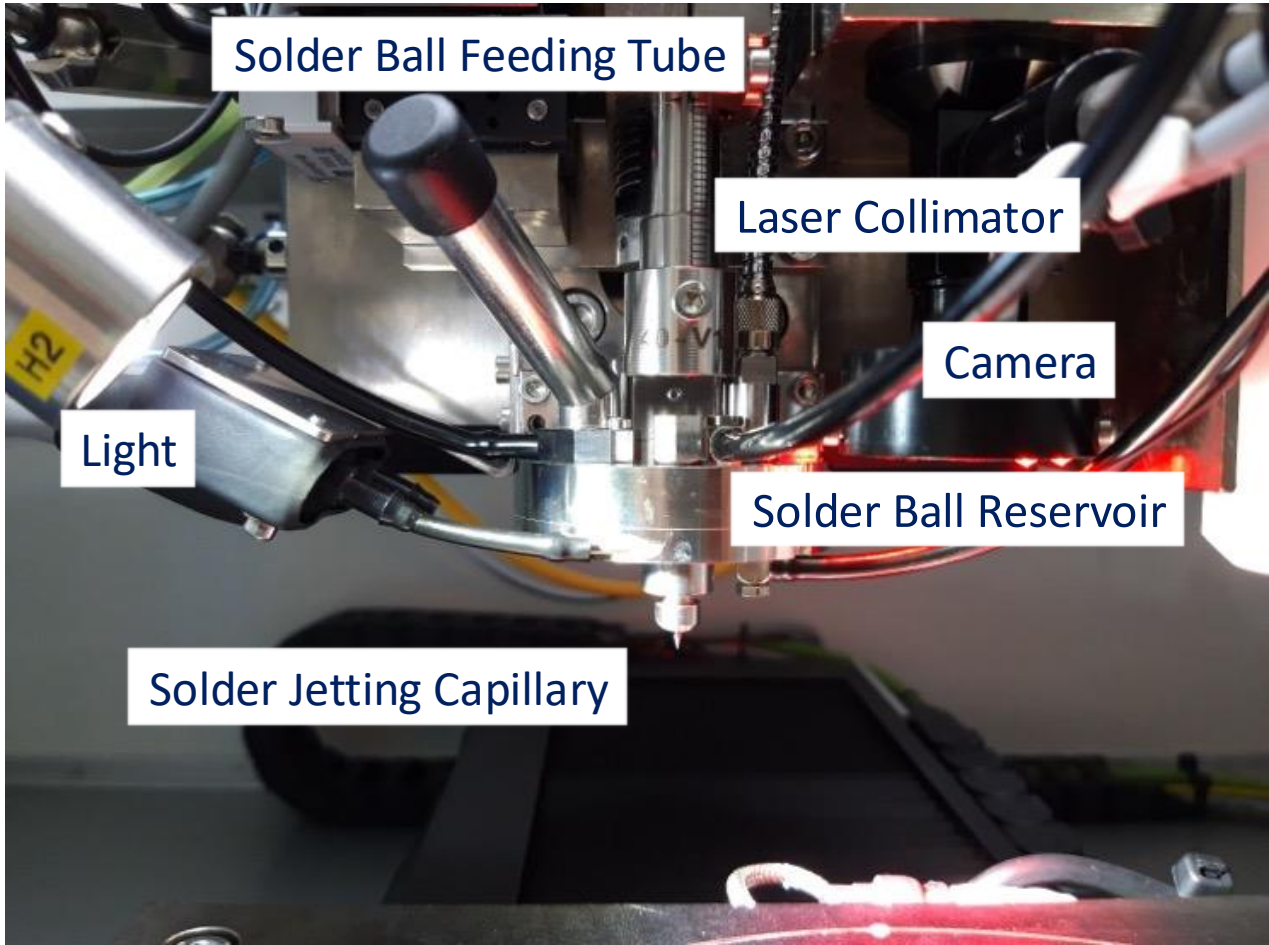
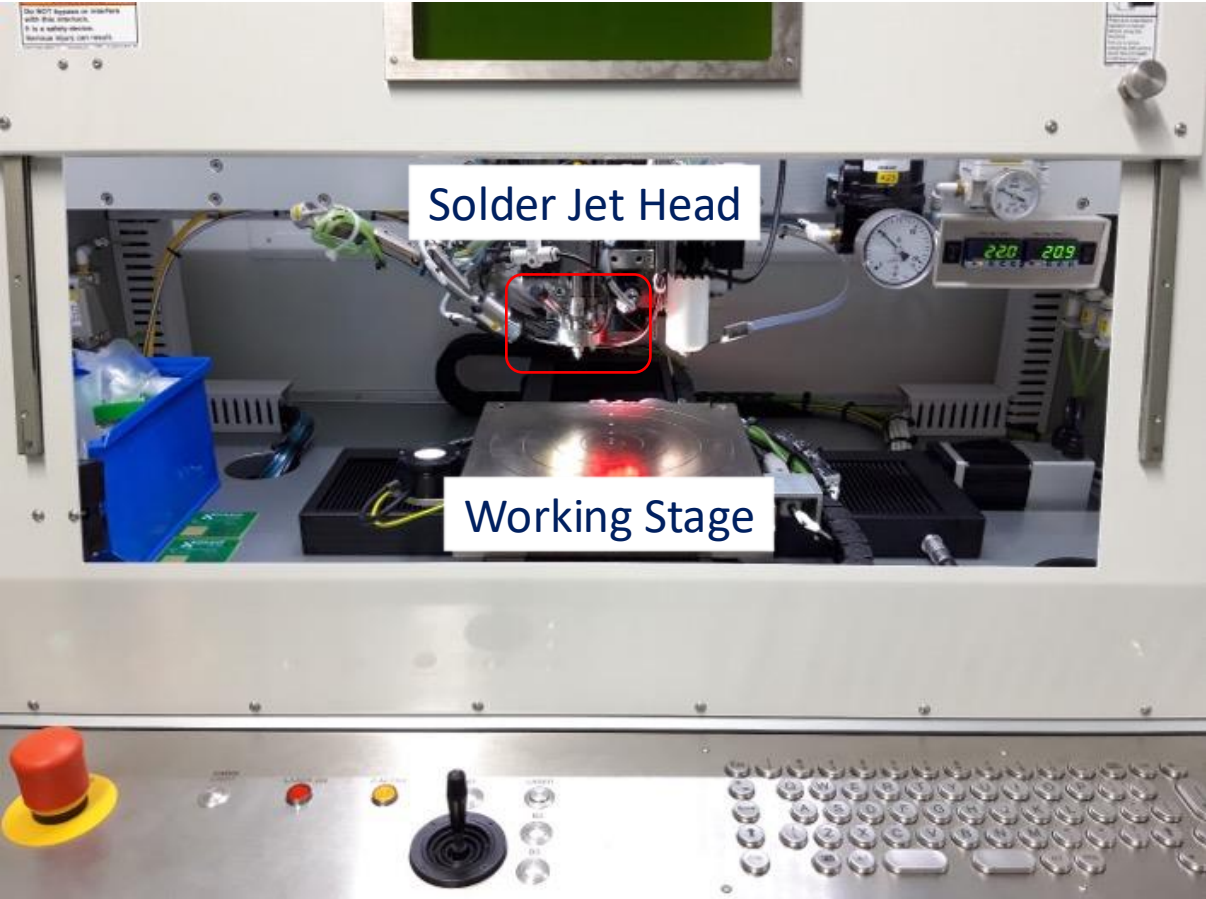
Electrical Packaging (solder sphere jetting)



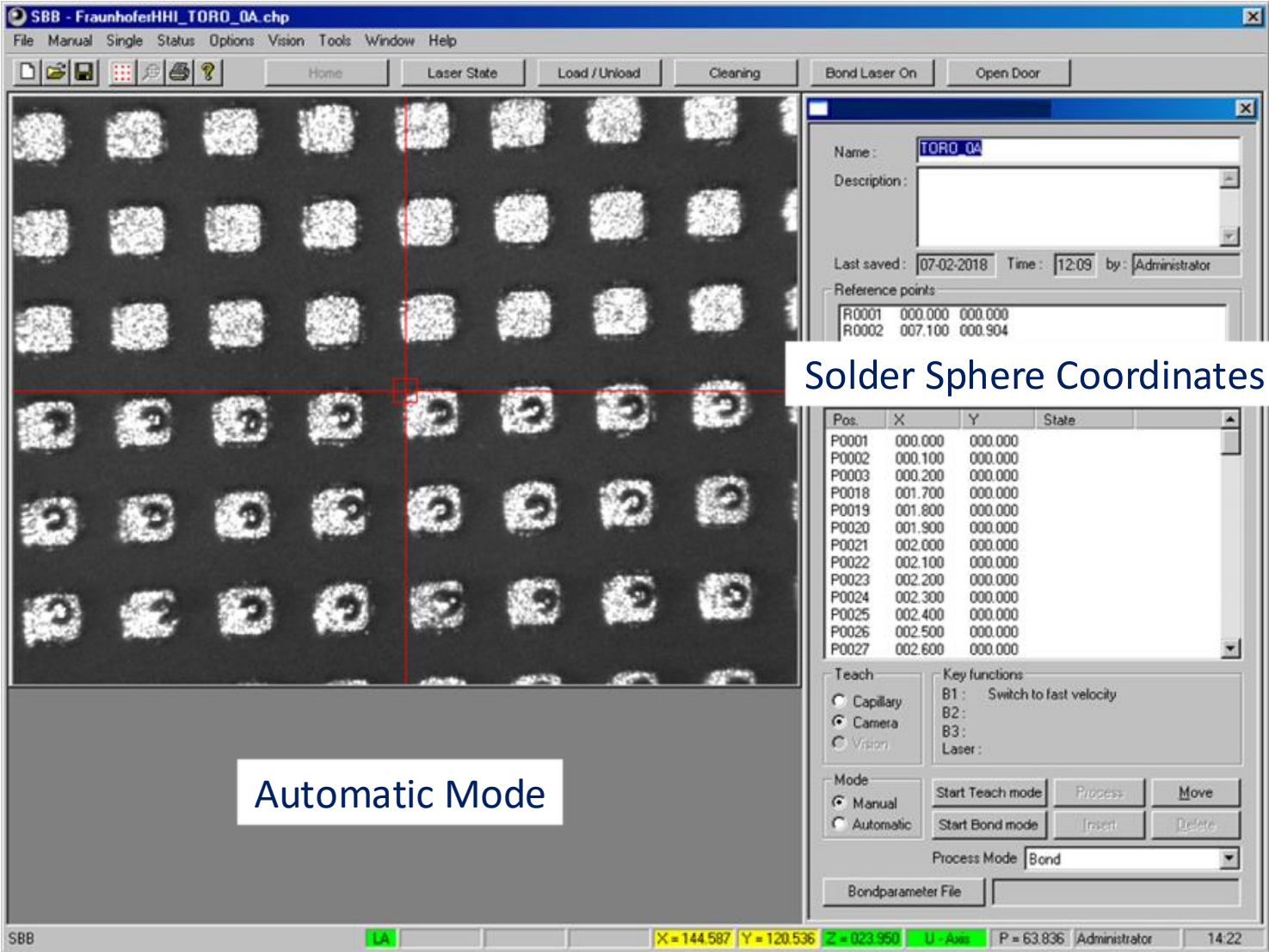
Electrical Packaging (electrical interposers)



Electrical Packaging (solder sphere jetting)



Electrical Packaging (solder sphere jetting)



The screenshot displays the SBB - FraunhoferHHL_TORO_0A.chp software interface. The main window shows a grid of solder spheres with a red crosshair indicating a selected point. The interface includes a menu bar (File, Manual, Single, Status, Options, Vision, Tools, Window, Help) and a toolbar with icons for Home, Laser State, Load / Unload, Cleaning, Bond Laser On, and Open Door. A right-hand panel contains a 'Name' field (TORO_0A), a 'Description' field, 'Last saved' information (07-02-2018, 12:09, Administrator), and a 'Reference points' table:

Pos.	X	Y	State
P0001	000.000	000.000	
P0002	000.100	000.000	
P0003	000.200	000.000	
P0018	001.700	000.000	
P0019	001.800	000.000	
P0020	001.900	000.000	
P0021	002.000	000.000	
P0022	002.100	000.000	
P0023	002.200	000.000	
P0024	002.300	000.000	
P0025	002.400	000.000	
P0026	002.500	000.000	
P0027	002.600	000.000	

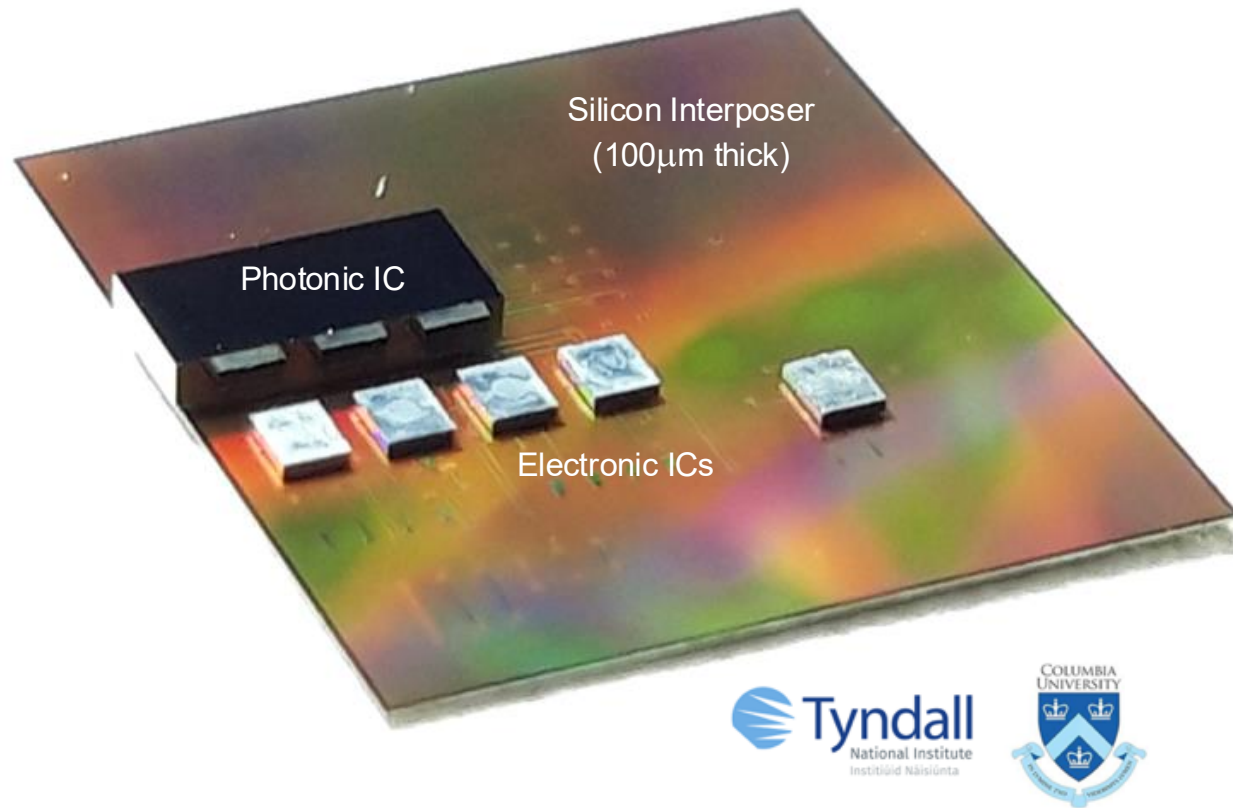
Below the table are 'Teach' and 'Mode' sections. The 'Teach' section has radio buttons for Capillary, Camera (selected), and Vision. The 'Mode' section has radio buttons for Manual (selected) and Automatic. A 'Process Mode' dropdown is set to 'Bond'. At the bottom, a status bar shows 'SBB', 'LA', and coordinates: X = 144.587, Y = 120.536, Z = 023.950, U - Axis, P = 63.836, Administrator, 14:22.

Solder Sphere Coordinates

Automatic Mode

Electrical Packaging (IC integration)

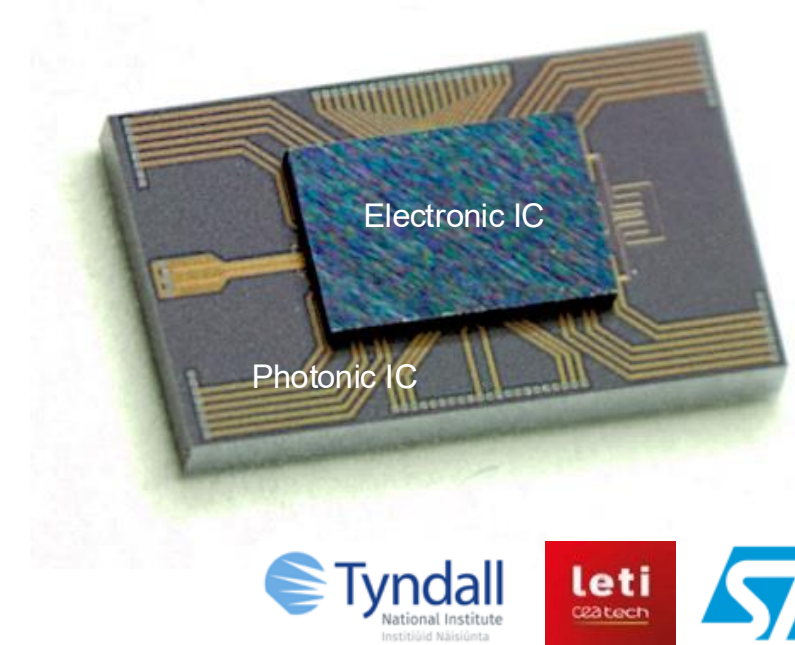
2.5D PIC-EIC Co-Packaging



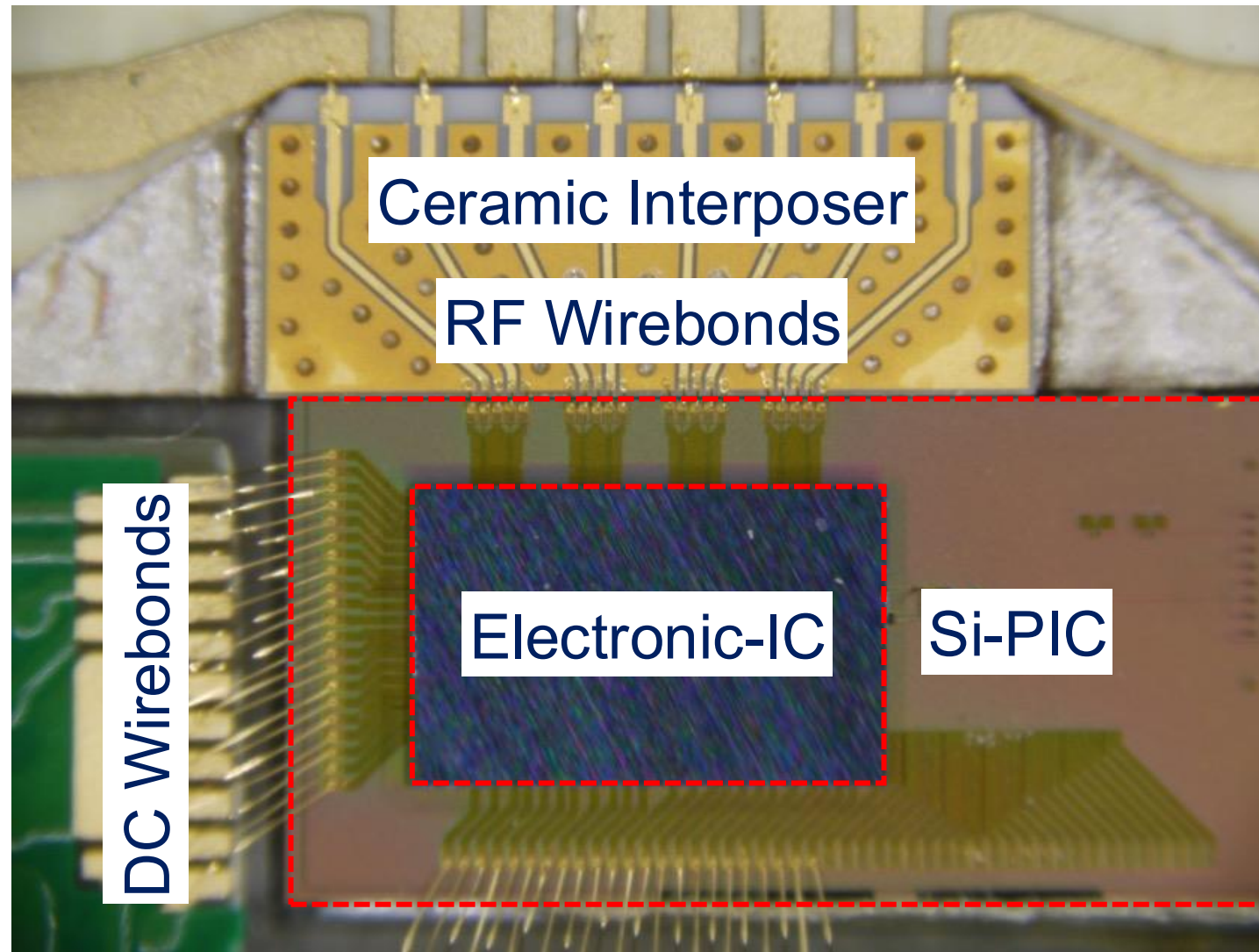
Ultralow-crosstalk, strictly non-blocking microring-based optical switch
Photonics Research, Vol.7 Issue, 2, 2019.

Silicon photonic 2.5D multi-chip module transceiver for high-performance data centers,
Journal of Lightwave Technology, 38(13), Jan 2020.

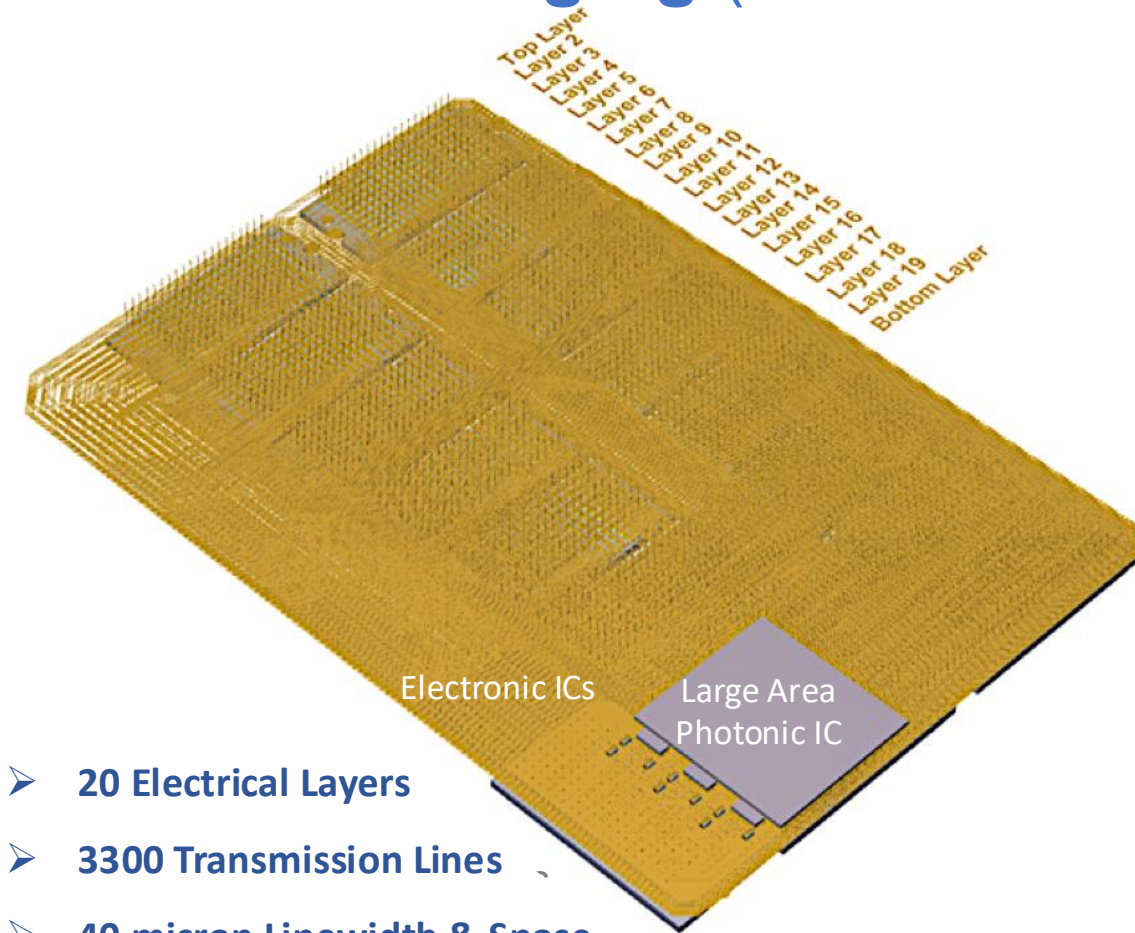
3D PIC-EIC Co-Packaging



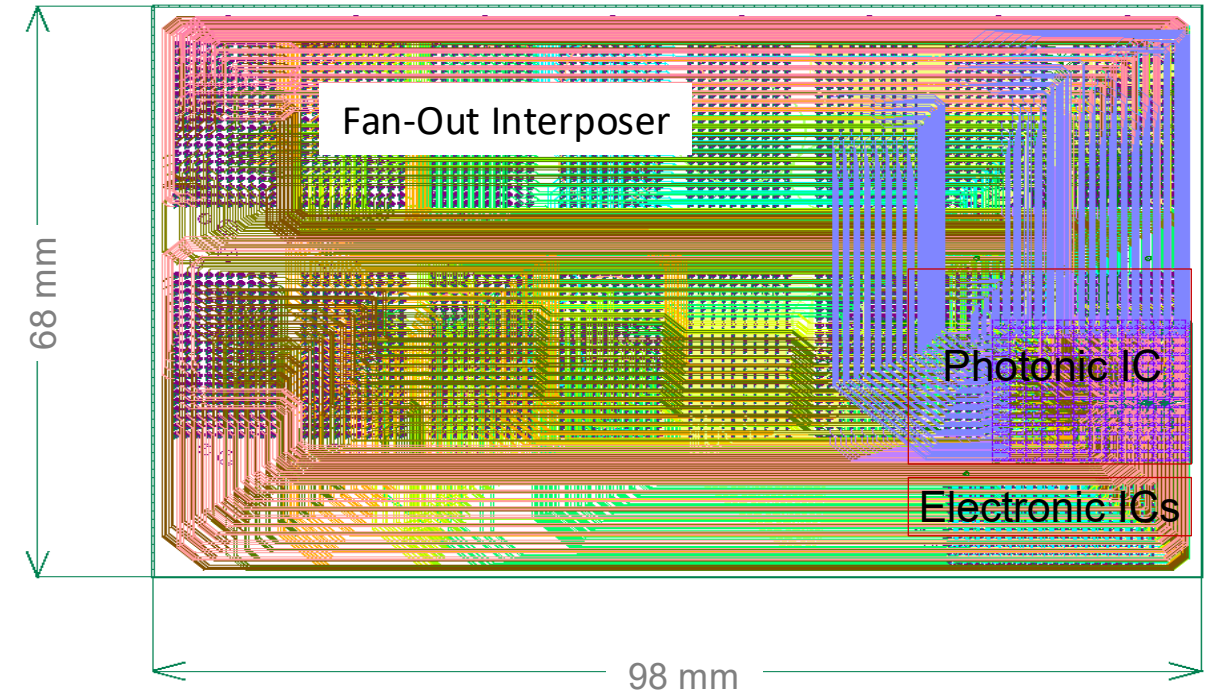
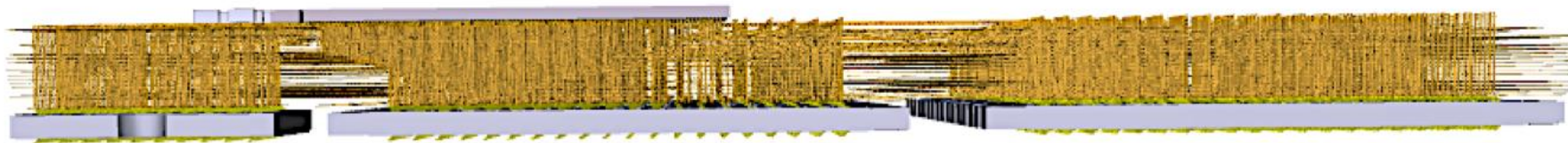
Electrical Packaging (IC integration)



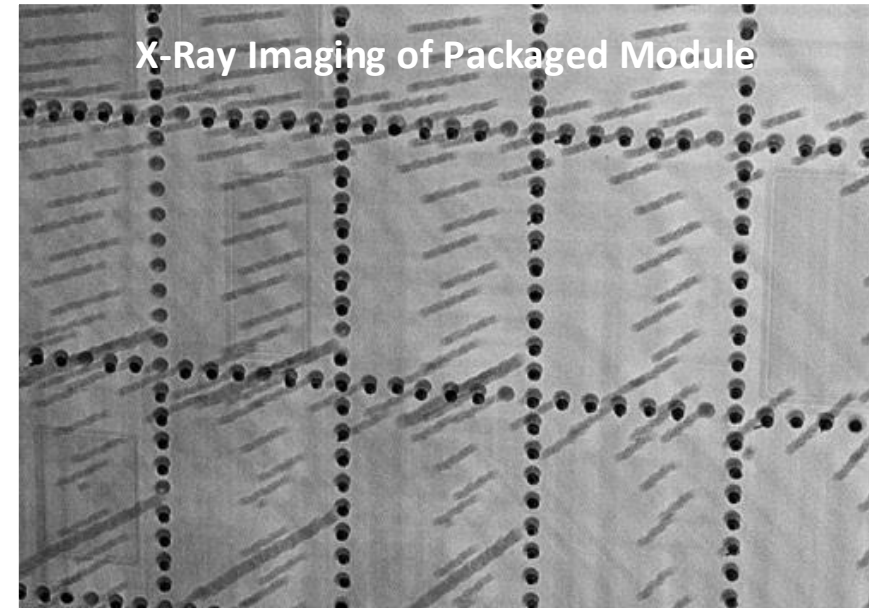
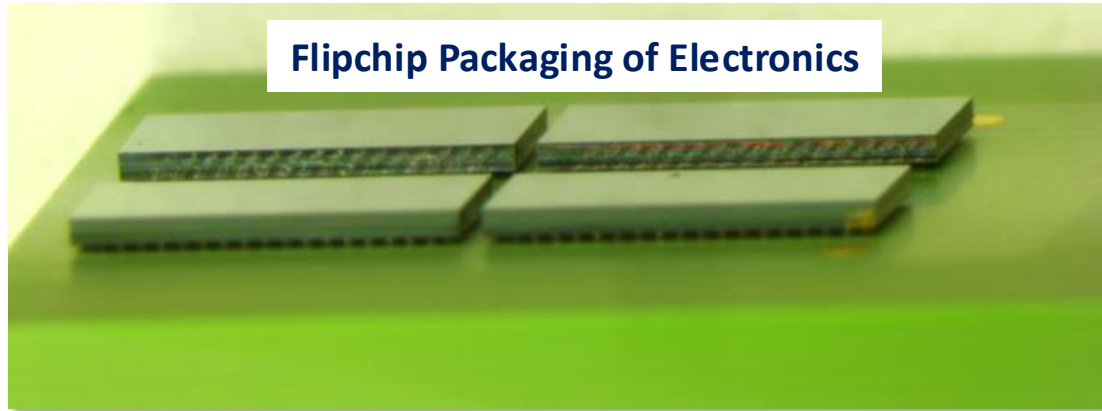
Electrical Packaging (electrical interposers)



- 20 Electrical Layers
- 3300 Transmission Lines
- 40 micron Linewidth & Space

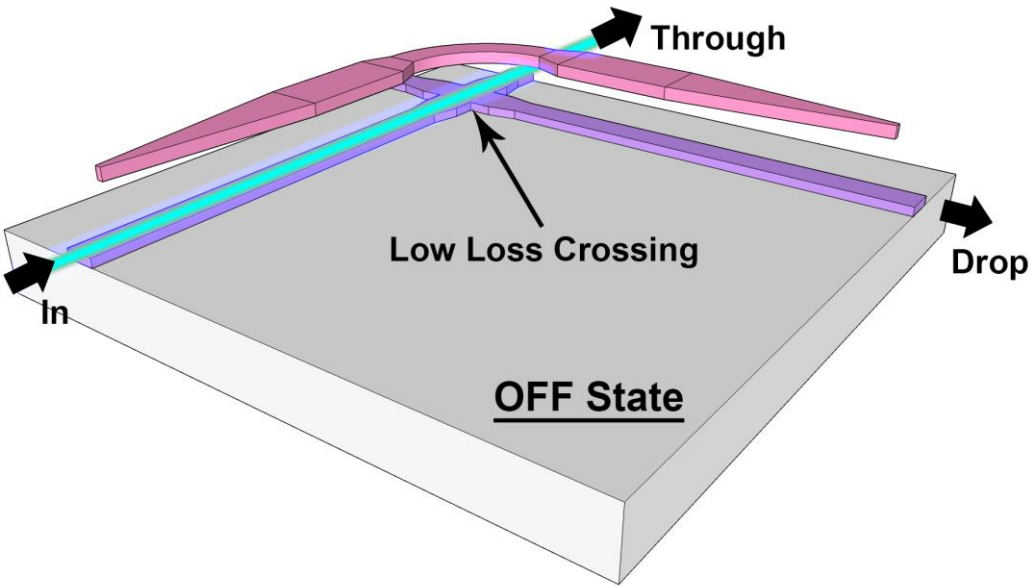
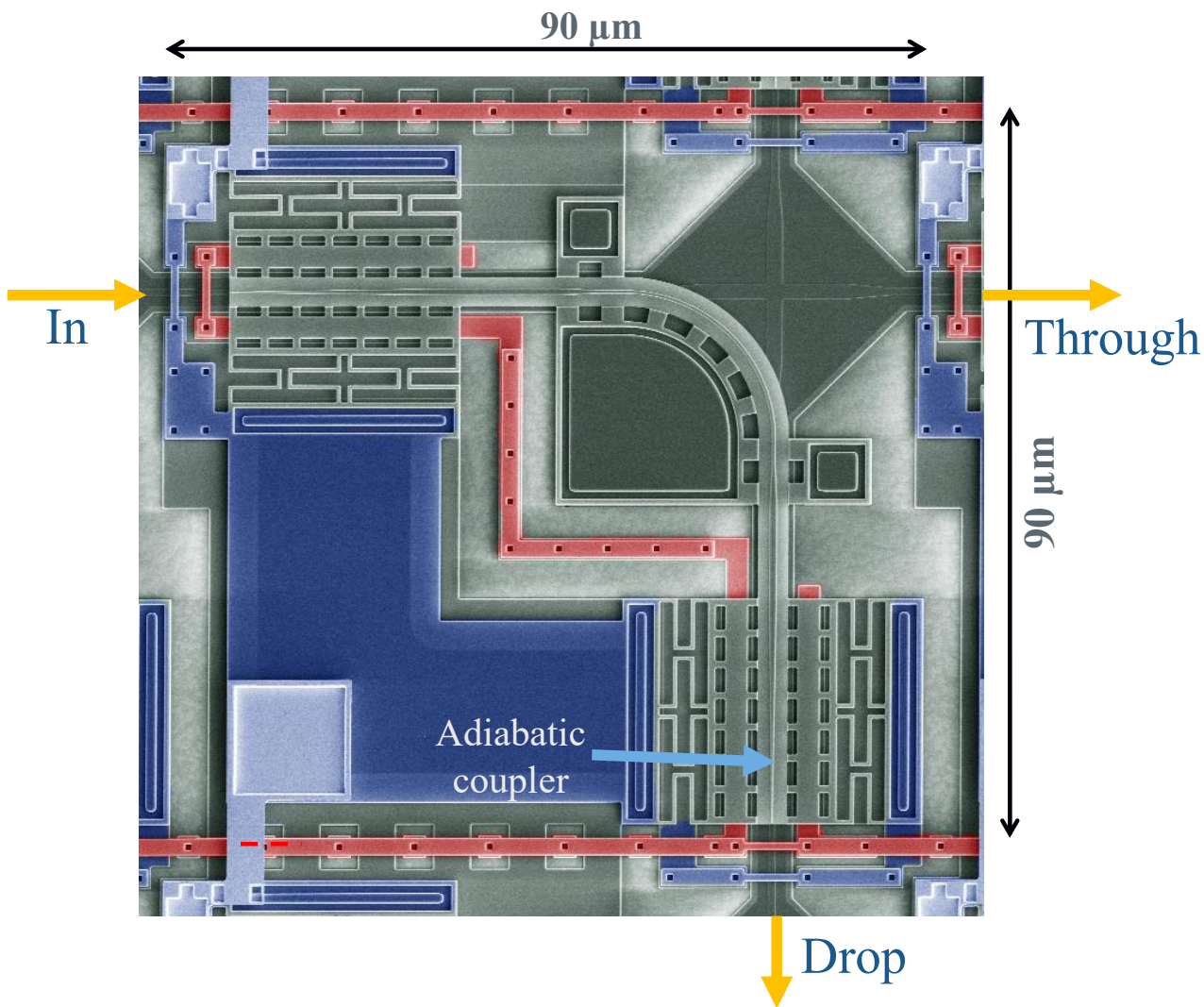


Electrical Packaging (electrical interposers)

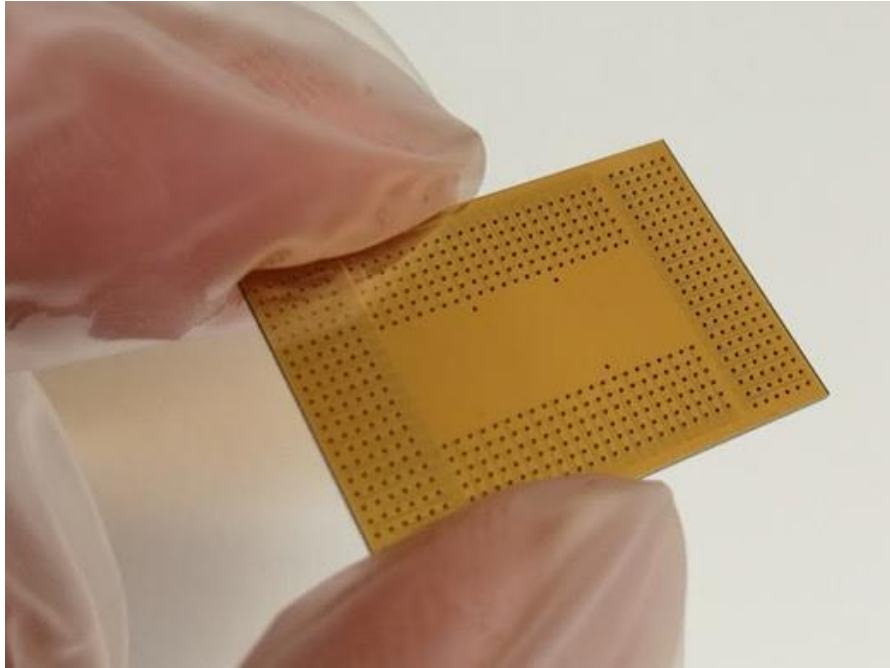


Electrical Packaging (electrical interposers)

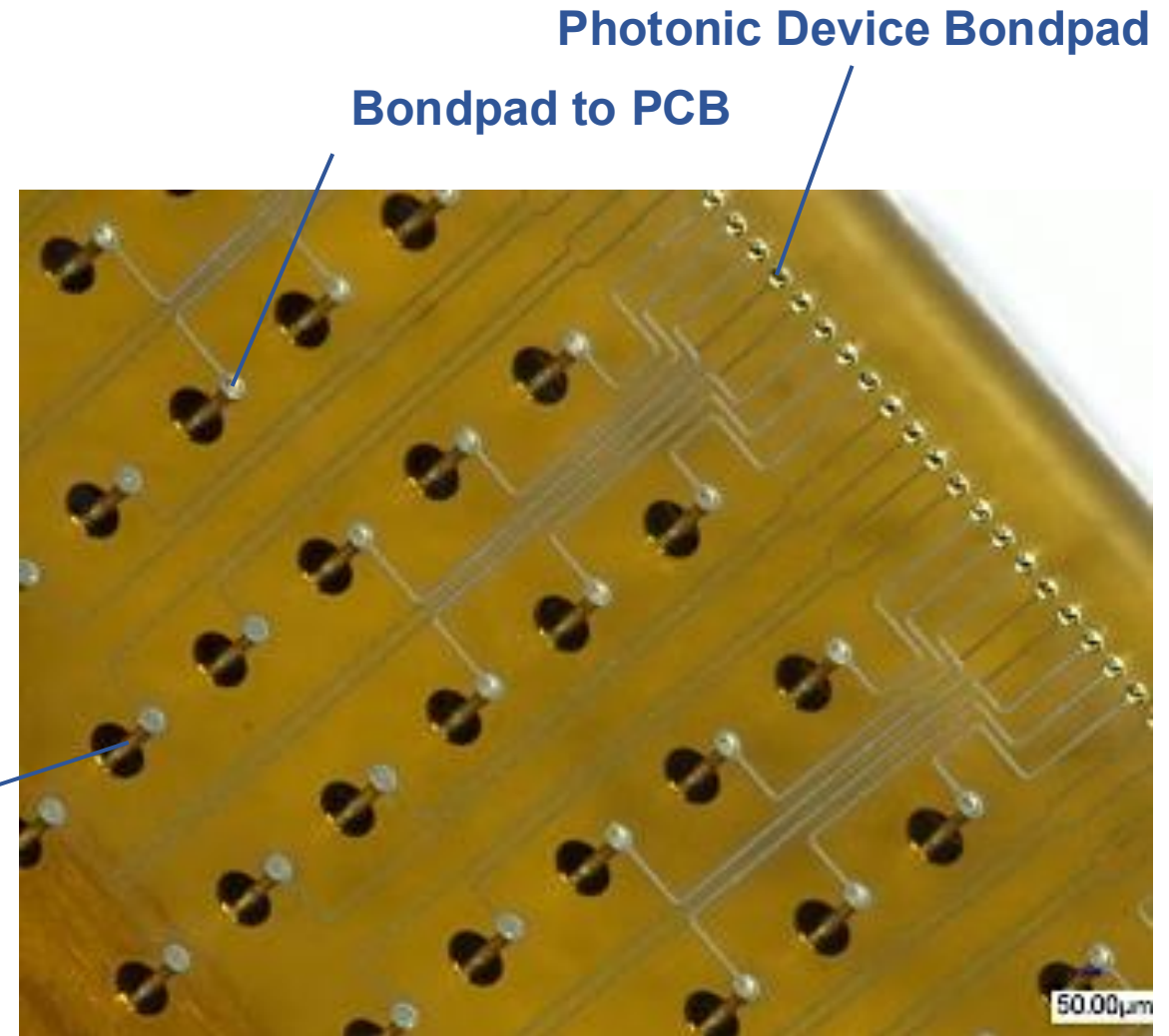
Unit Cell of 128 x 128 Switch



Electrical Packaging (electrical interposers)

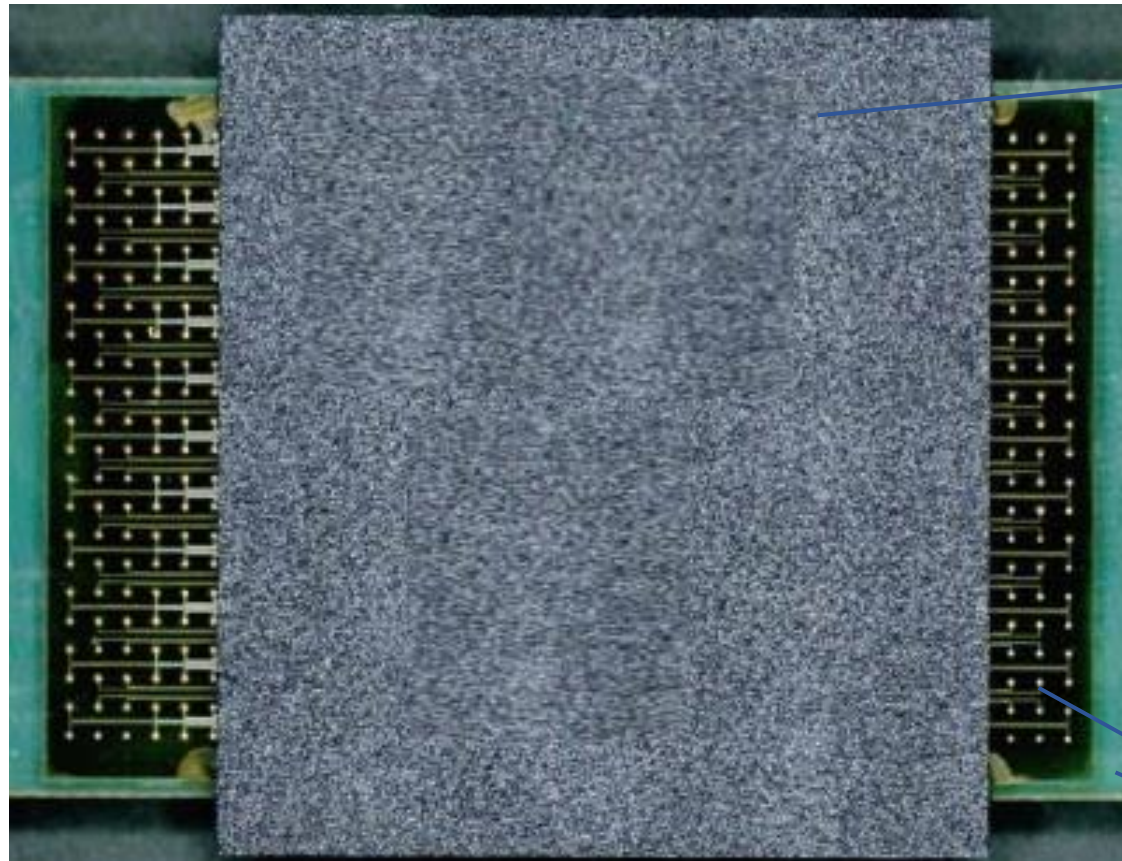


Through Glass Via
(40 μ m)



Photonic Device Bondpad
Bondpad to PCB

Electrical Packaging (electrical interposers)



Photonic Device

50 μ m Solder Ball

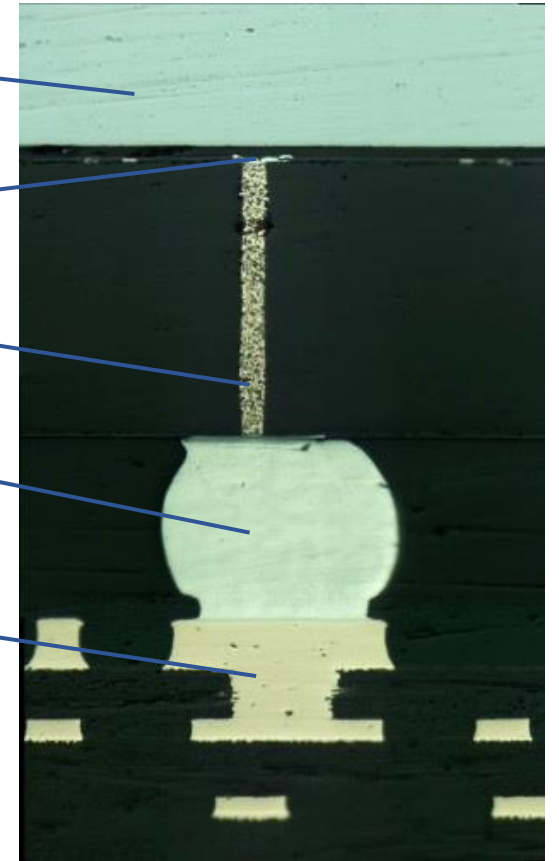
40 μ m TGV

300 μ m Solder Ball

PCB Via

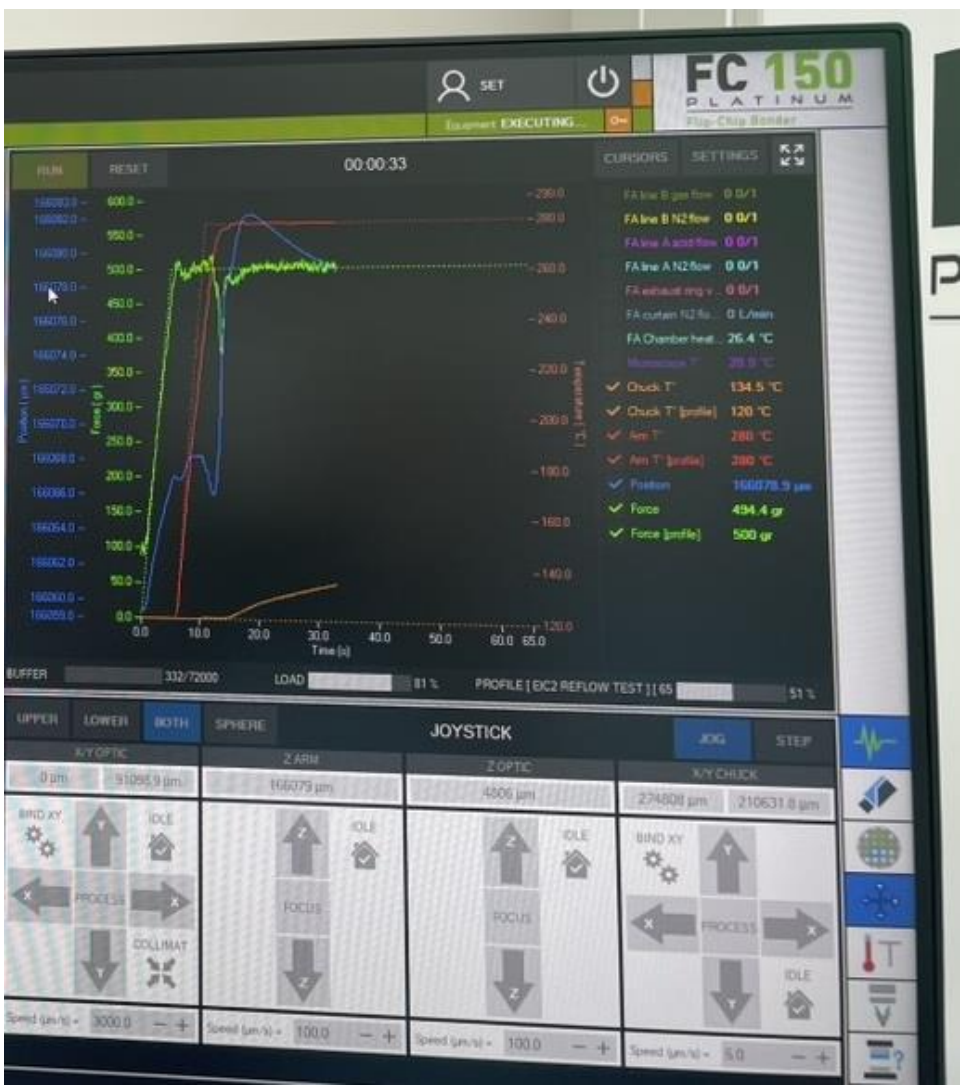
Glass Interposer

PCB



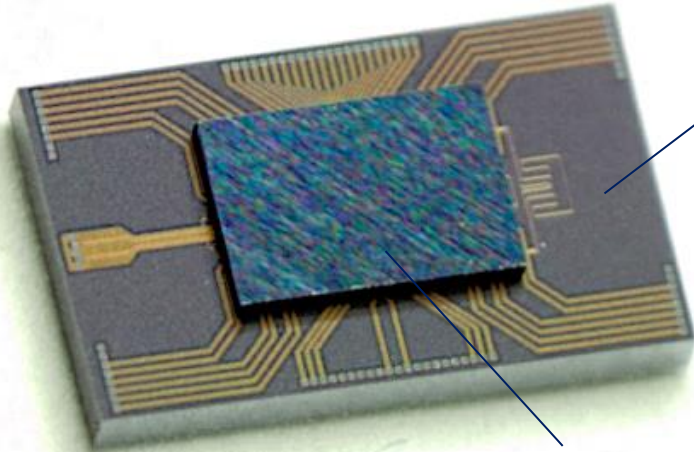
*'Flipchip packaging of digital silicon photonic MEMs switch for cloud computing and data centres
IEEE Photonics, Vol.8 No. 3, 2017.*

Electrical Packaging (flipchip)

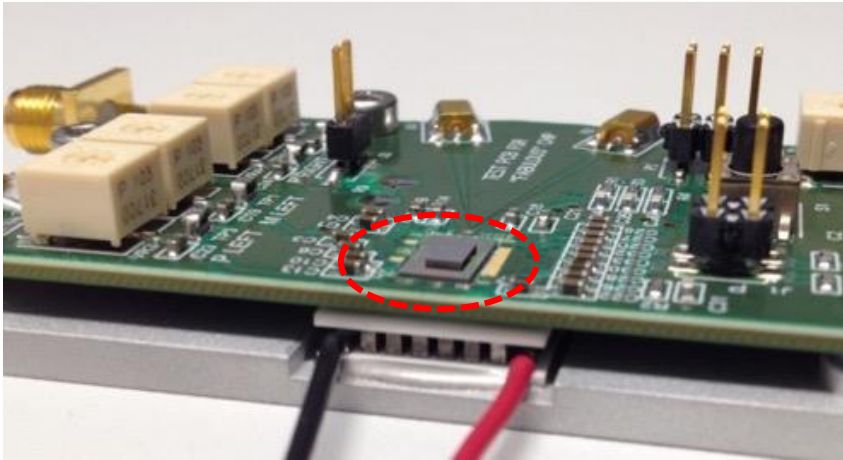


Electrical Packaging (3D integration)

Si-PIC



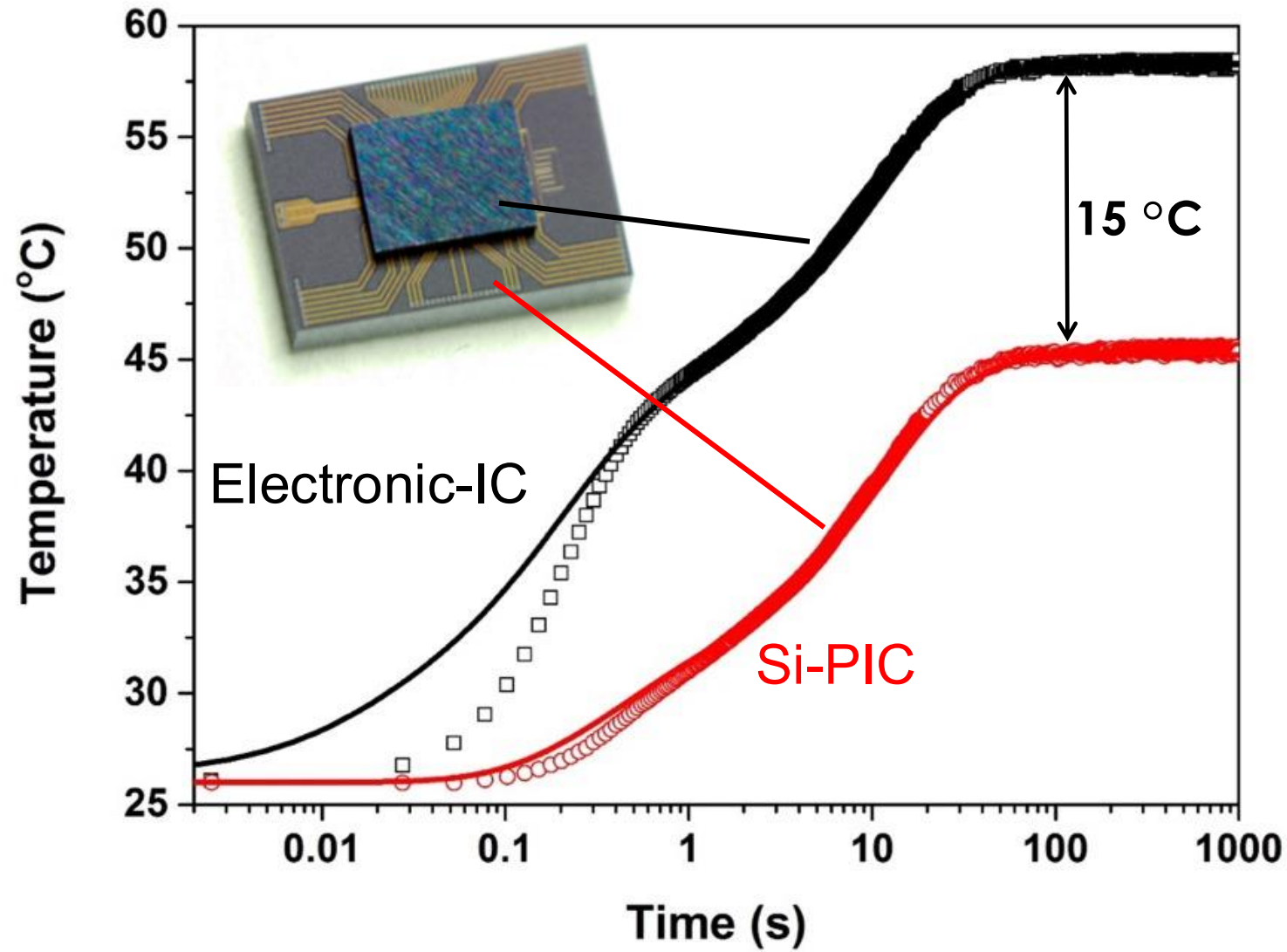
Electronic IC



Demonstration of a partially integrated silicon photonics ONU in a self-coherent reflective FDMA PON, post-deadline paper, ECOC, September 2016.



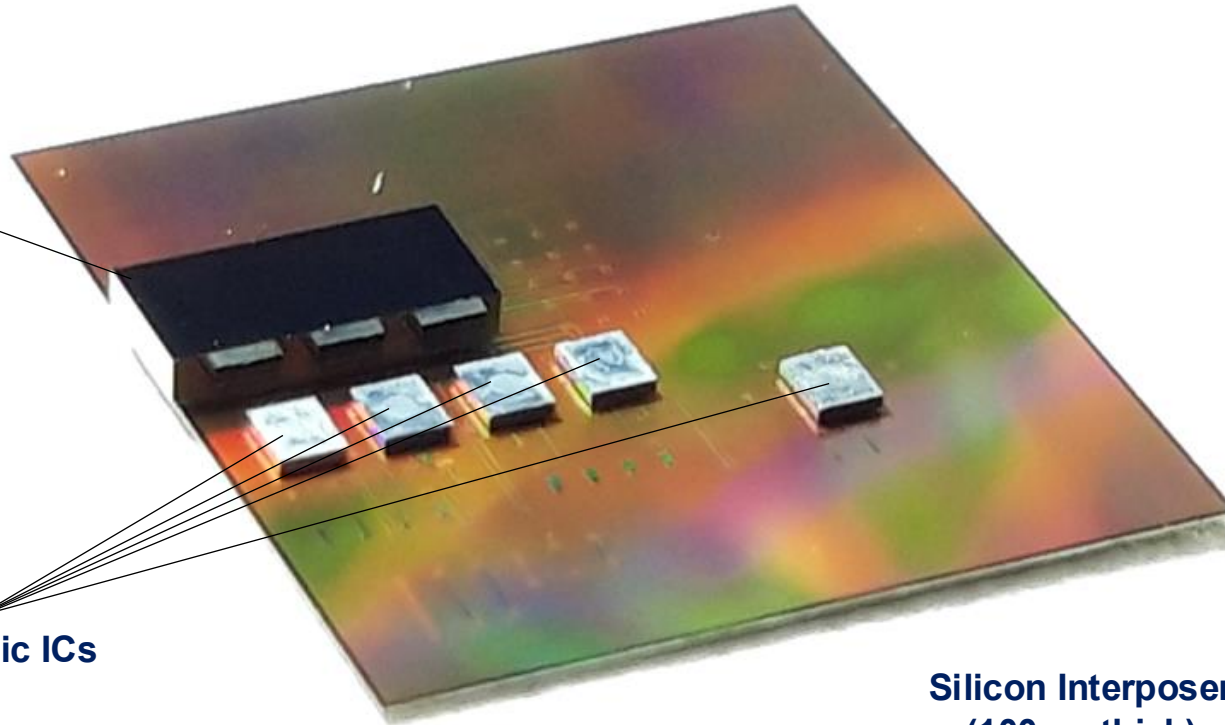
Electrical Packaging (3D integration)



Electrical Packaging (electrical interposers)

Photonic IC

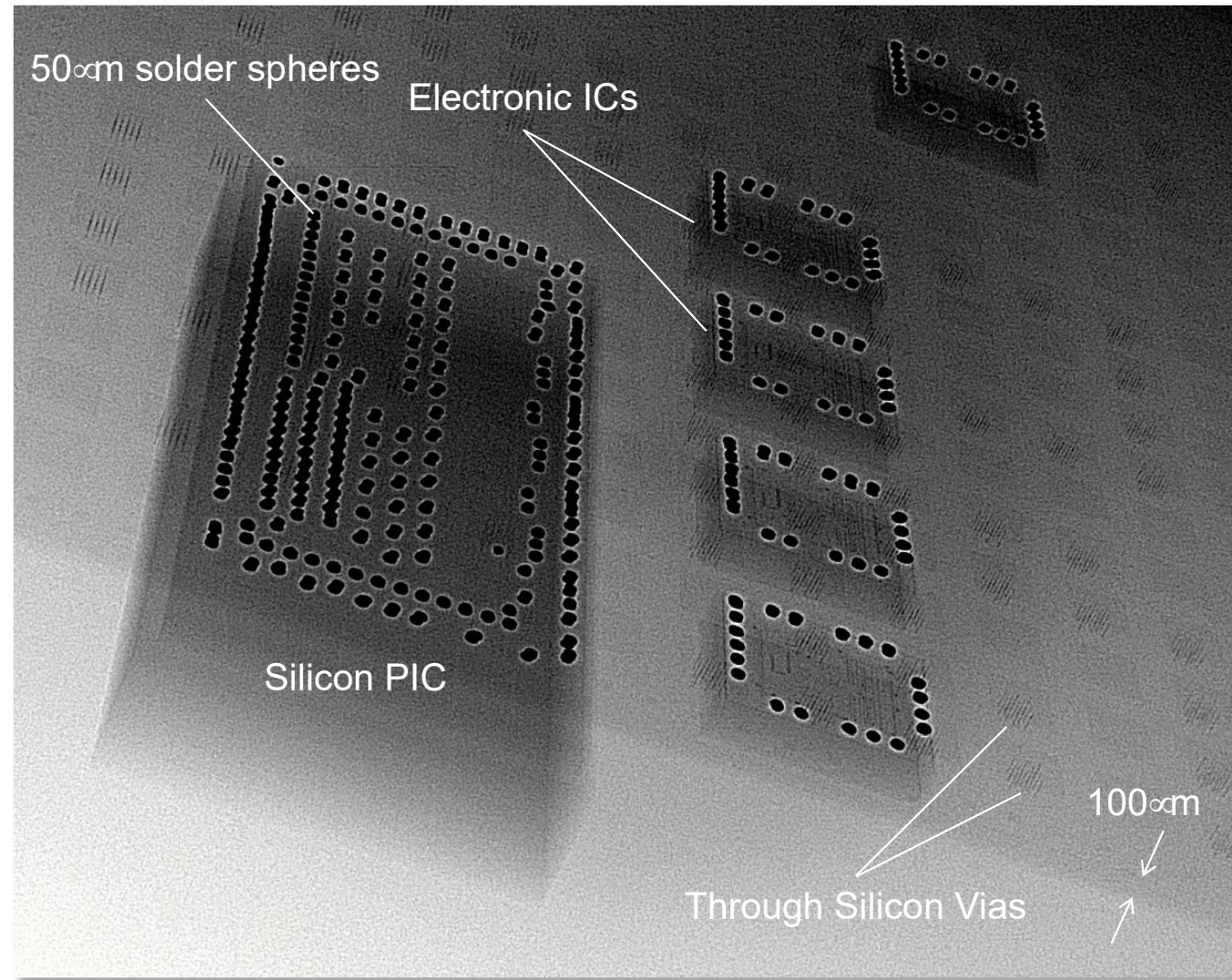
Electronic ICs



Silicon Interposer
(100µm thick)

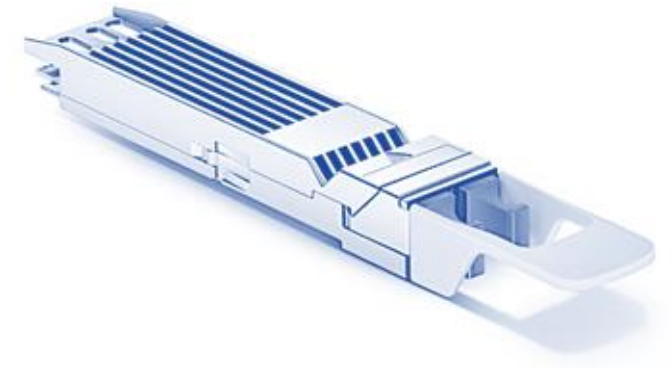
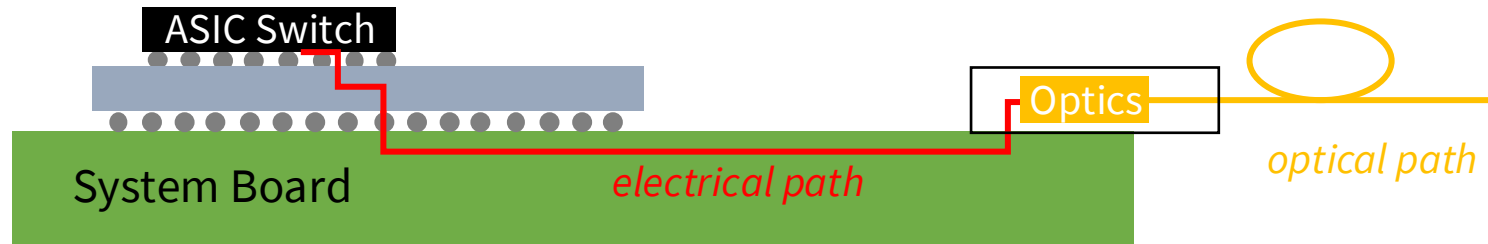


Electrical Packaging (electrical interposers)

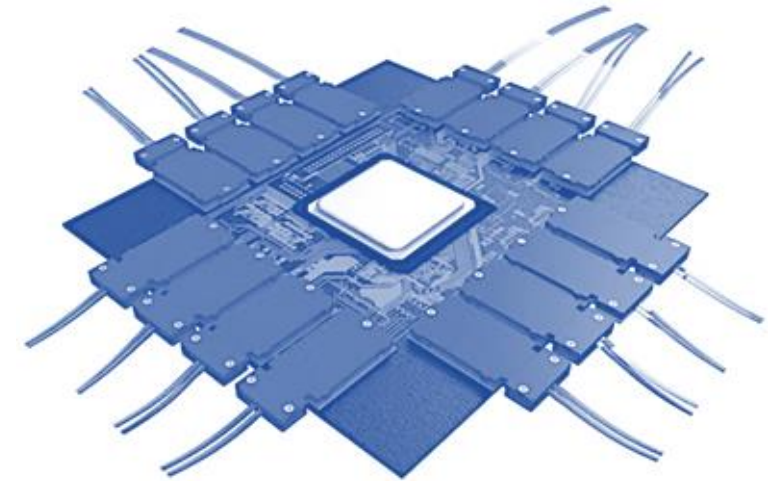


Photonic-Electronic Co-Packaging

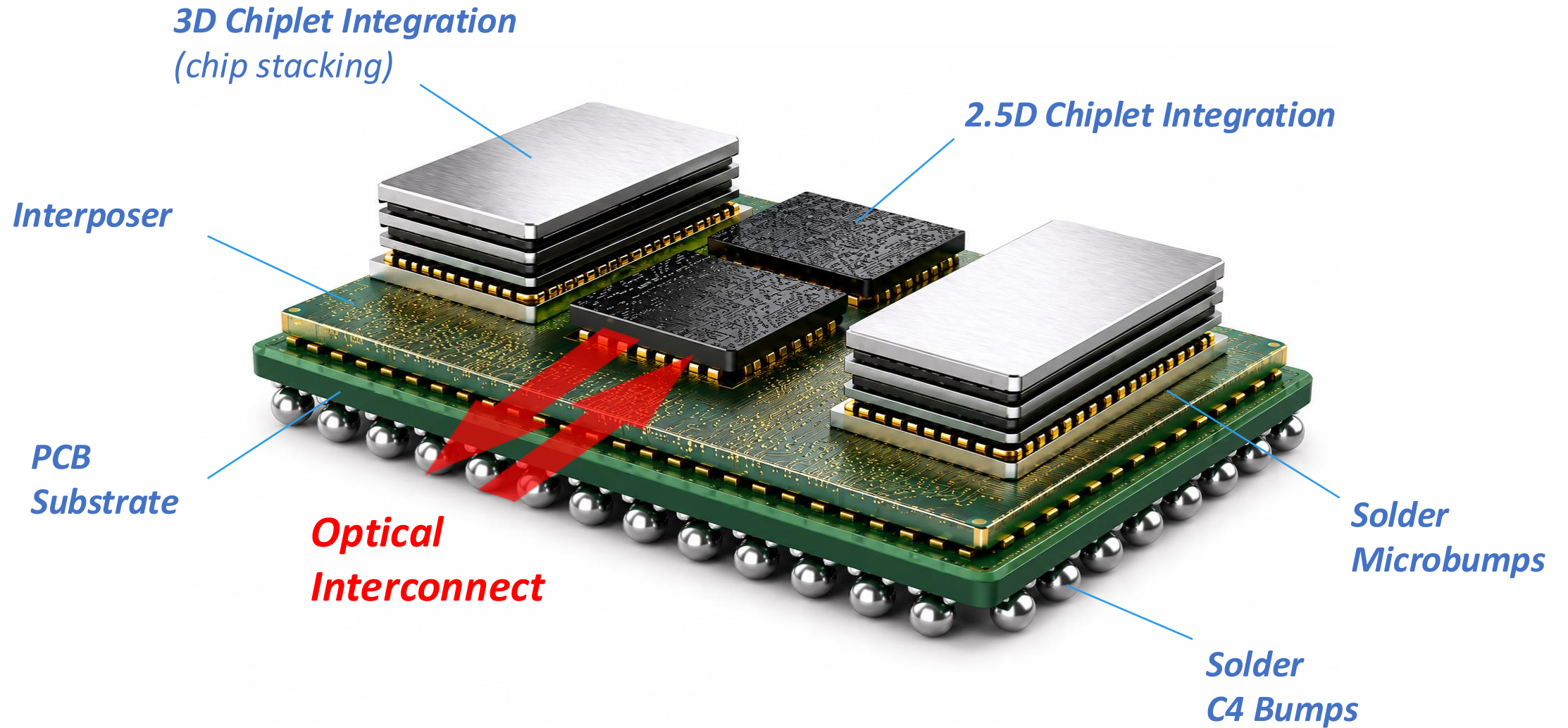
Pluggable Transceiver Optics



Co-Packaged Optics



Photonic-Electronic Co-Packaging



Advanced Packaging, Chiplets & Interposers



Silicon

- High-density integration with ultra-fine-pitch wiring, micro-bumps and TSVs
- Low CTE well-matched to photonic and electronic chips
- More expensive than other interposer technologies



Glass

- High-density integration with fine-pitch wiring, micro-bumps and TSVs
- Ultra-low Rf, electrical loss and low CTE well-matched to photonic and electronic chips
- Processed in large panels for low cost manufacturing



Ceramic

- High thermal conductivity, low CTE and high reliability (e.g. space applications)
- Lower wiring density than silicon or glass
- Relatively expensive manufacturing solution



Organic

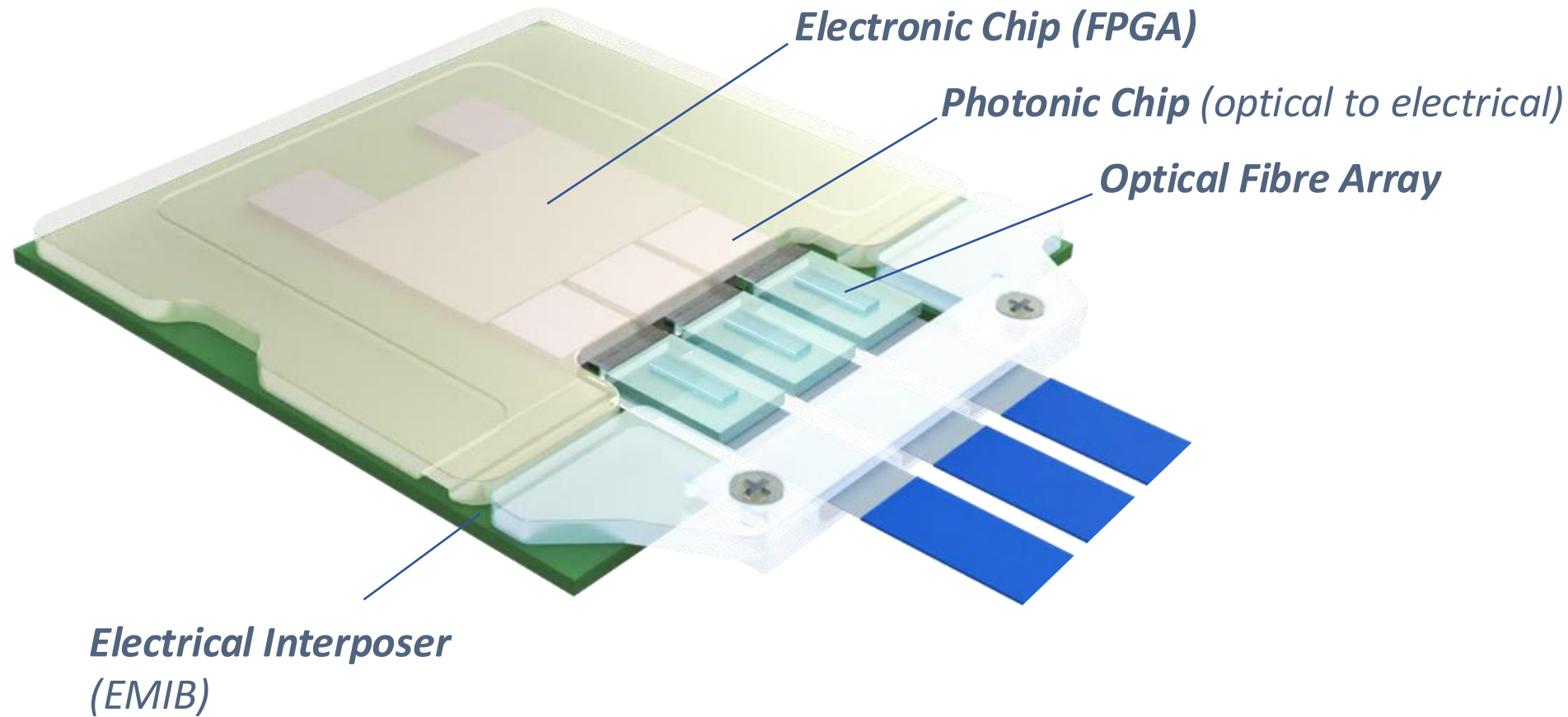
- Lower wiring density than silicon or glass
- High CTE and prone to significant warpage issues
- Processed in large panels for very low cost manufacturing



Hybrid

- Combines silicon, glass or ceramic with glass or organic substrates for coarse routing
- High CTE with warpage issues
- Lower cost solution than silicon or glass

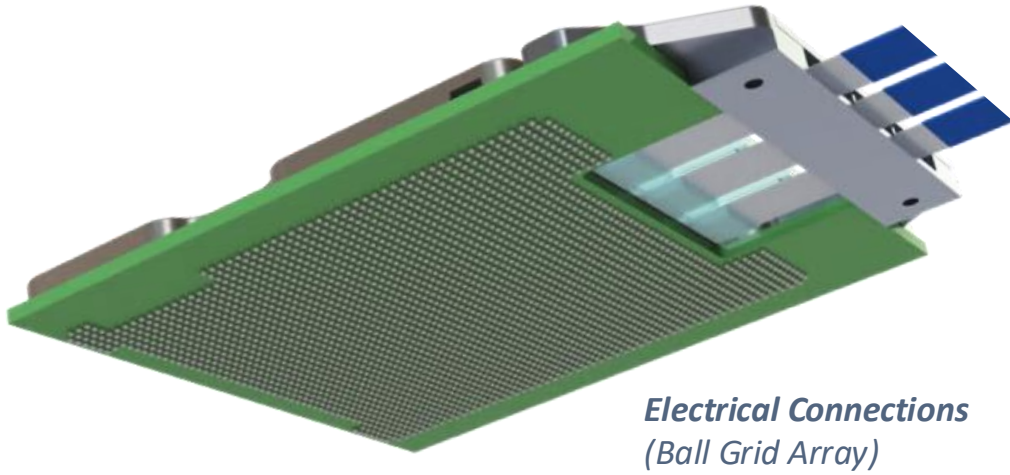
Photonic-Electronic Co-Packaging



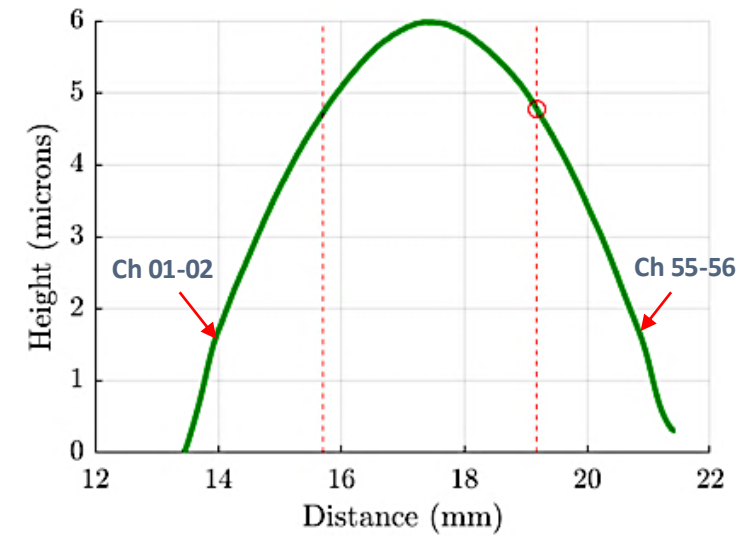
Innovations in fibre array coupling and integration for high-bandwidth FPGA multichip packages, Matthew Hall, SPIE Photonics West, January 2025.



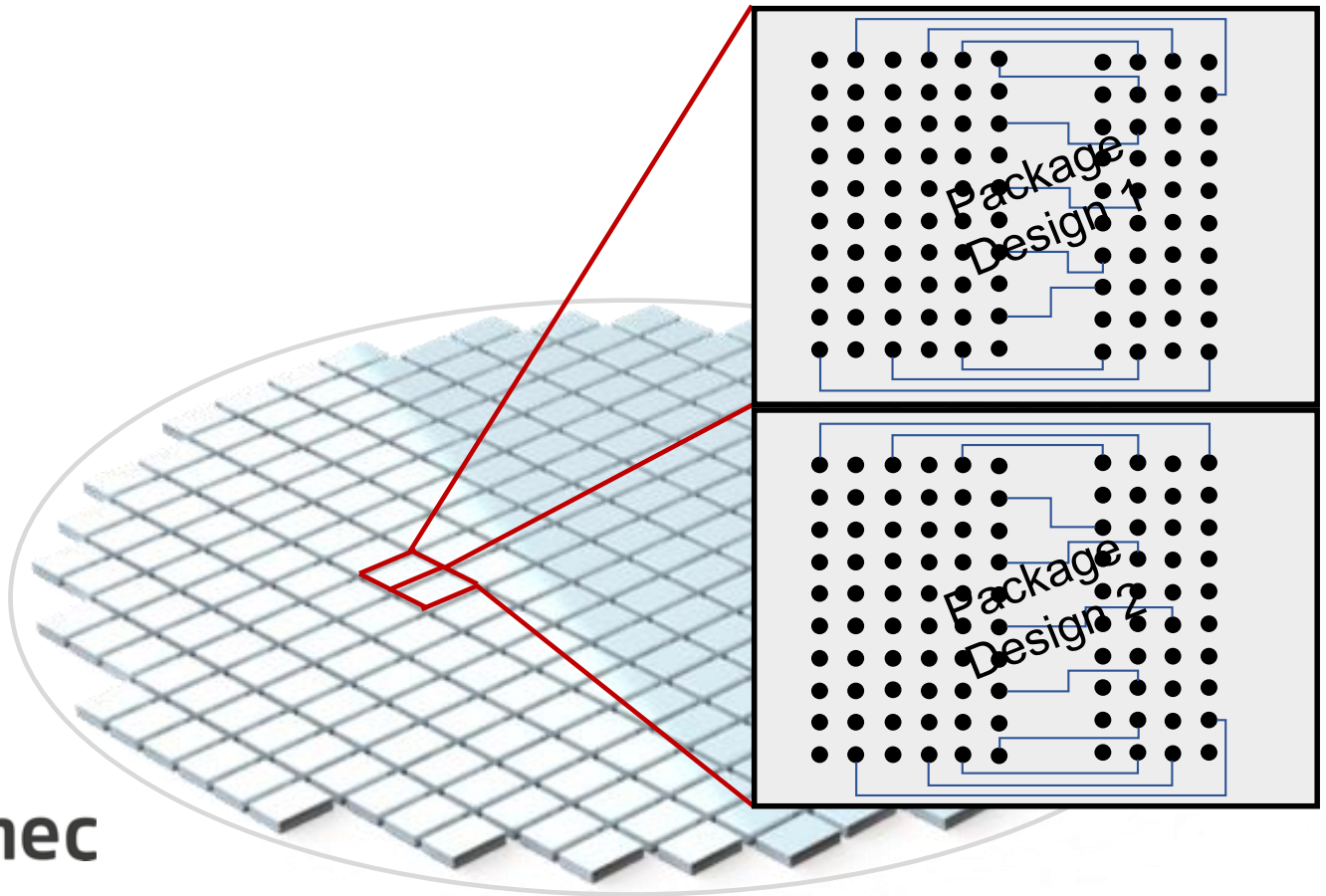
Photonic-Electronic Co-Packaging



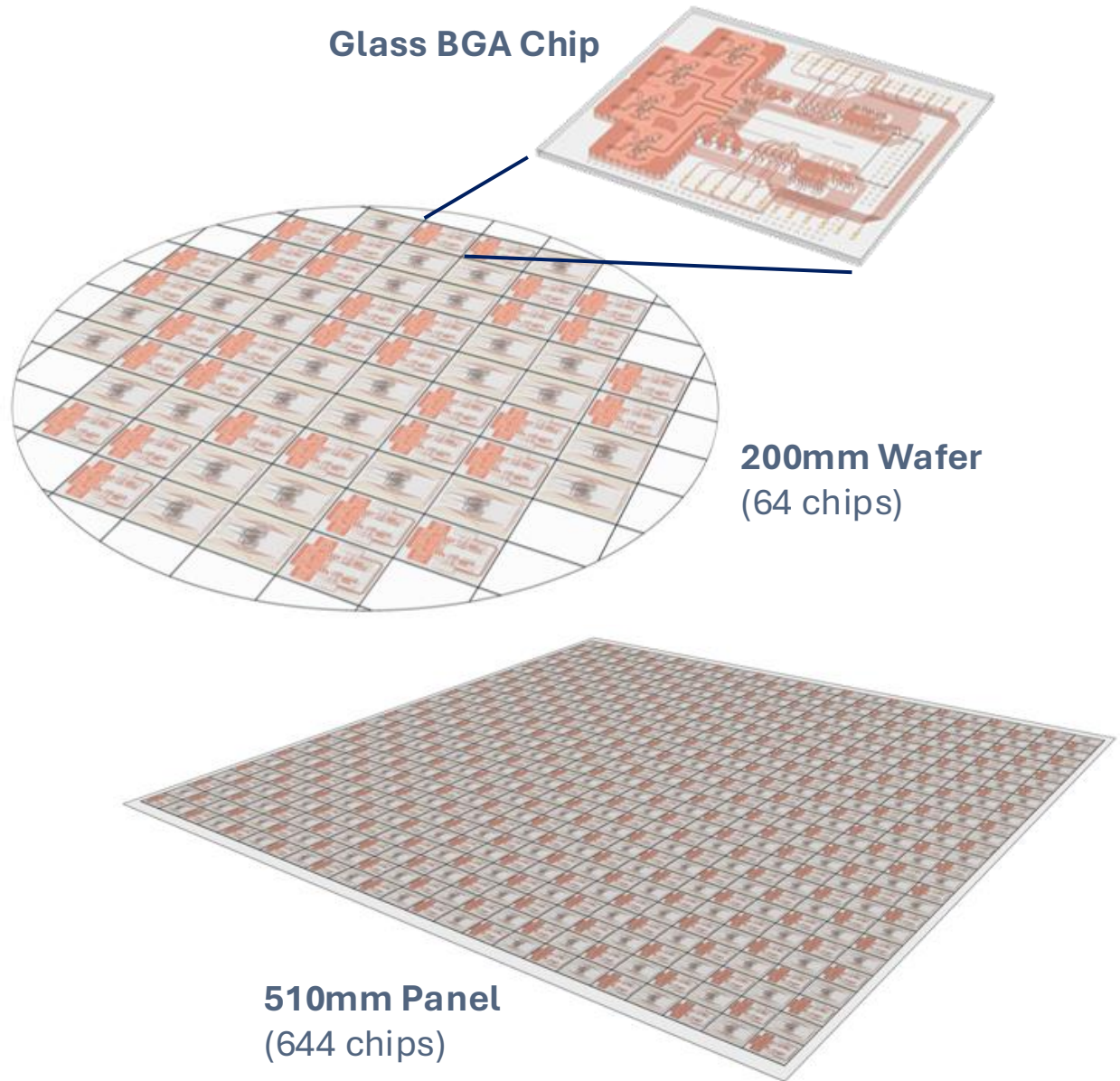
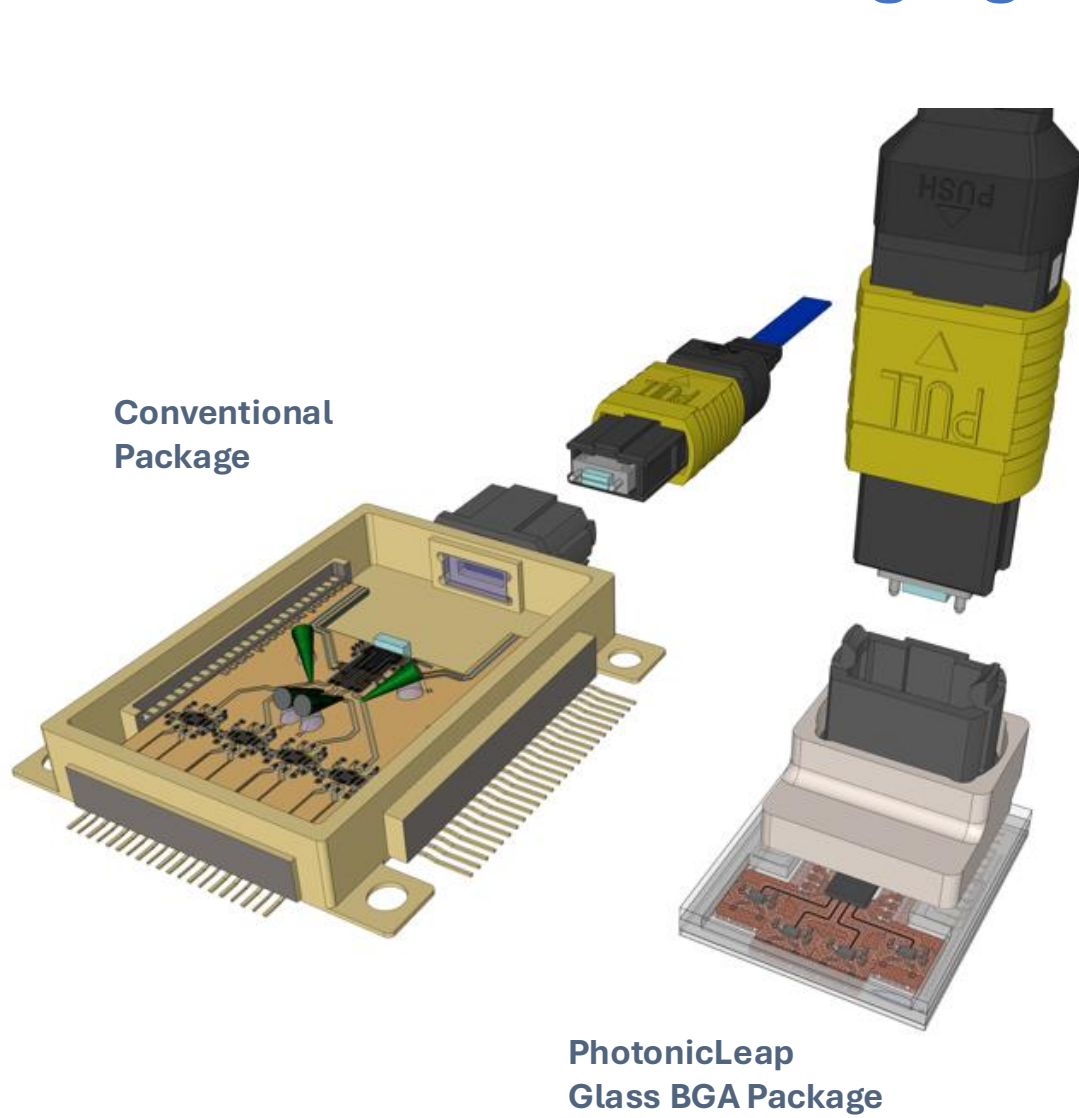
Innovations in fibre array coupling and integration for high-bandwidth FPGA multichip packages, SPIE Photonics West, January 2025.



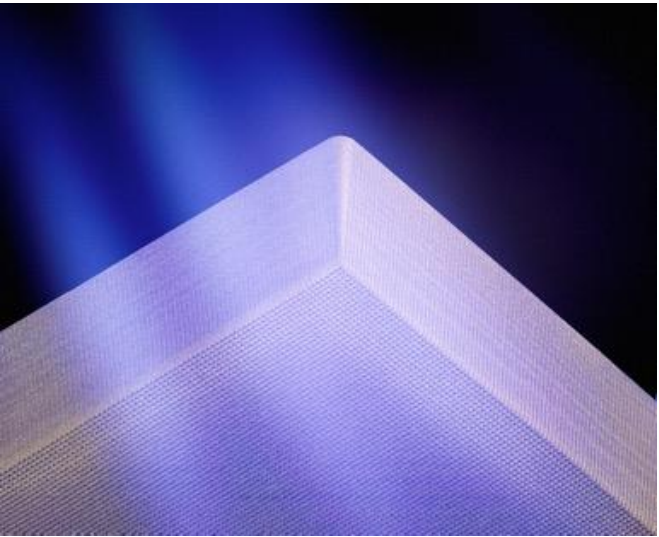
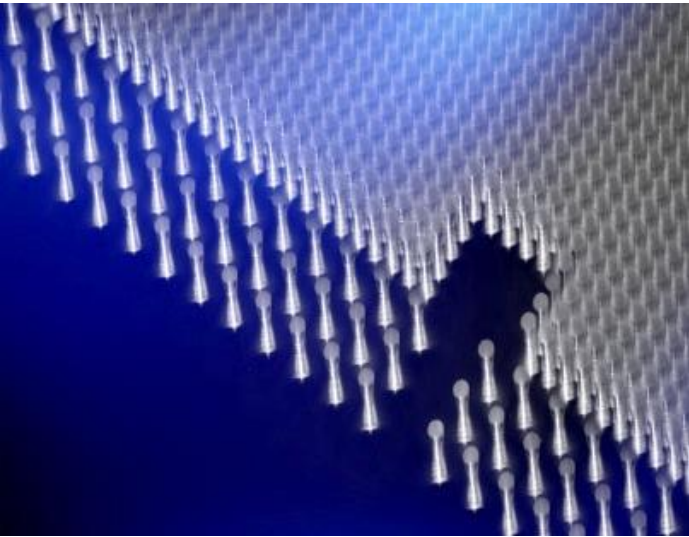
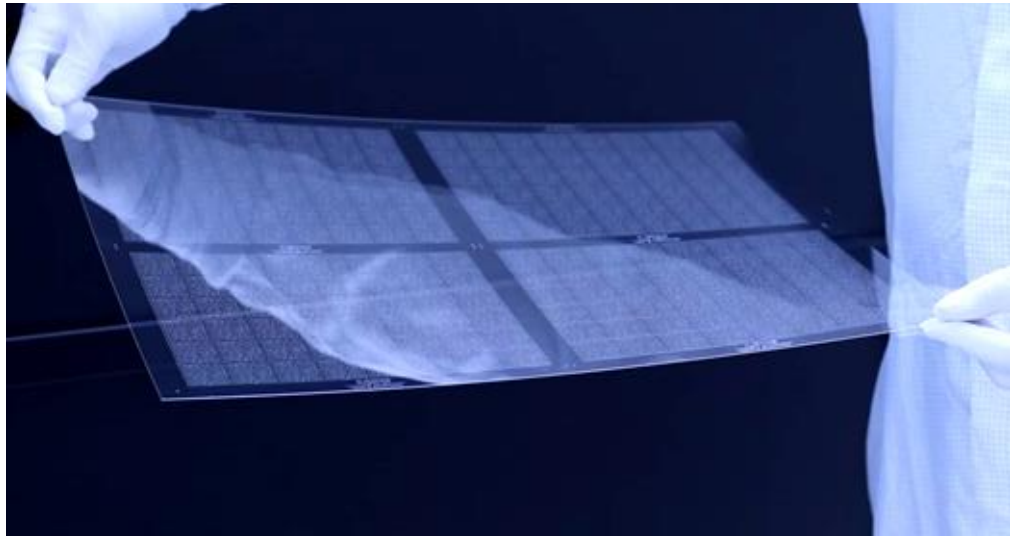
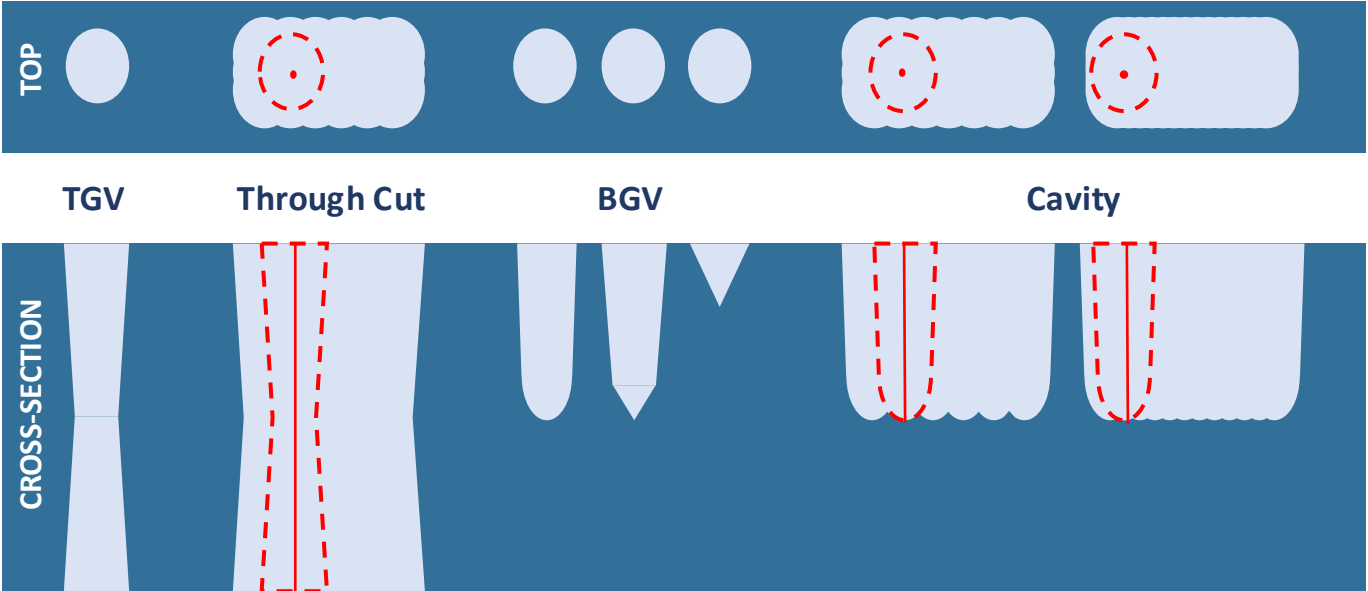
Glass Wafer-Level Packaging



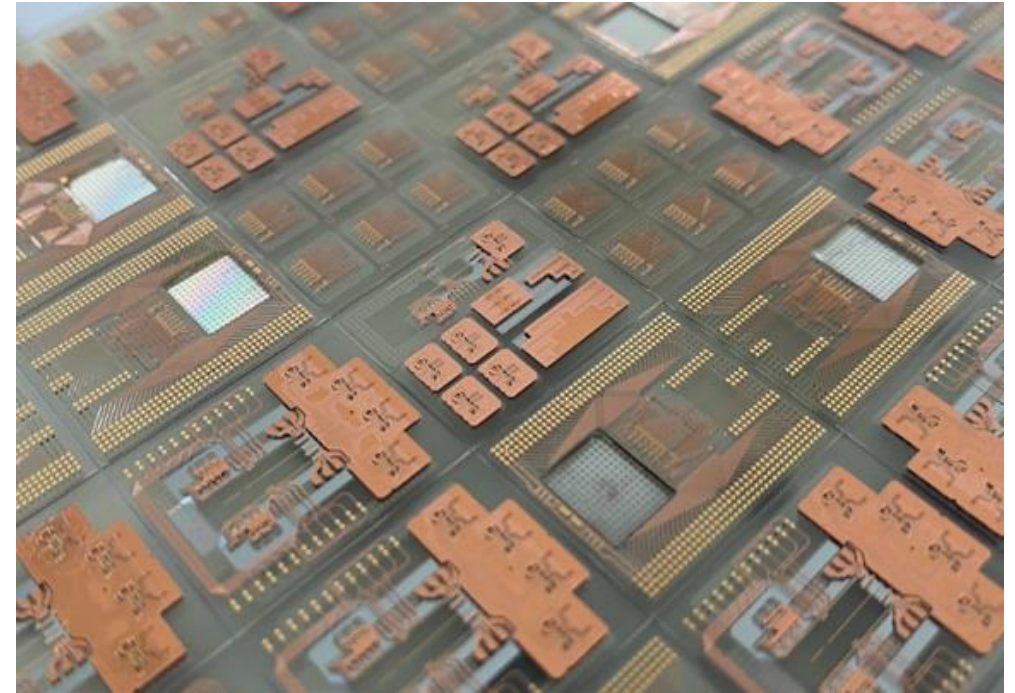
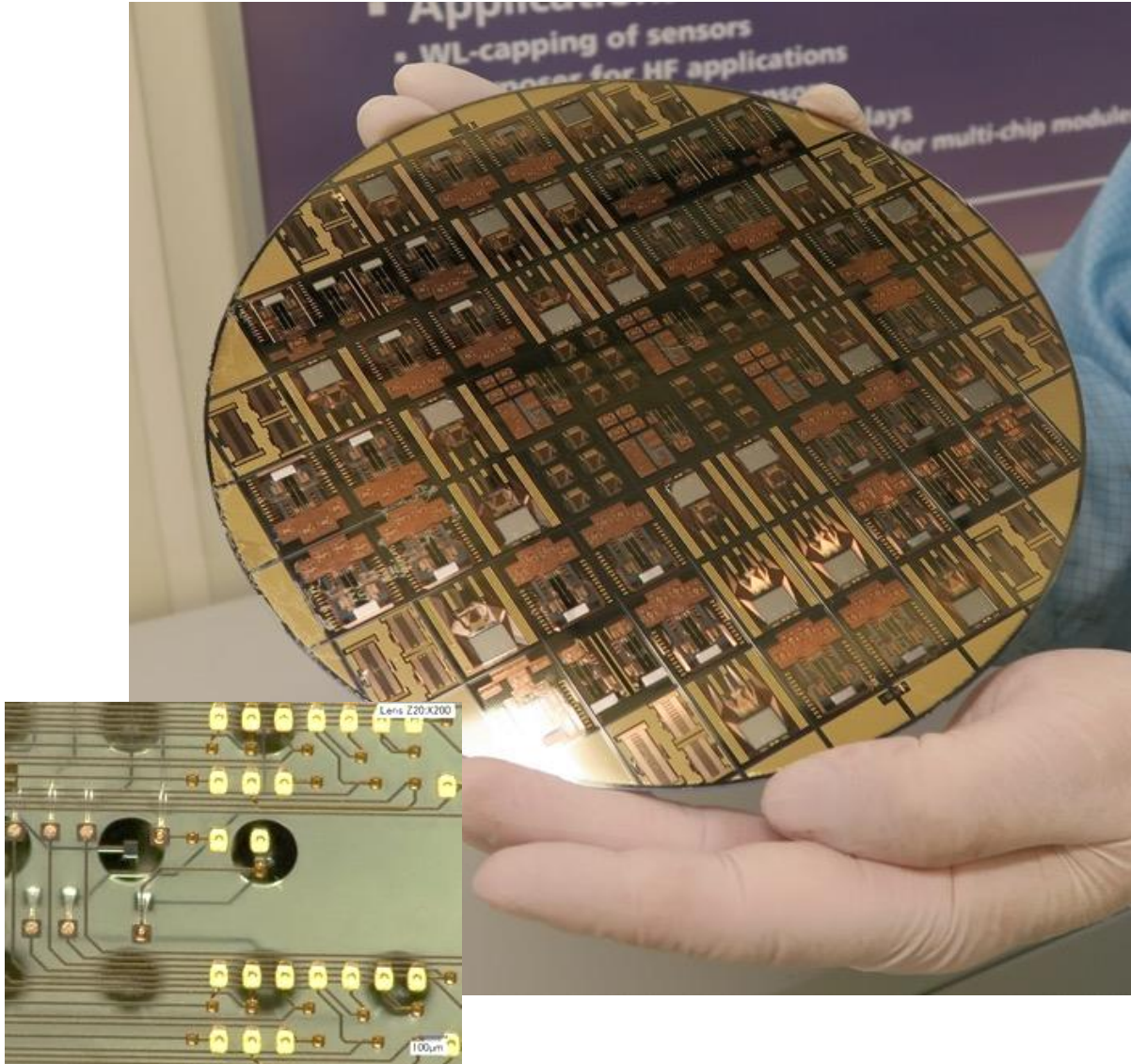
Glass Wafer-Level Packaging



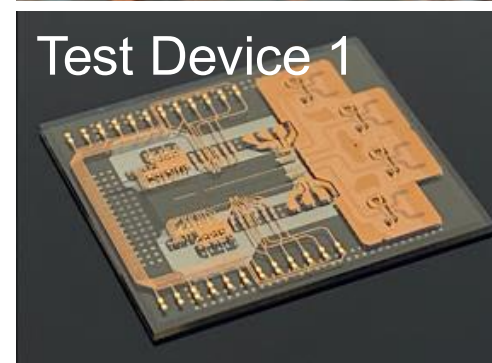
Glass Wafer-Level Packaging



Glass Wafer-Level Packaging



Test Device 1



Test Device 2

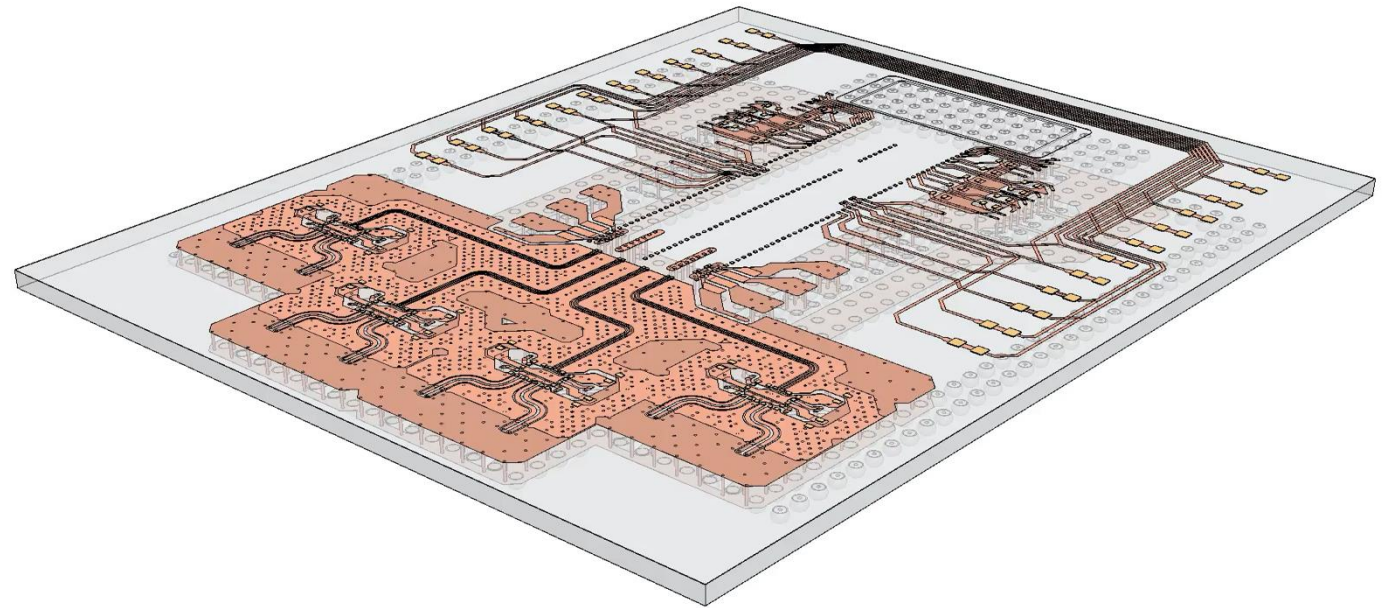


Glass Wafer-Level Packaging

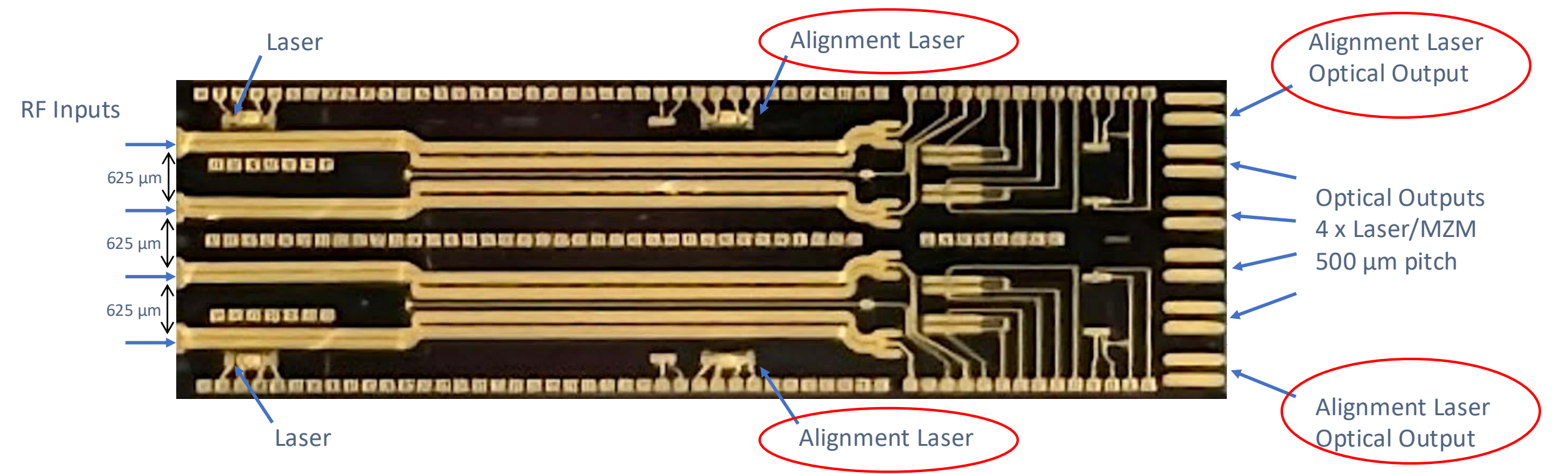
InP PIC

cavity in glass substrate

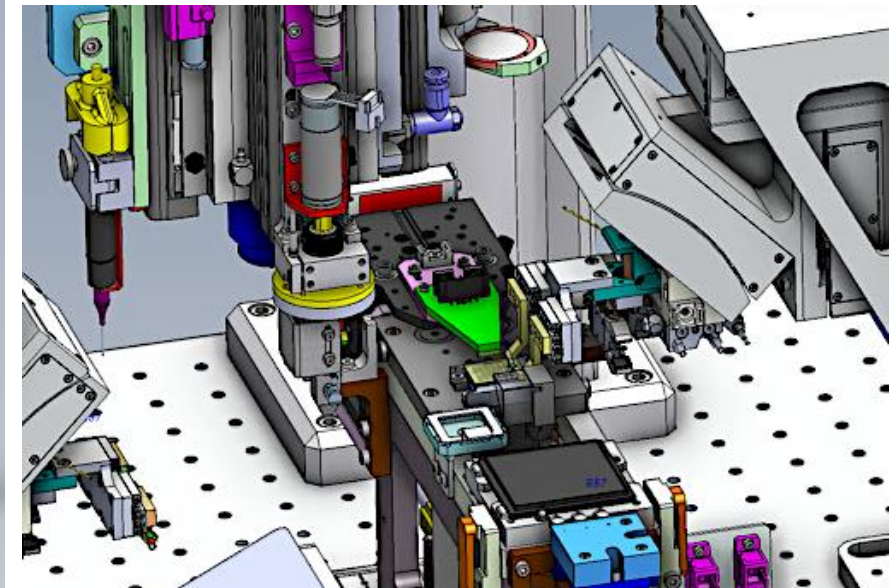
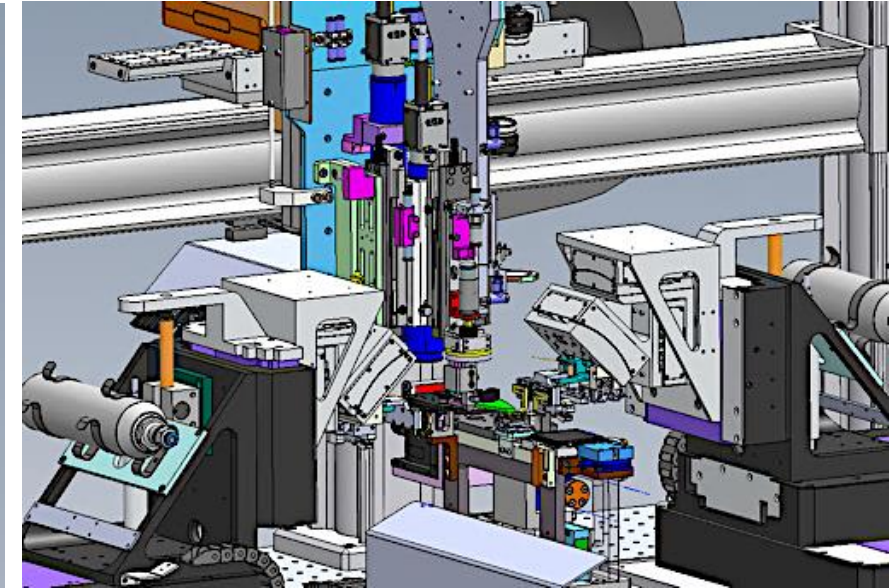
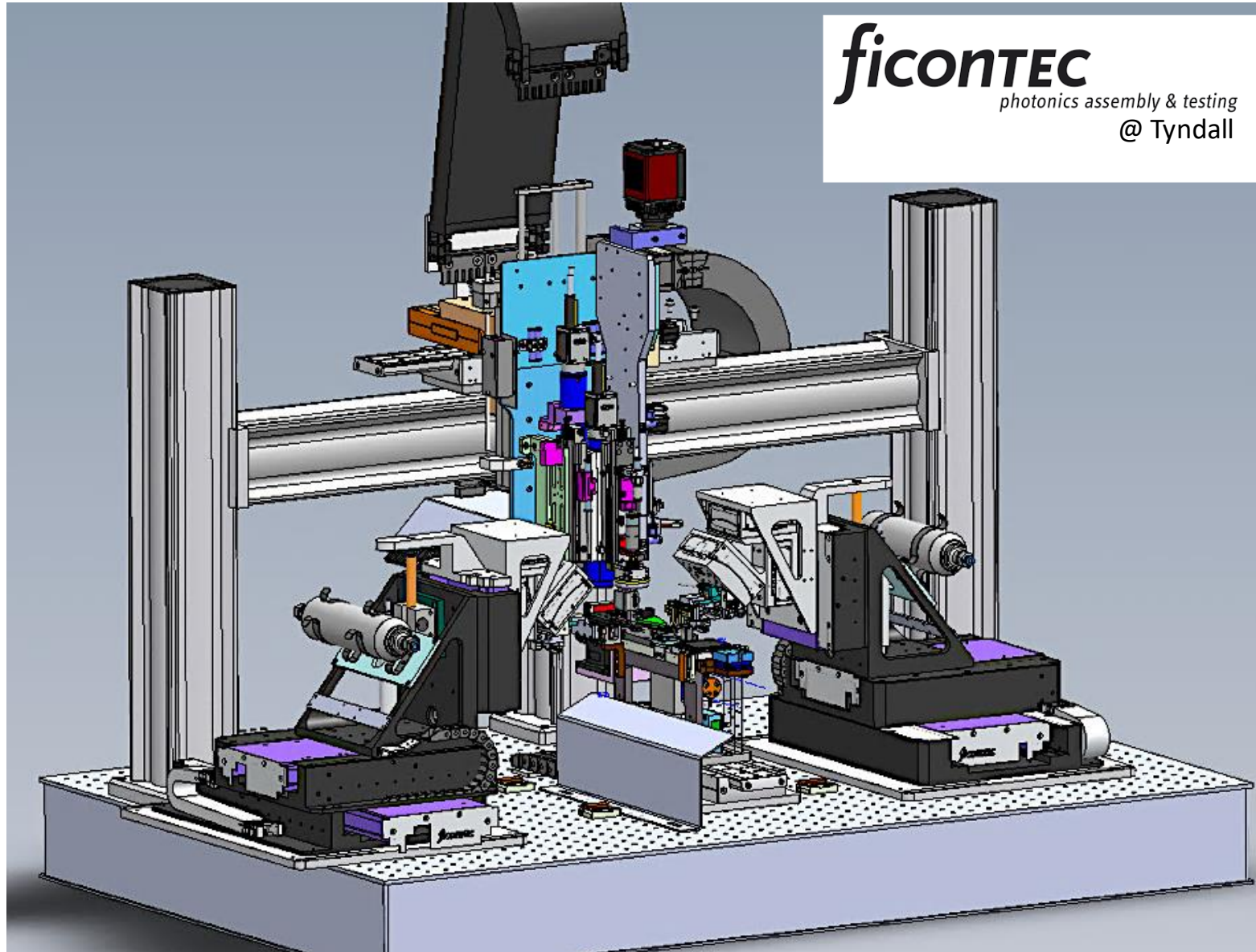
*Glass Interposer
(BGA connections)*



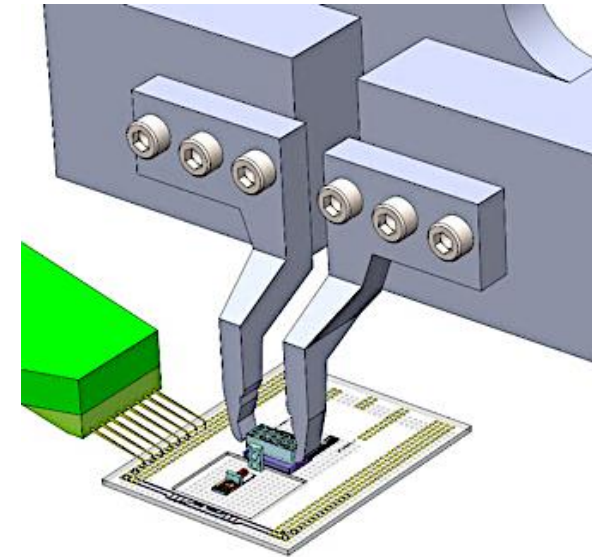
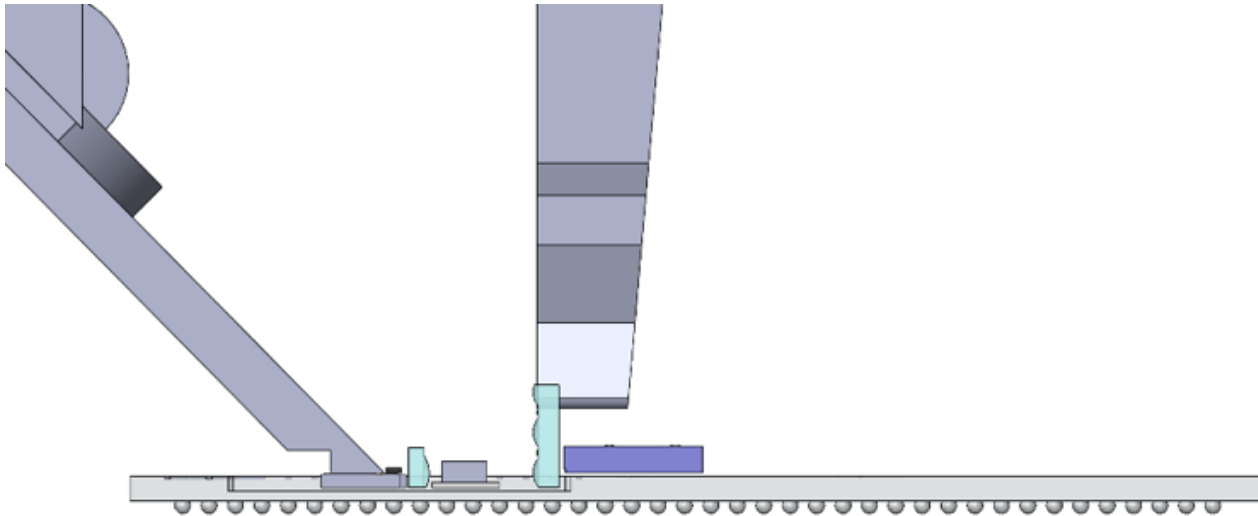
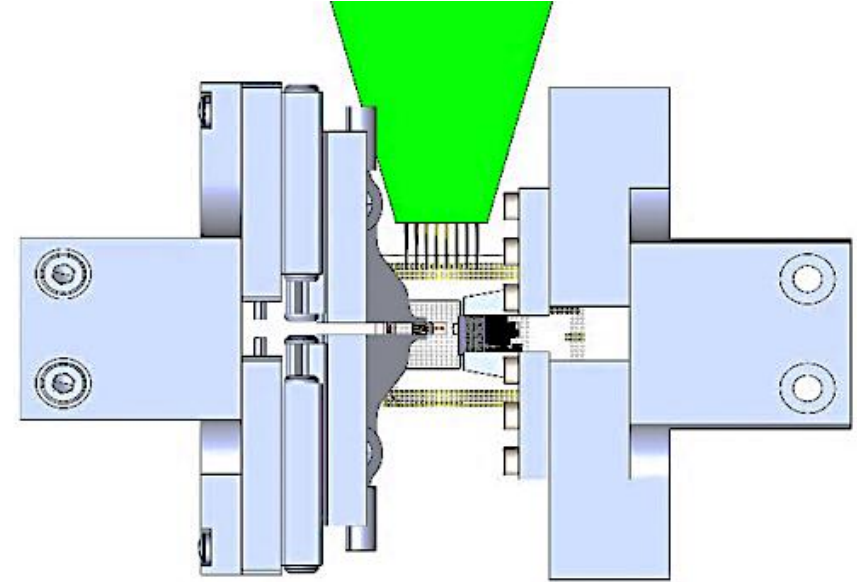
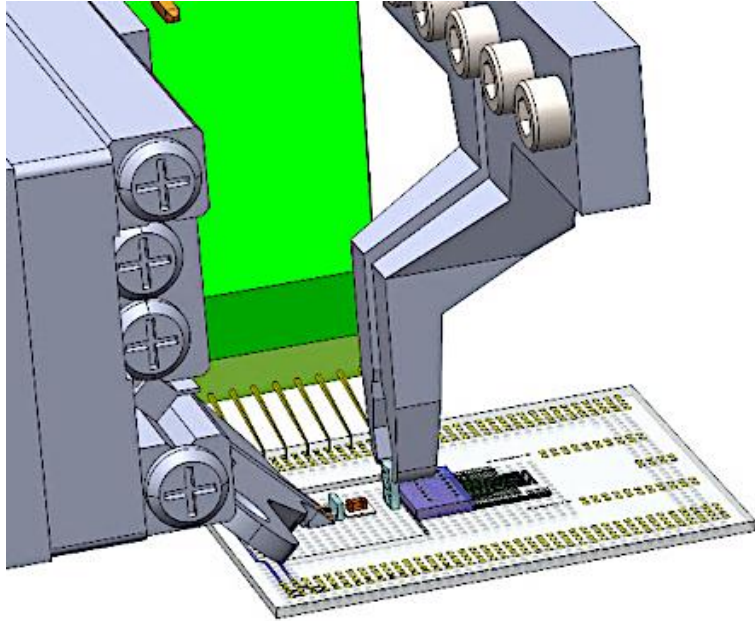
Glass Wafer-Level Packaging



Glass Wafer-Level Packaging



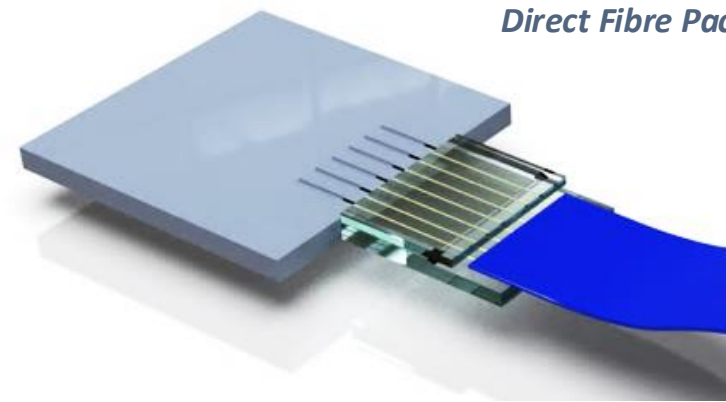
Glass Wafer-Level Packaging



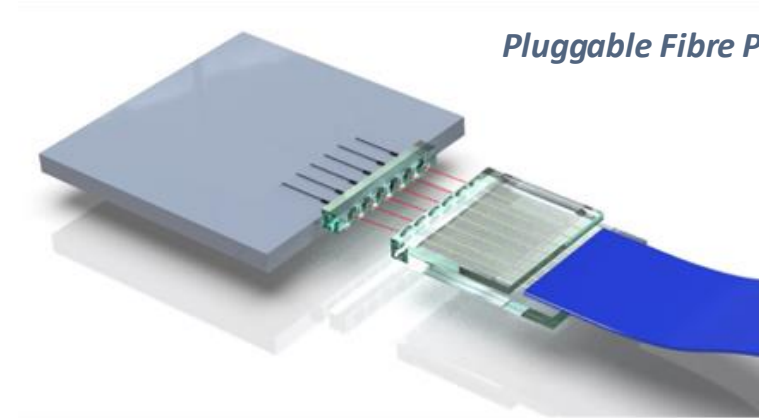
Glass Wafer-Level Packaging



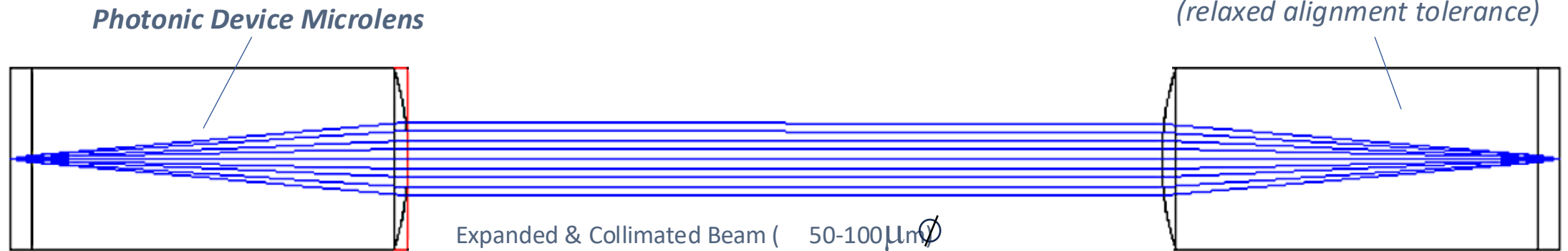
Glass Wafer-Level Packaging



Direct Fibre Packaging

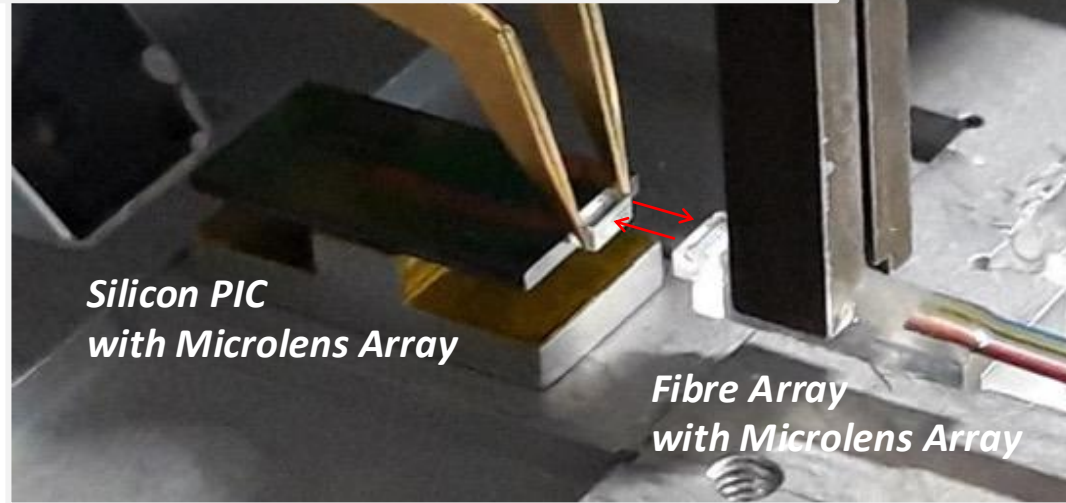
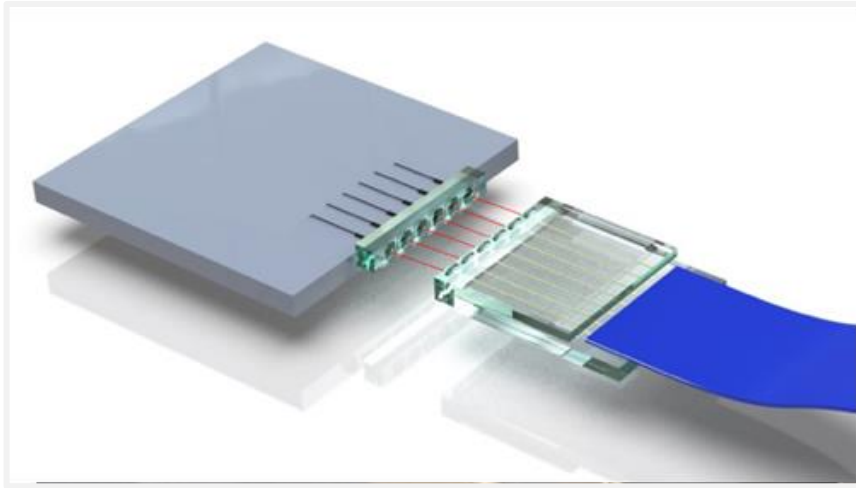


Pluggable Fibre Packaging



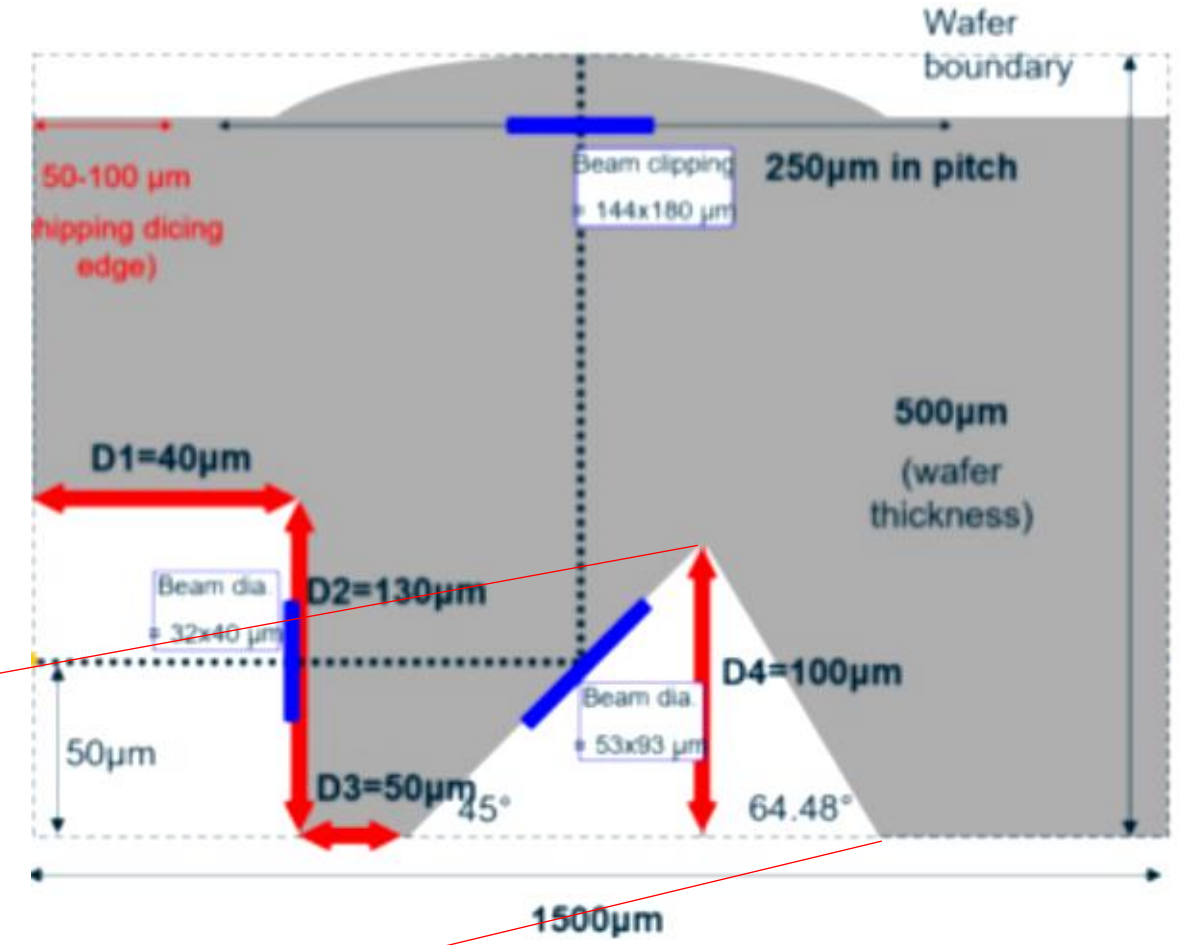
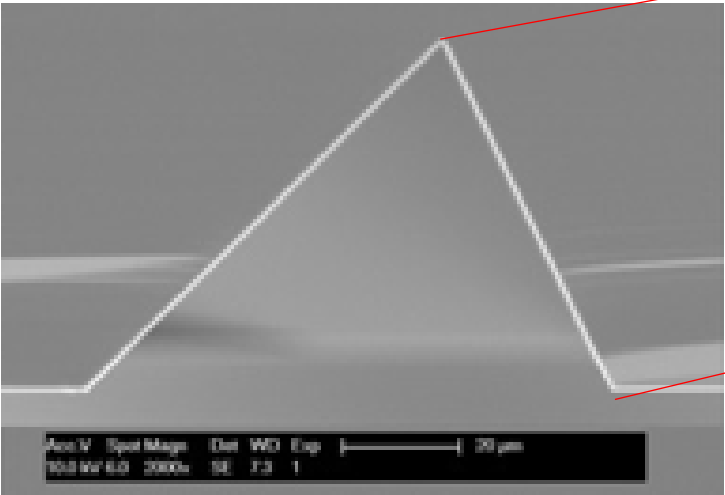
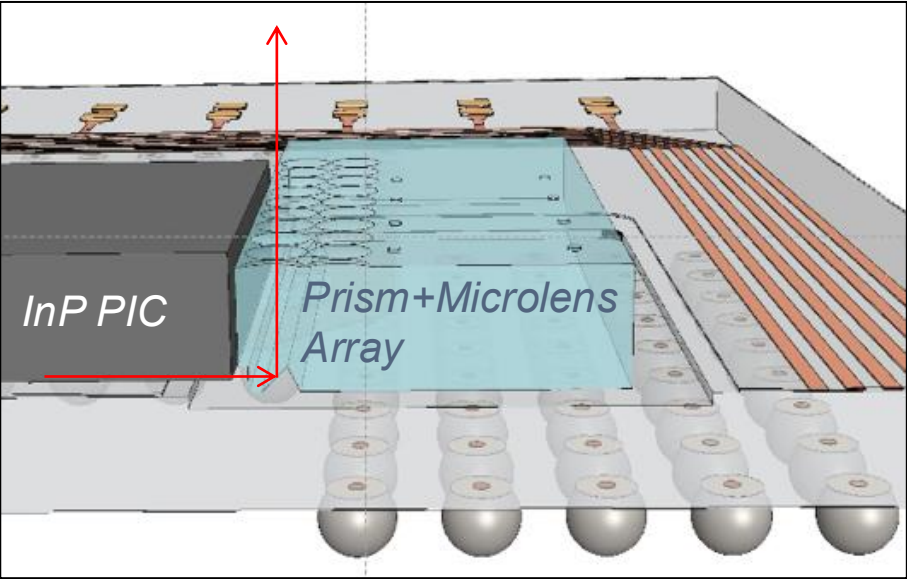
'Pluggable single-mode fiber-array-to-PIC coupling using micro-lenses' IEEE Photon. Tech. Letters, 2017.

Glass Wafer-Level Packaging

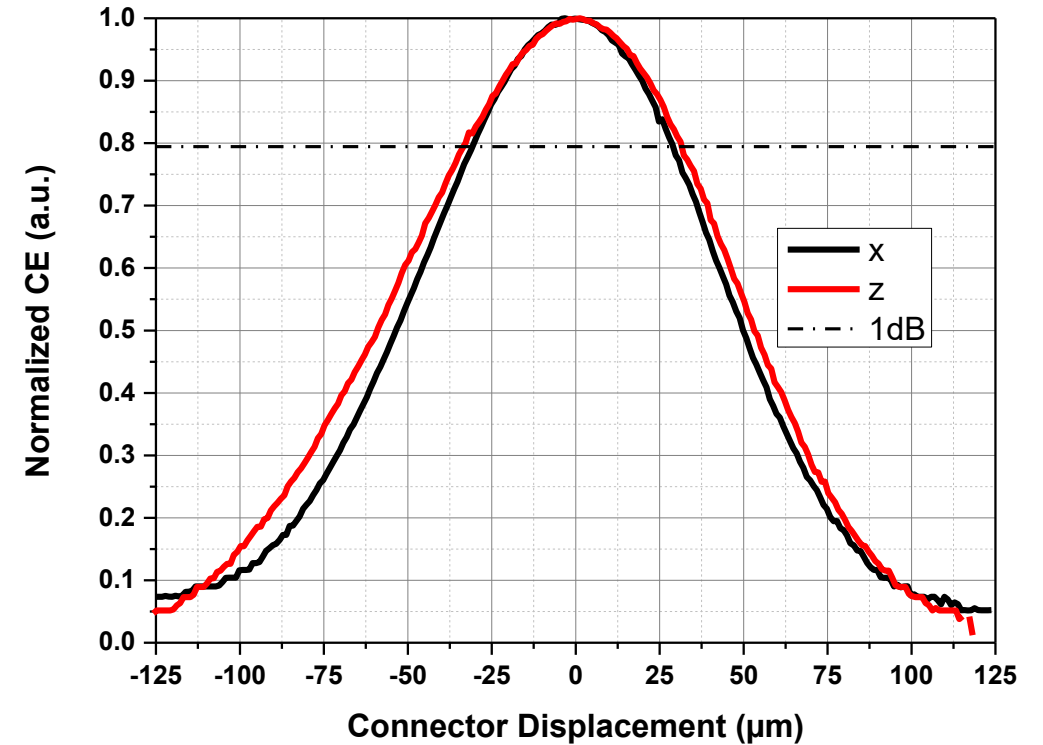
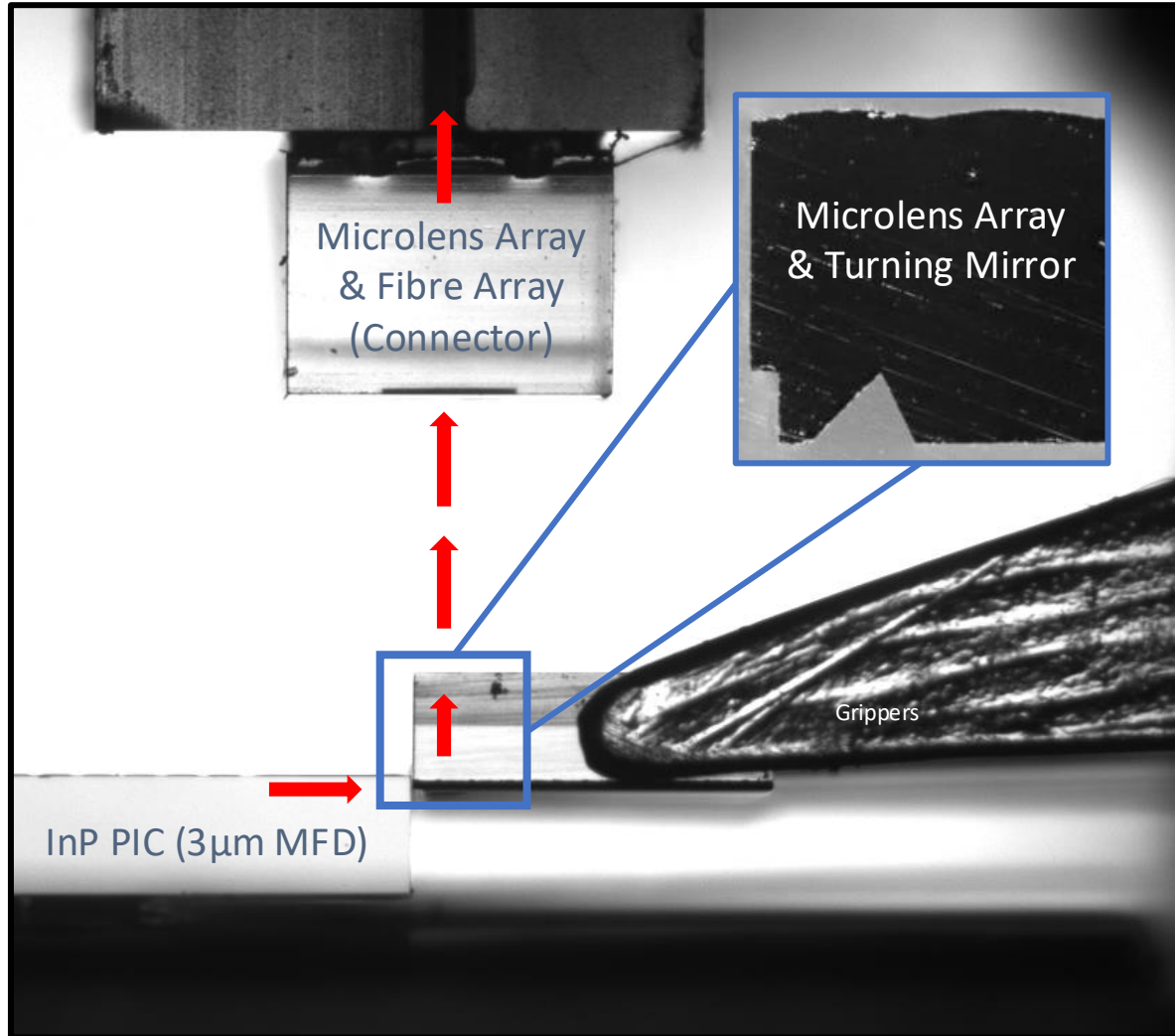


‘Demonstration of Single-Mode Expanded Beam Connectorised Module for Photonic Integrated Circuits’ IEEE, Journal of Lightwave Technology, 2023.

Glass Wafer-Level Packaging



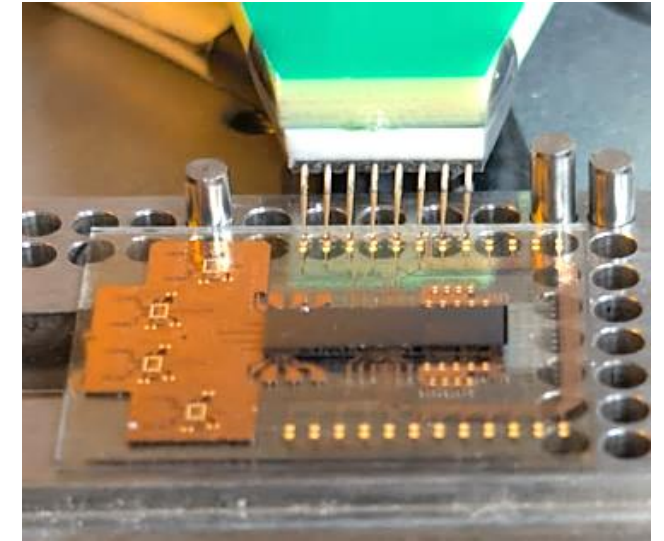
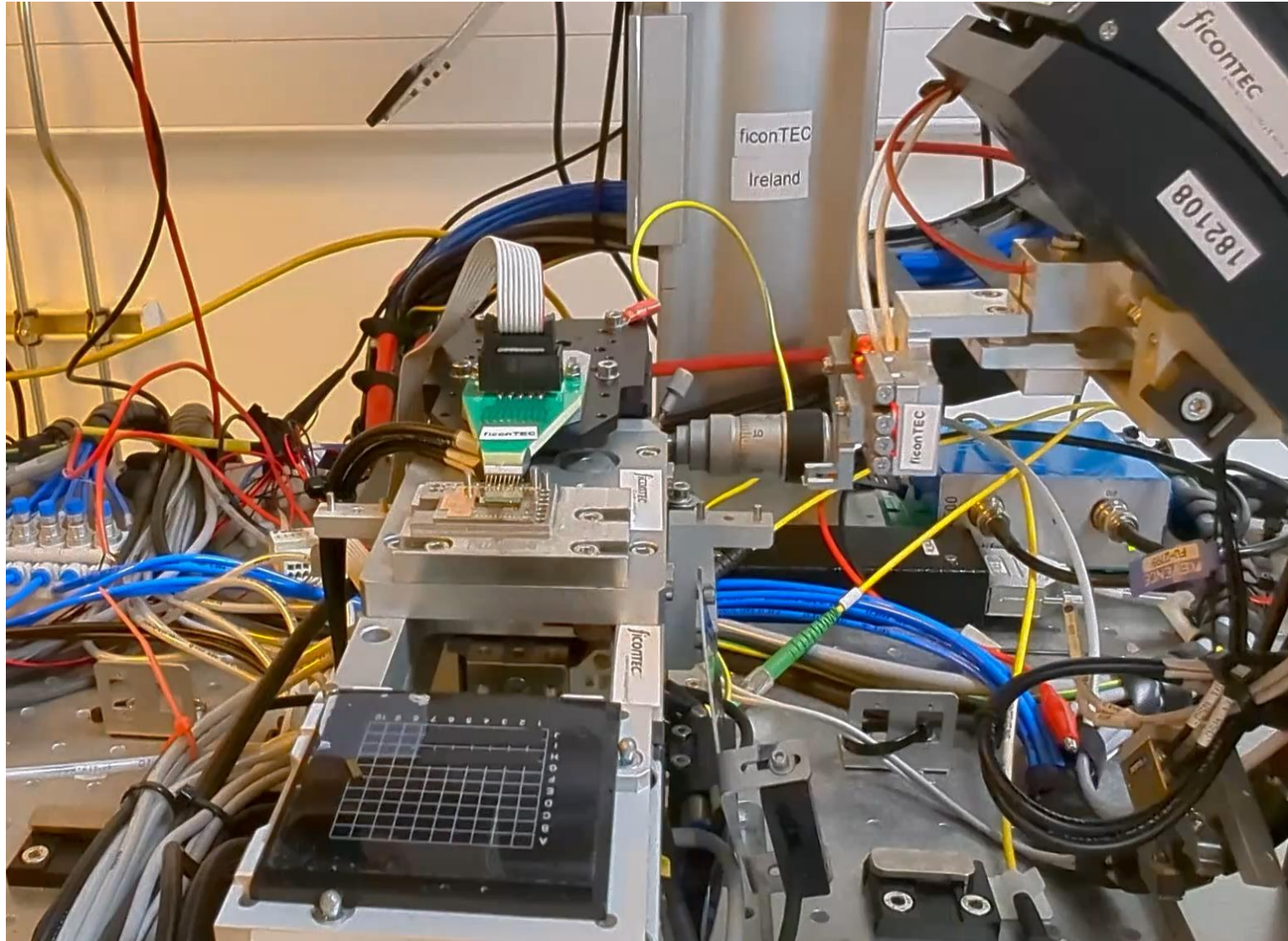
Glass Wafer-Level Packaging



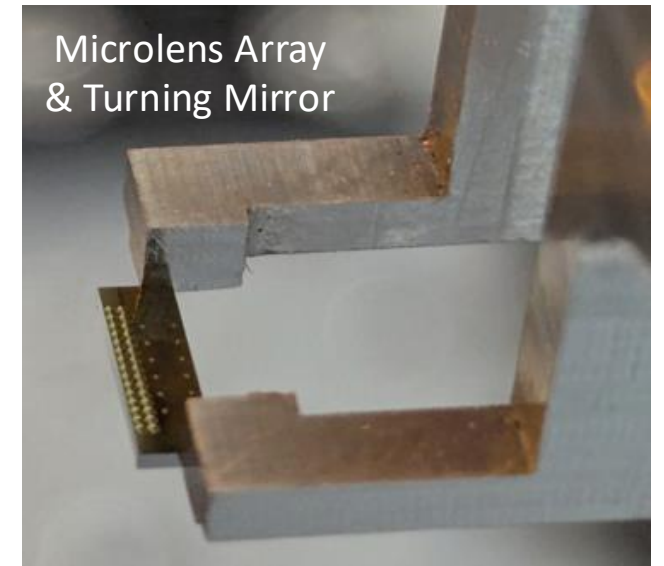
- Alignment Tolerance @ -1dB $\pm 25\mu\text{m}$
- Coupling Loss (PIC to Fibre) - 1.7dB

Out-of-Plane Optical Coupling to Photonic Integrated Circuits Using Turning-Mirror Lens Arrays
IEEE Transactions on Components, Packaging and Manufacturing Technology, August 2025.

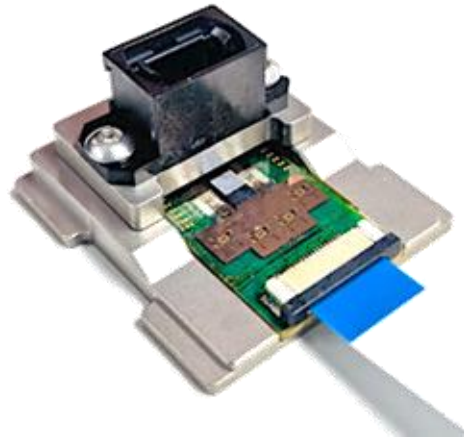
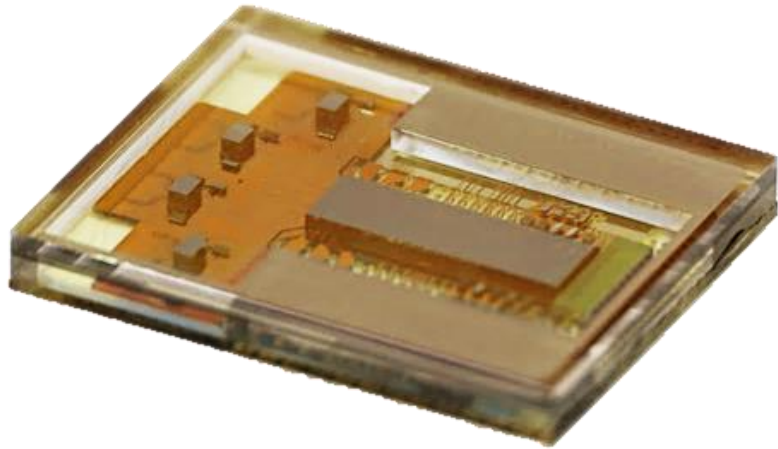
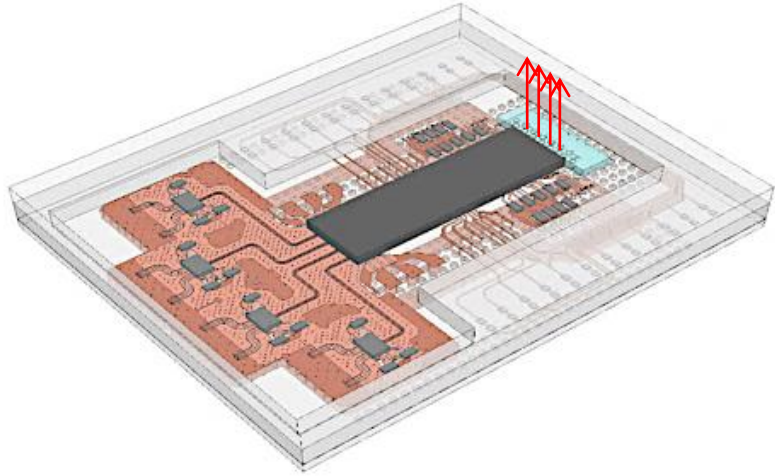
Glass Wafer-Level Packaging



Microlens Array
& Turning Mirror



Glass Wafer-Level Packaging





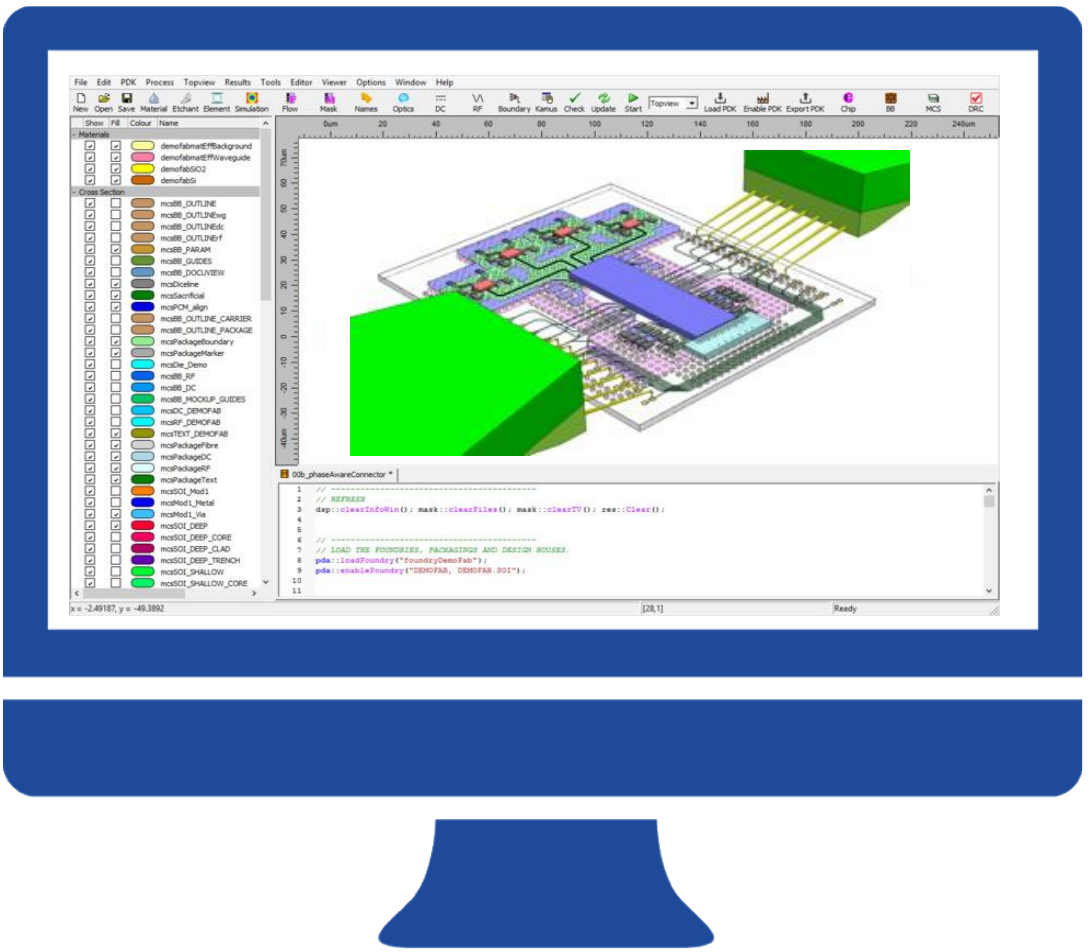
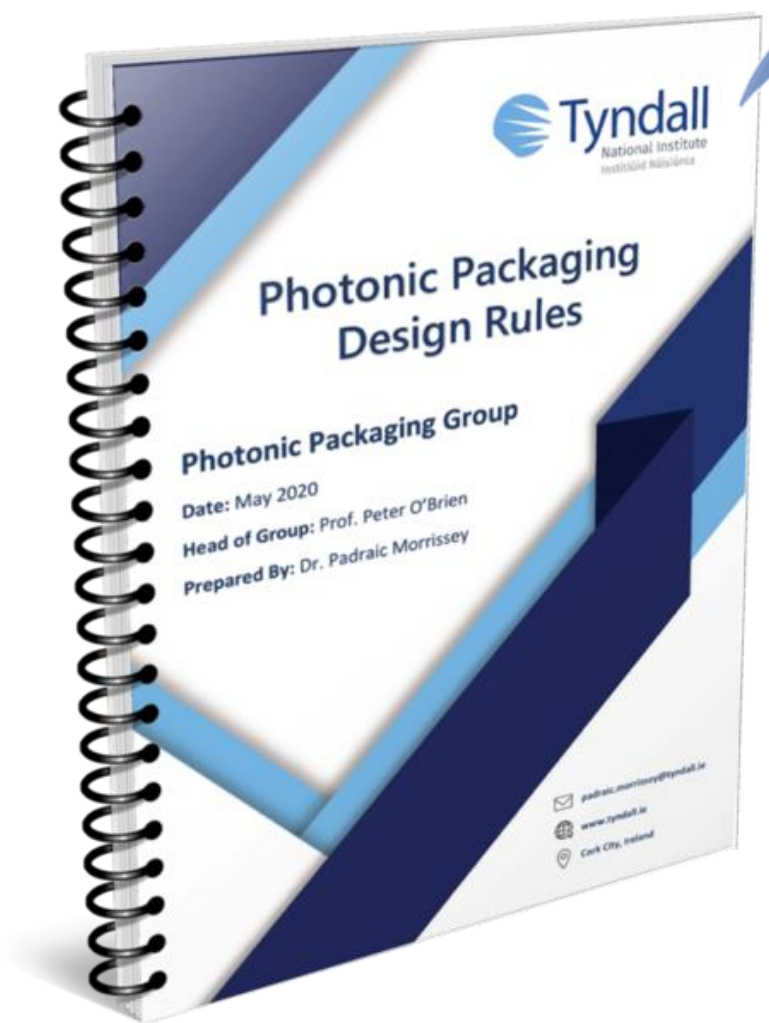
Automated Test Setup



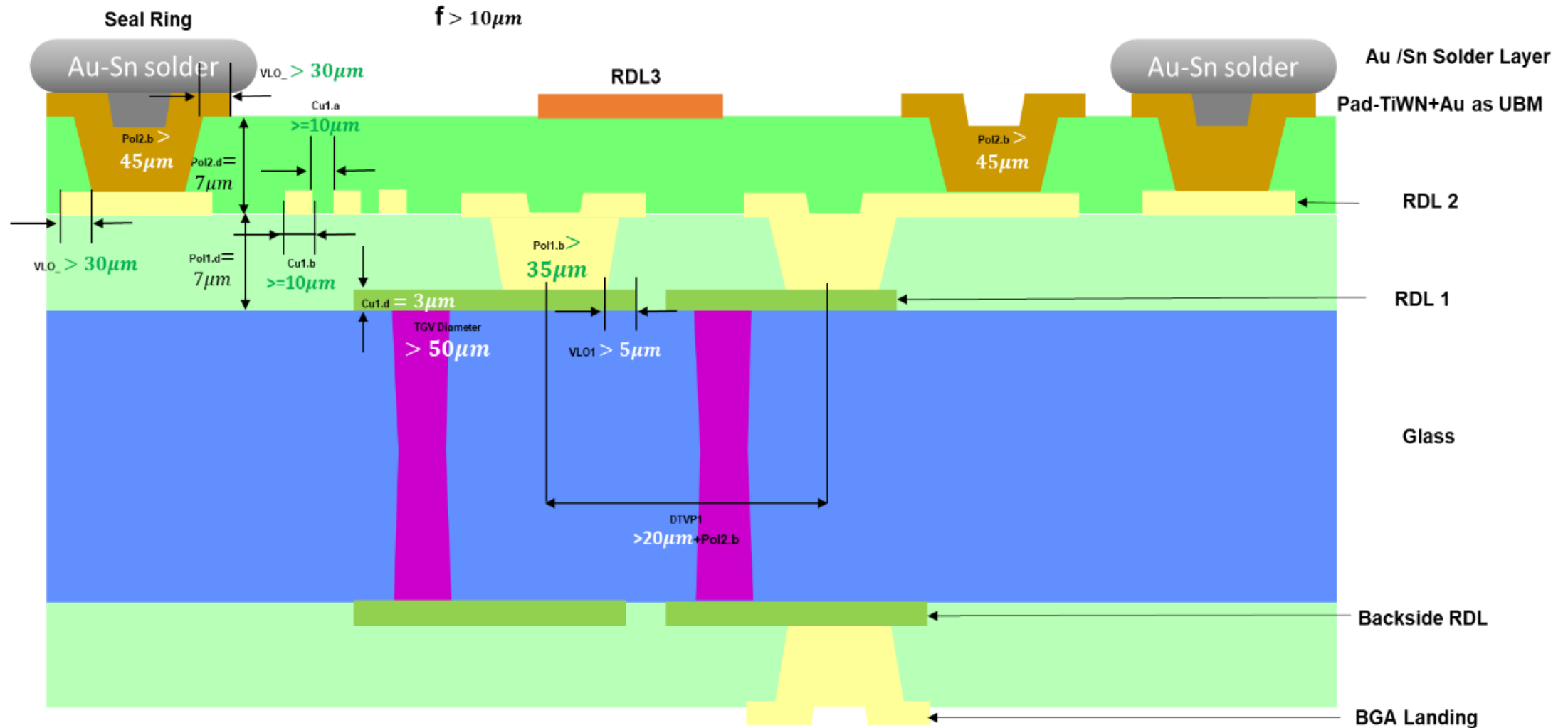
PHOTONICS PUBLIC PRIVATE PARTNERSHIP



Glass Wafer-Level Packaging



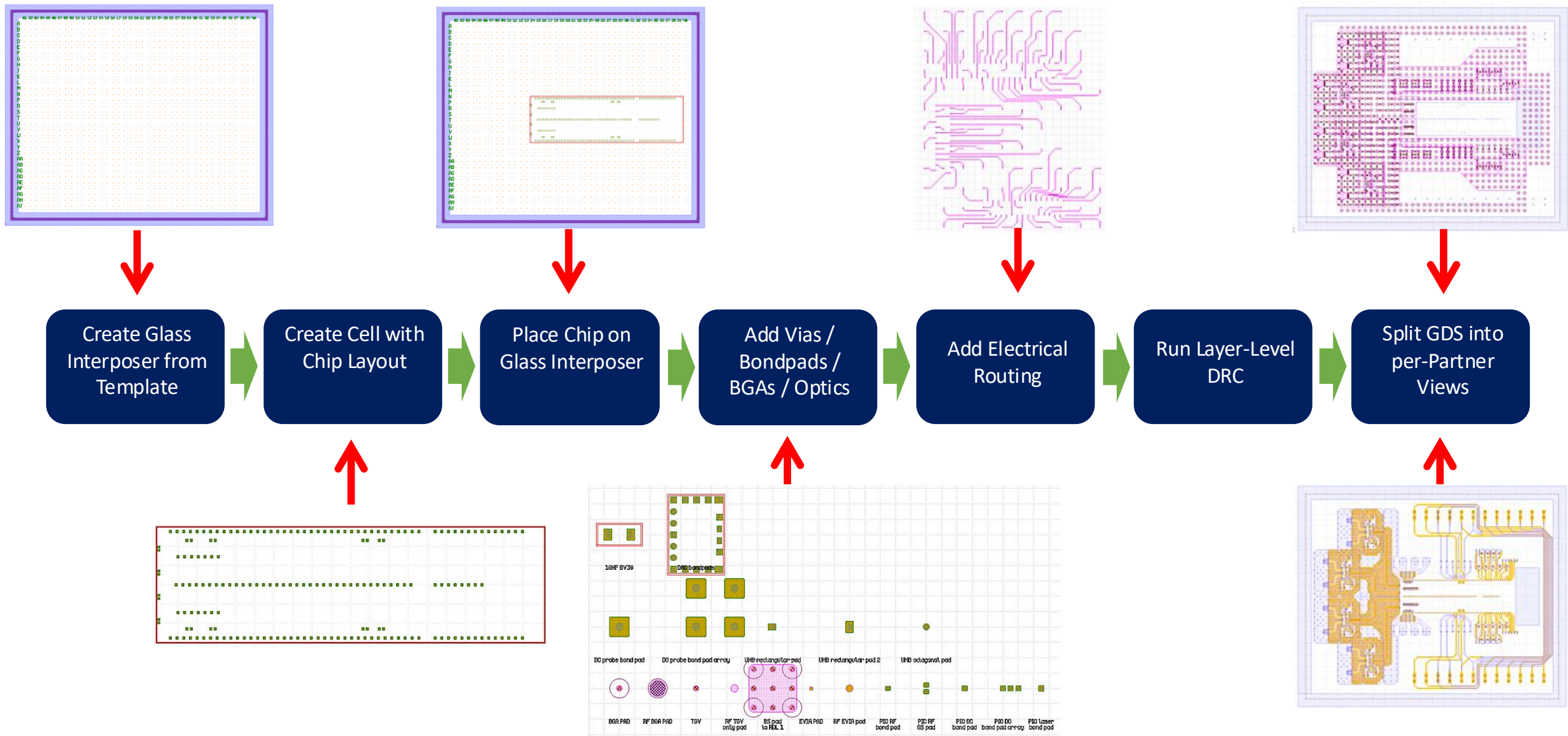
Glass Wafer-Level Packaging



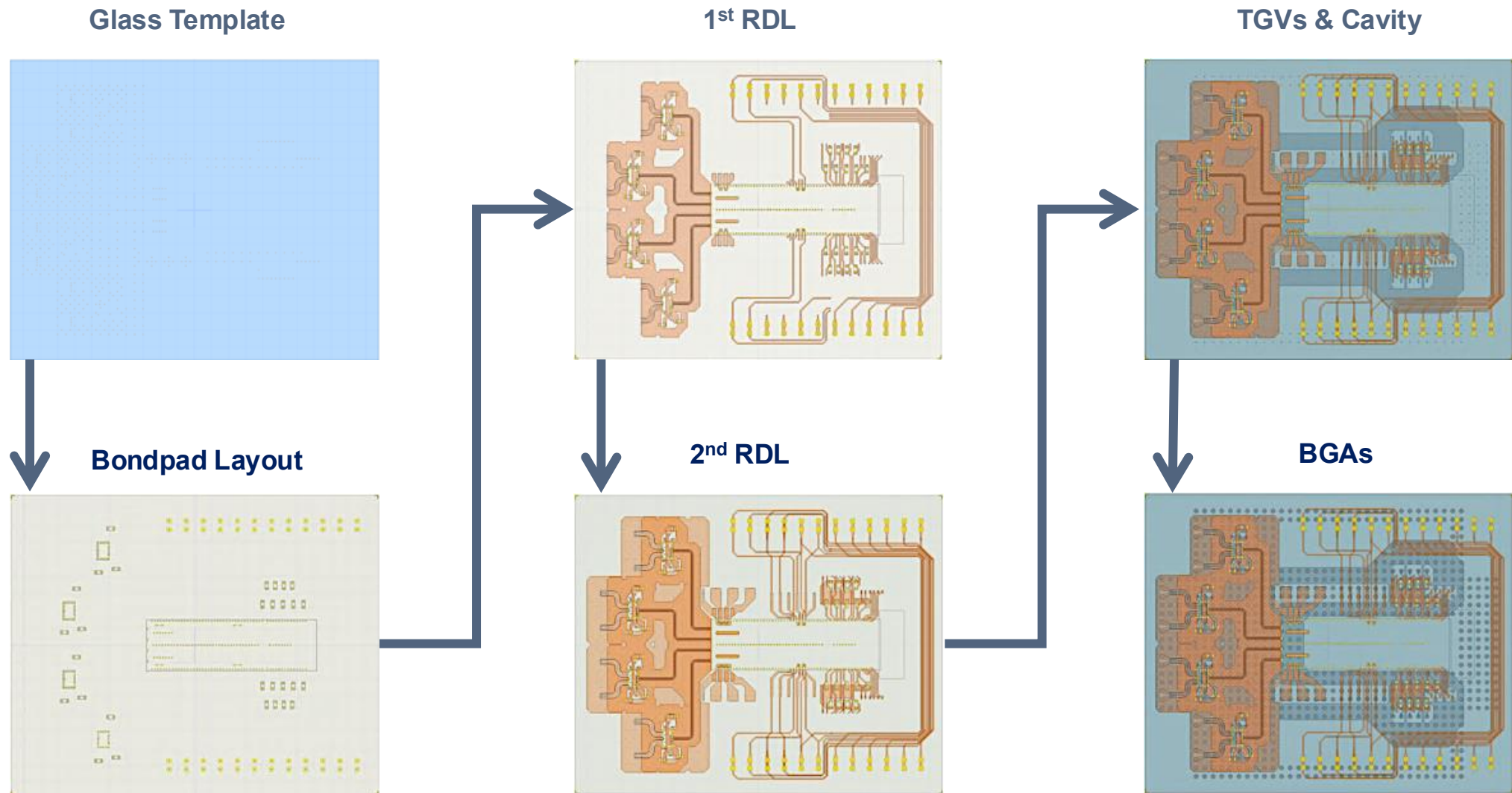
*Reference Thermal Chips for 2D and 3D Co-Packaging Process Development,
IEEE 73rd Electronic Components and Technology Conference, Orlando, 2023.*

*Thermal and Electrical Study of Glass Interposers in Co-Packaged Electronic-Photonic Systems
IEEE Transactions on Components, Packaging and Manufacturing Technology, August 2025.*

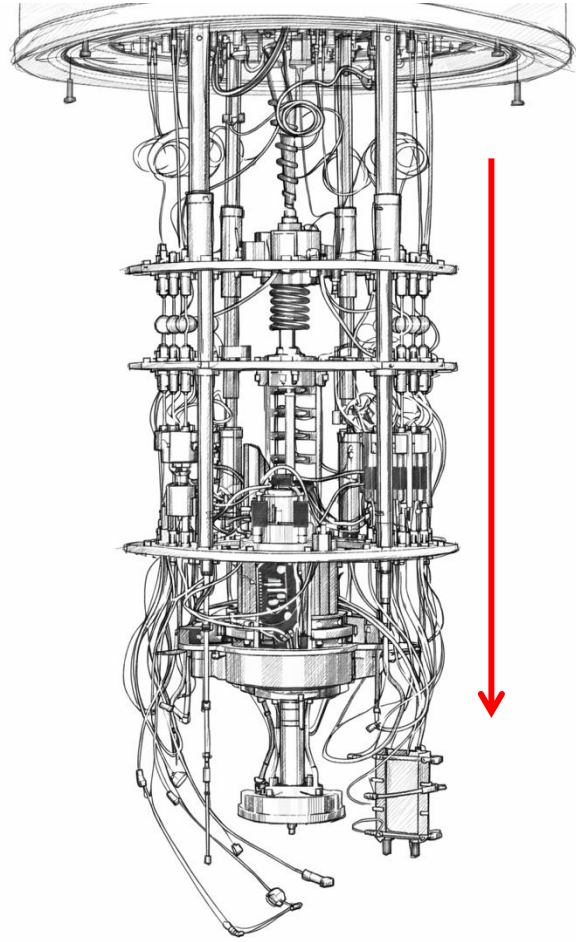
Glass Wafer-Level Packaging



Glass Wafer-Level Packaging

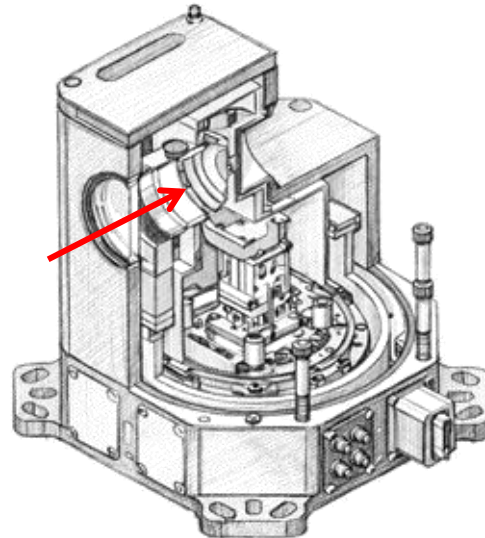


Quantum Device Packaging (cryogenic)



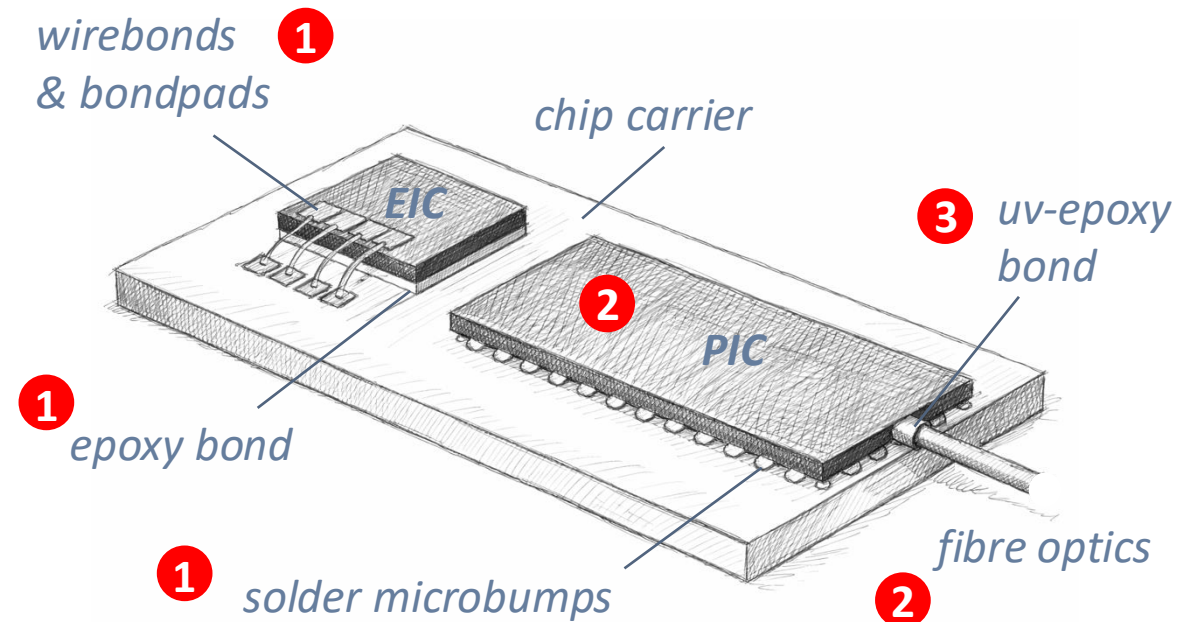
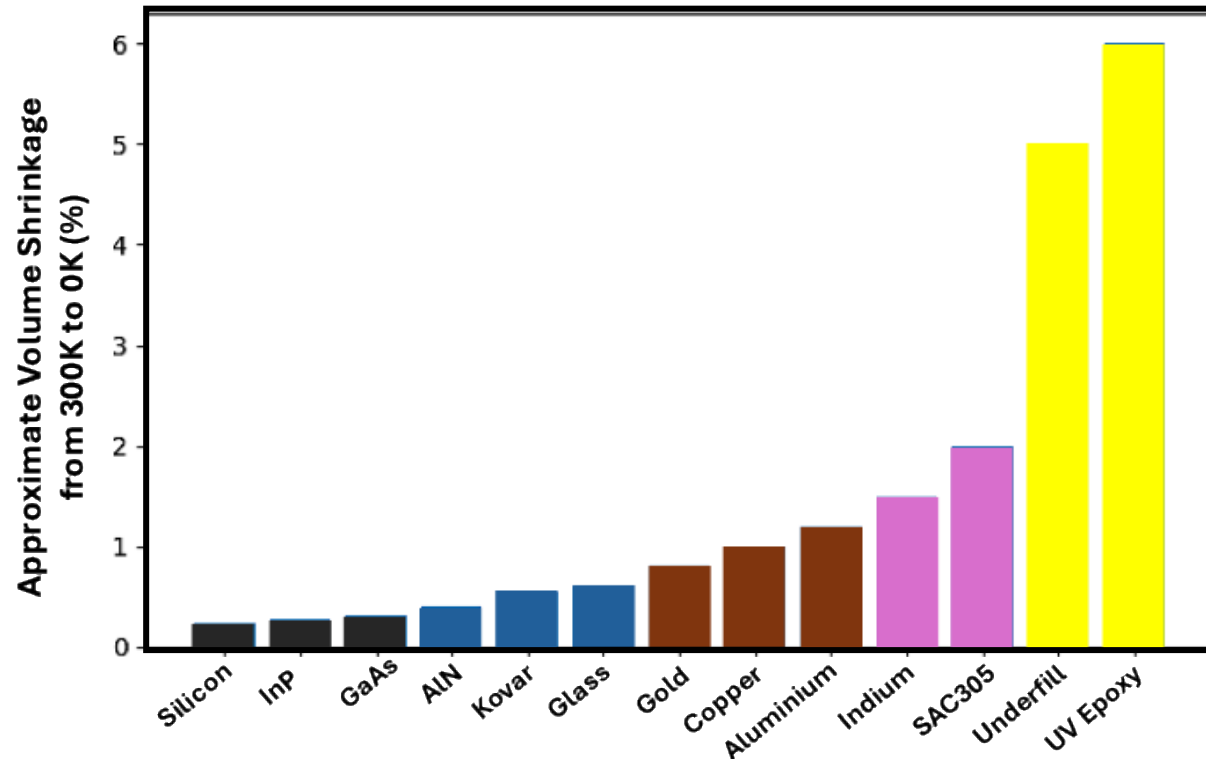
*optical & electrical
connections*

- Cryo chamber **design** affects package design (e.g. optical interfaces)
- Minimise **stress** on optical components (e.g. optical fibre strain relief)
- Polymer **outgassing** in vacuum (surface contamination)
- Structures stiffen and transmit **vibrations** (mechanical dampening)
- Package determines the '**thermal time constant**'



Quantum Device Packaging (cryogenic)

- 1 Significant CTE-induced stress between semiconductor chip and bonding/solder materials
(e.g. fracture between chip and electrical bonds cause open circuit)
- 2 Stress transfers into PIC chip waveguides, fibres and optical interfaces
- 3 Optical fibre alignment to chip changes during thermal cycling



Quantum Device Packaging (cryogenic)

- AgSnCu (e.g. SAC305) solder exhibits a **ductile-to-brittle transition** at approximately 200k
- High elastic modulus (**stiffening**) transmits strain into brittle (silicon) chip **increasing fracture risk**
- Solder-Chip fracture can induce **open electrical circuits** (accelerated by thermal cycling)

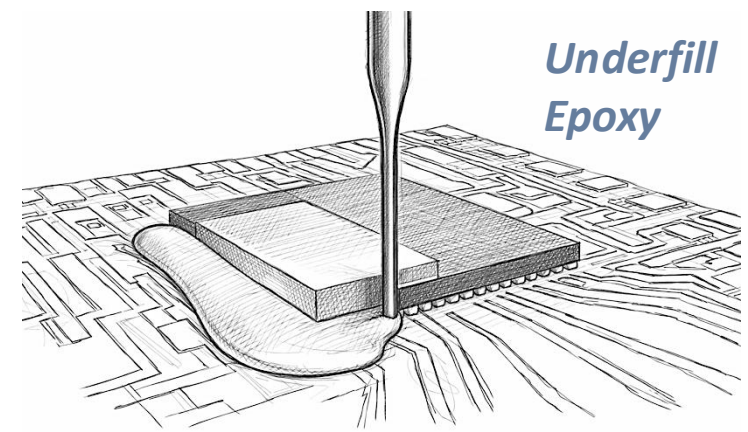
*Solder
Micro-Bumps*



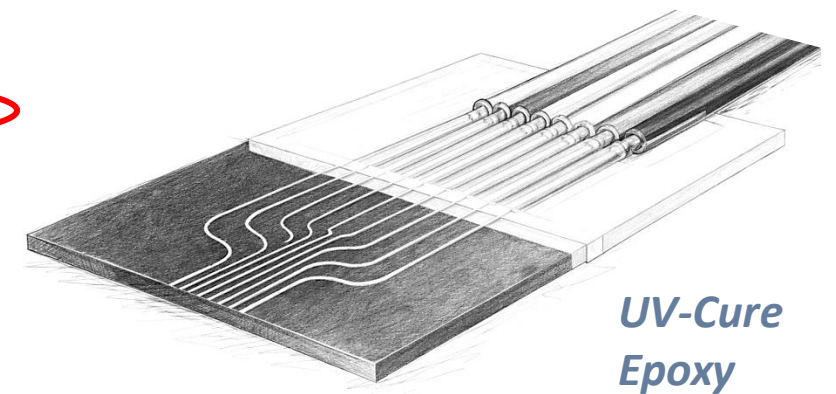
- Indium solder remains **ductile** at cryogenic temperatures
- **Accommodates CTE mismatch** between different materials by plastic deforming
- Excellent **thermal conductivity** and **low contact resistance** at cryogenic temperatures
- Low melting point ($\sim 156^\circ\text{C}$) allows **safe soldering** of sensitive cryogenic components
- Wets difficult surfaces (ceramics, glass, oxidised metals) enabling **reliable cryogenic joints**

Quantum Device Packaging (cryogenic)

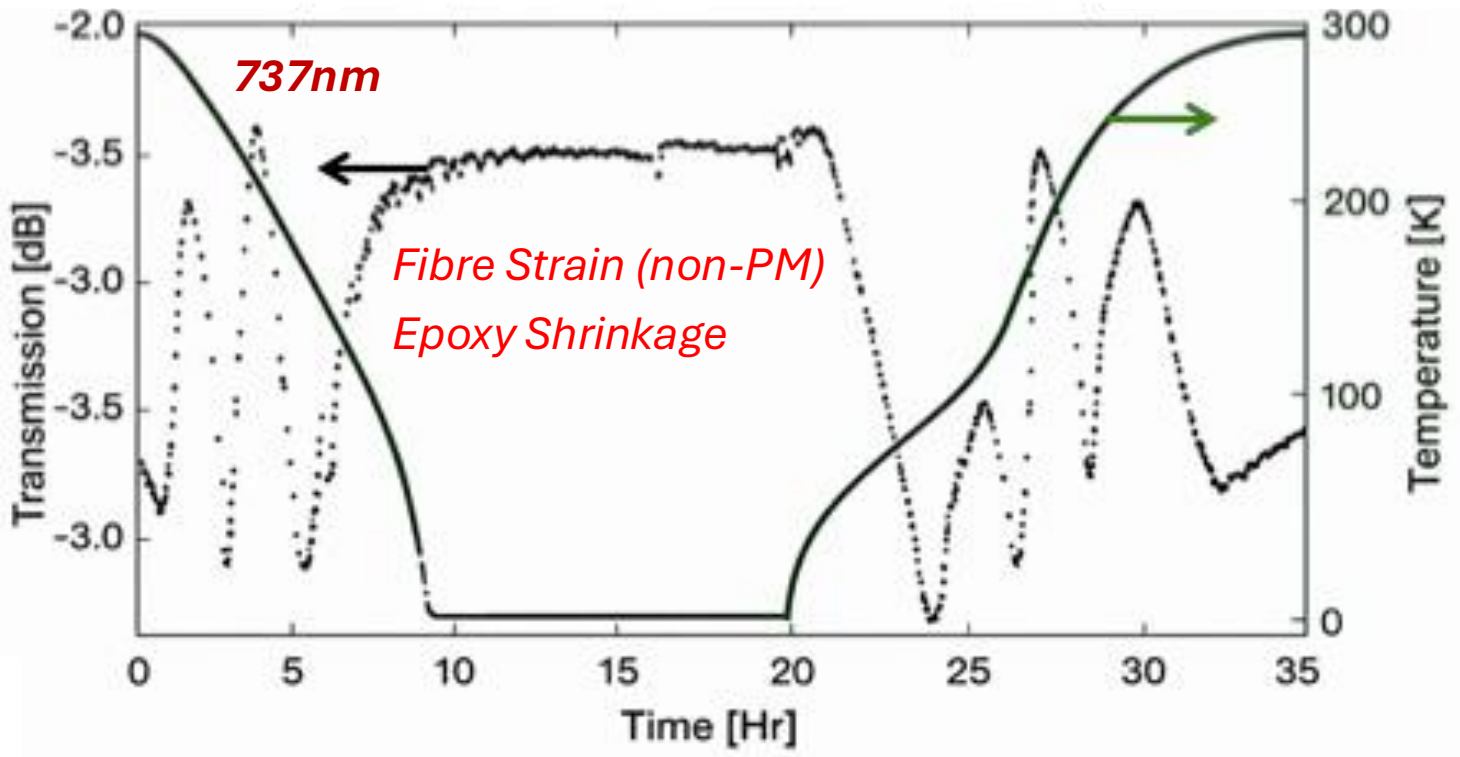
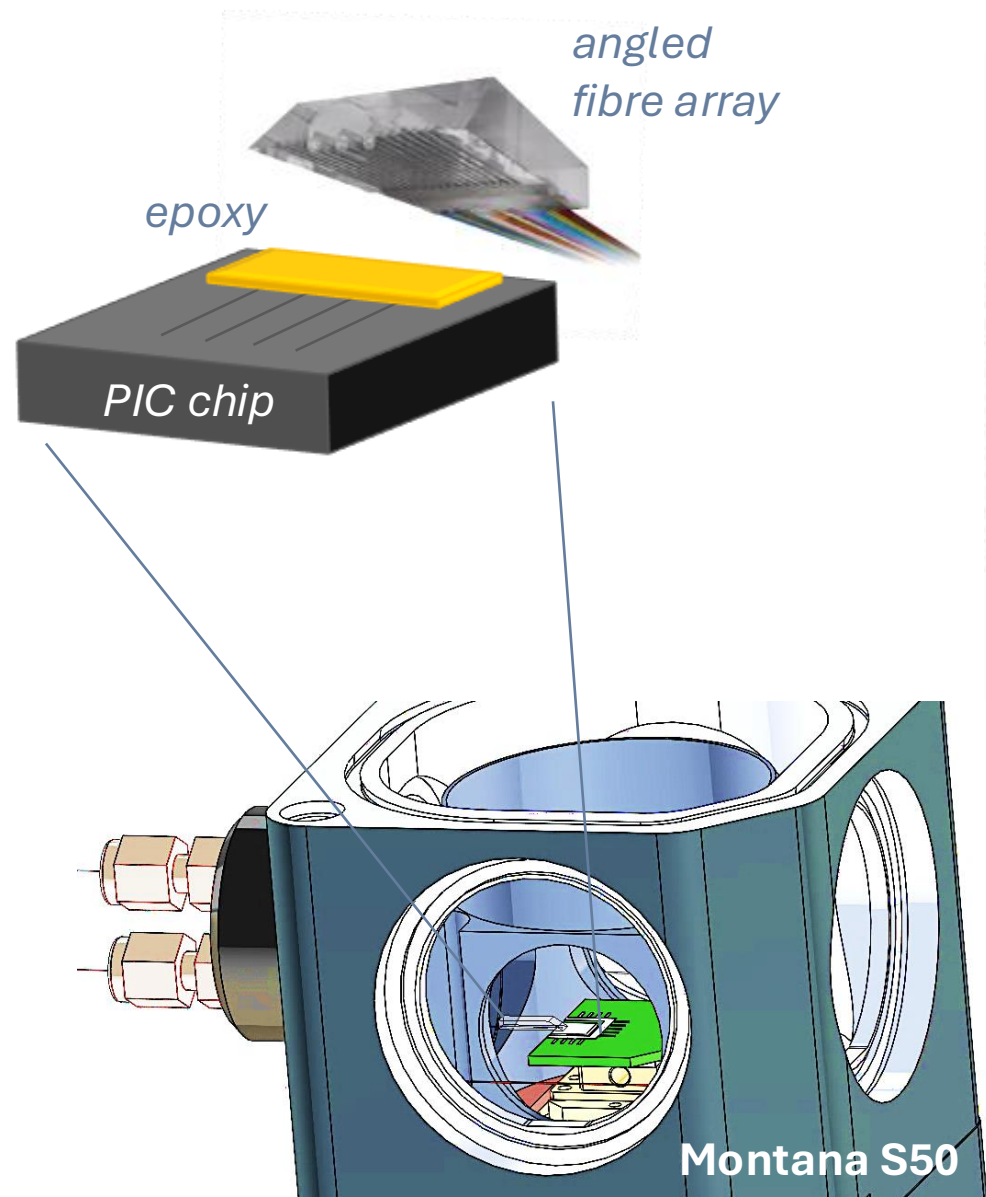
- Below their **T_g**, epoxies **lose ductility** and fracture toughness
- No longer able to deform to relieve **thermal-mismatch strain**
- Increased stiffness & brittleness induce micro-defects, especially during **thermal cycling**
- **Epoxy fillers** used in underfill materials can minimise brittleness
- Ensure **thin epoxy bondline**, typically between 10-30 microns (with low CTE)



- Thermal cycling will **shift fibre optical fibre alignment** to PIC chip
- Alignment tolerance typically **+/- 0.5 micron for 1dB optical loss**
- Where possible, need to design PIC with **large mode size** adaptor
- **Stress transfers** into PIC waveguides and optical interfaces
- Use **smaller optical components**



Quantum Device Packaging (cryogenic)



<i>UV Cure Epoxy</i>	<i>Dymax OP29</i>
<i>Modulus of Elasticity</i>	<i>234 MPa (relatively low)</i>
<i>Shear Force</i>	<i>8 kgF @ bonding</i>
	<i>7 kgF after thermal cycling</i>

Quantum Device Packaging (cryogenic)

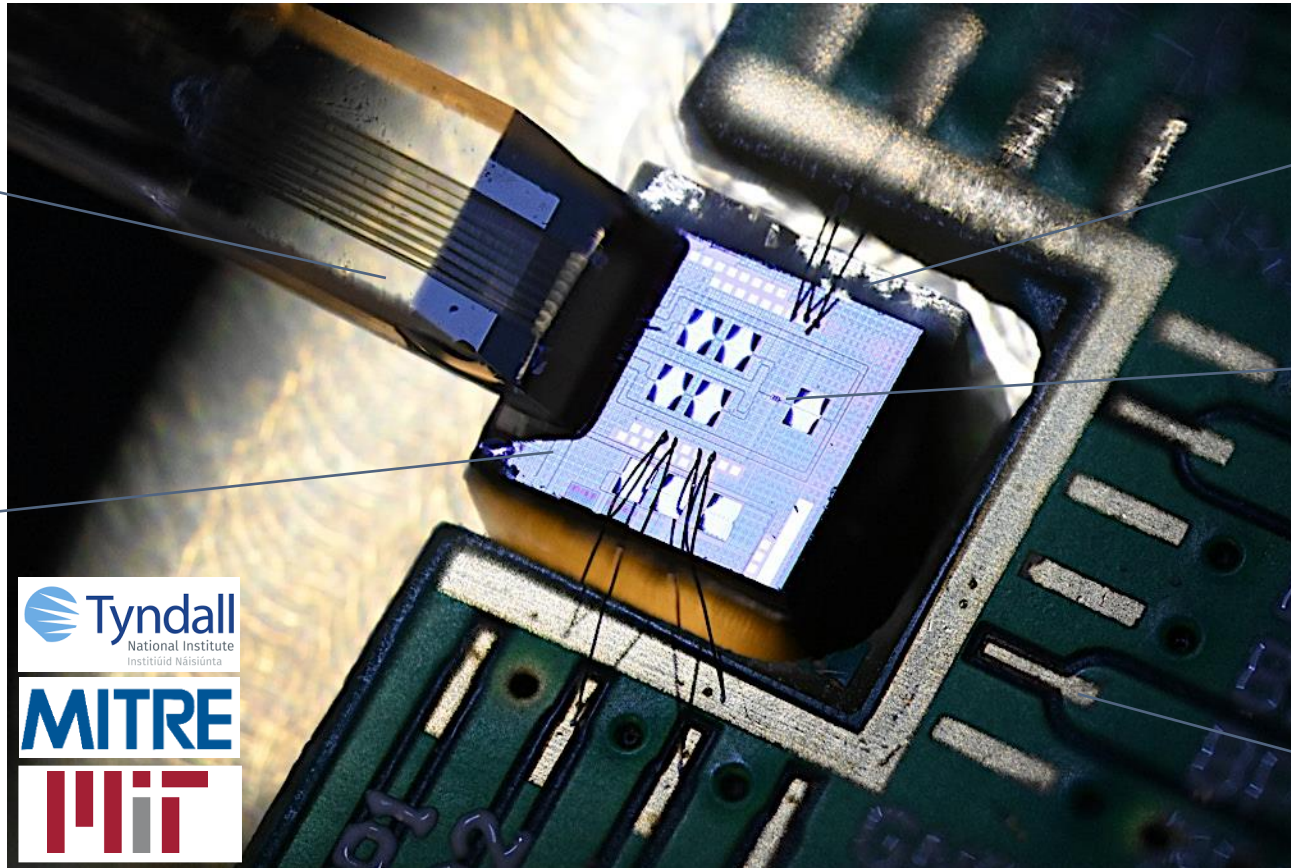
*optical fibre array
(grating coupled)*

*photonic chip
(SiN waveguides)
(fab at Sandia Labs)*

*copper submount
(400 mKelvin)*

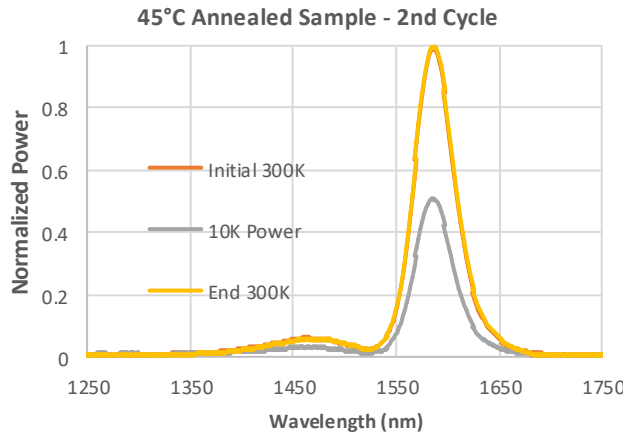
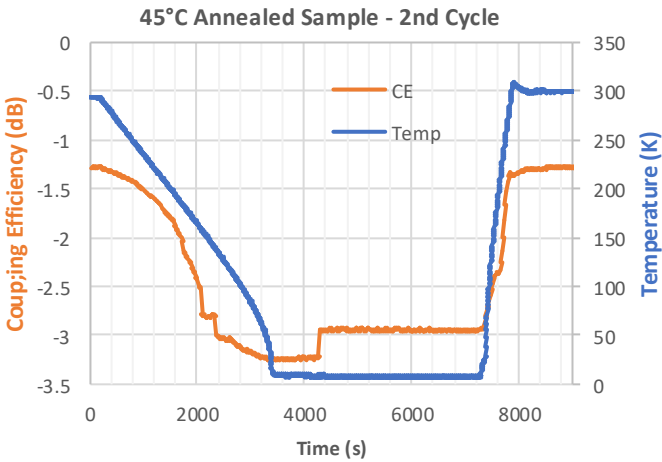
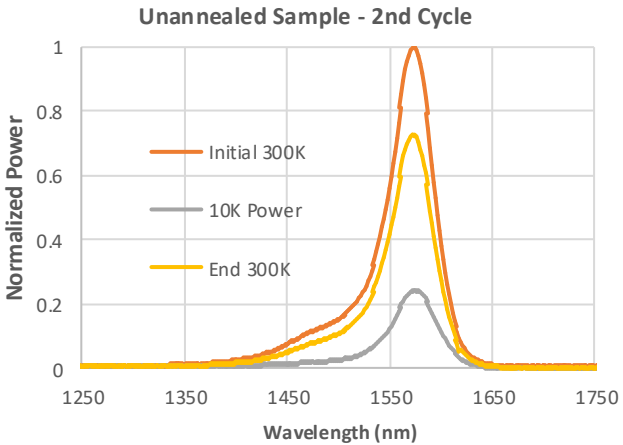
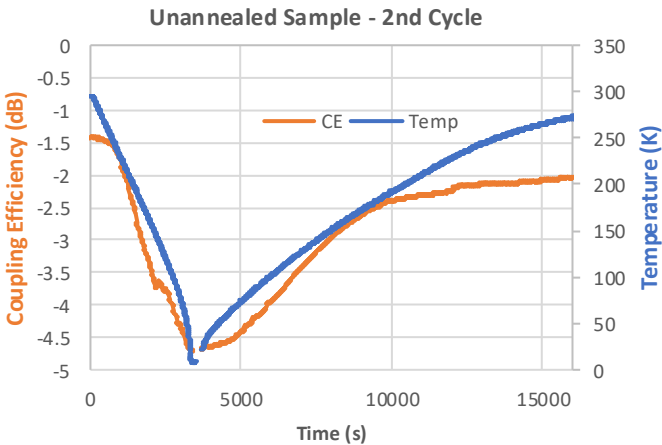
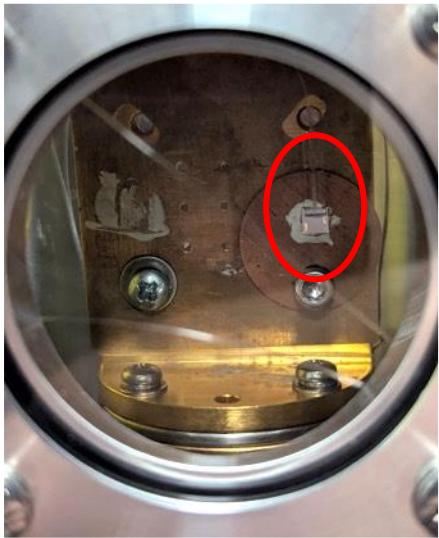
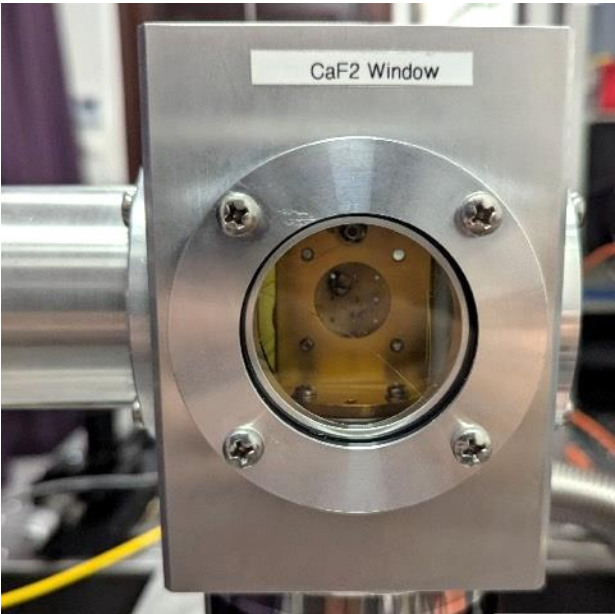
*Diamond MicroChiplet
(SiV Colour Centres)*

PCB



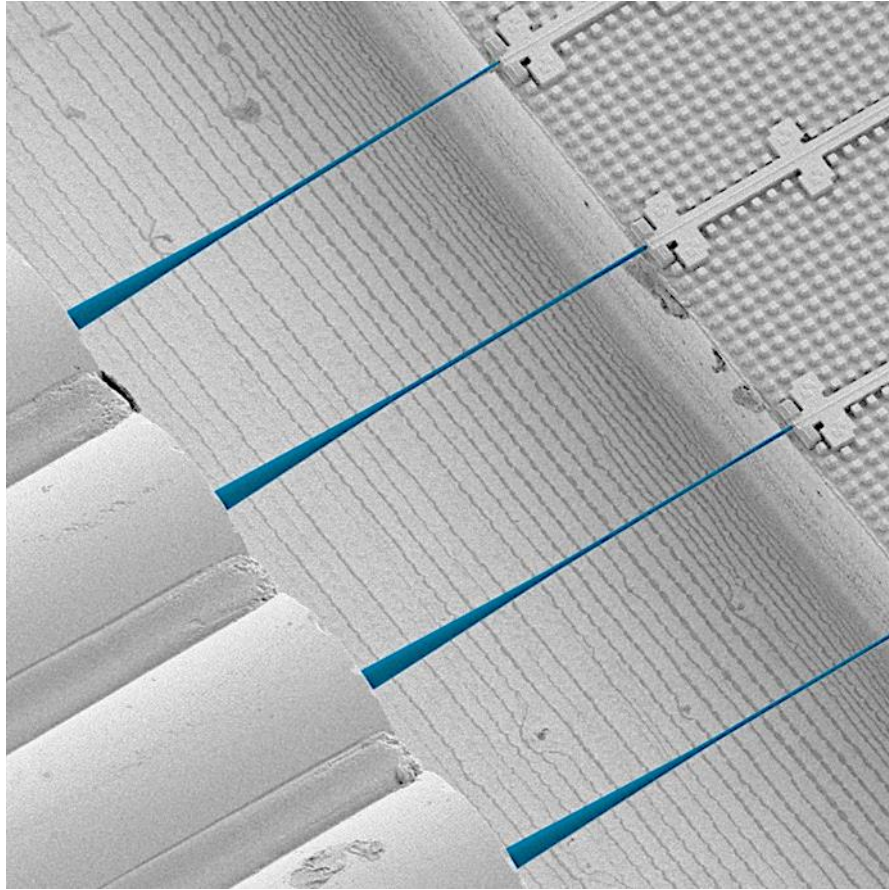
*Scalable low-loss cryogenic packaging of quantum memories in CMOS-foundry processed photonic chips
Optica Quantum, December 2025.*

Quantum Device Packaging (cryogenic)

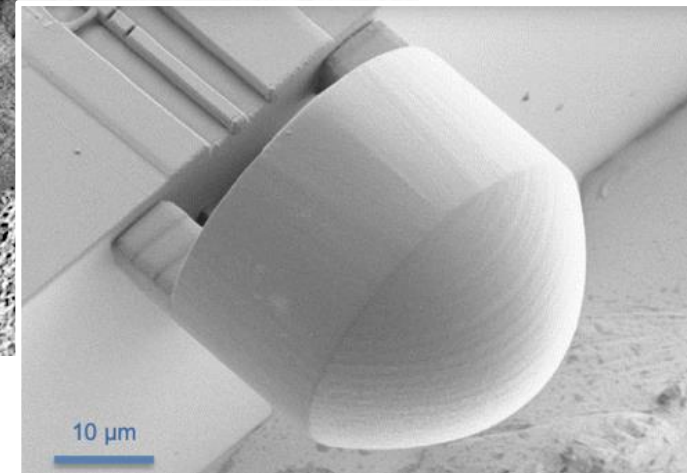
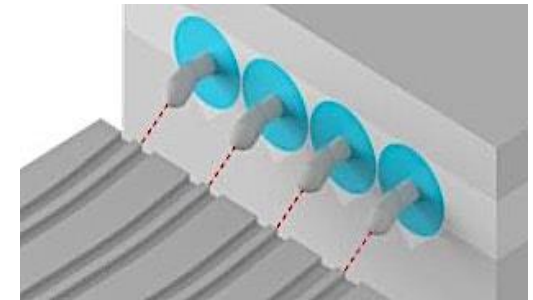
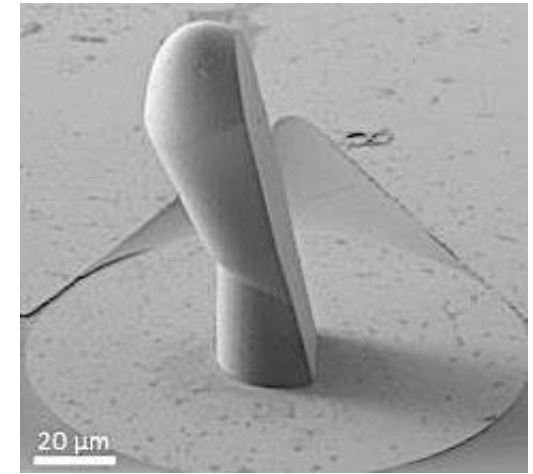
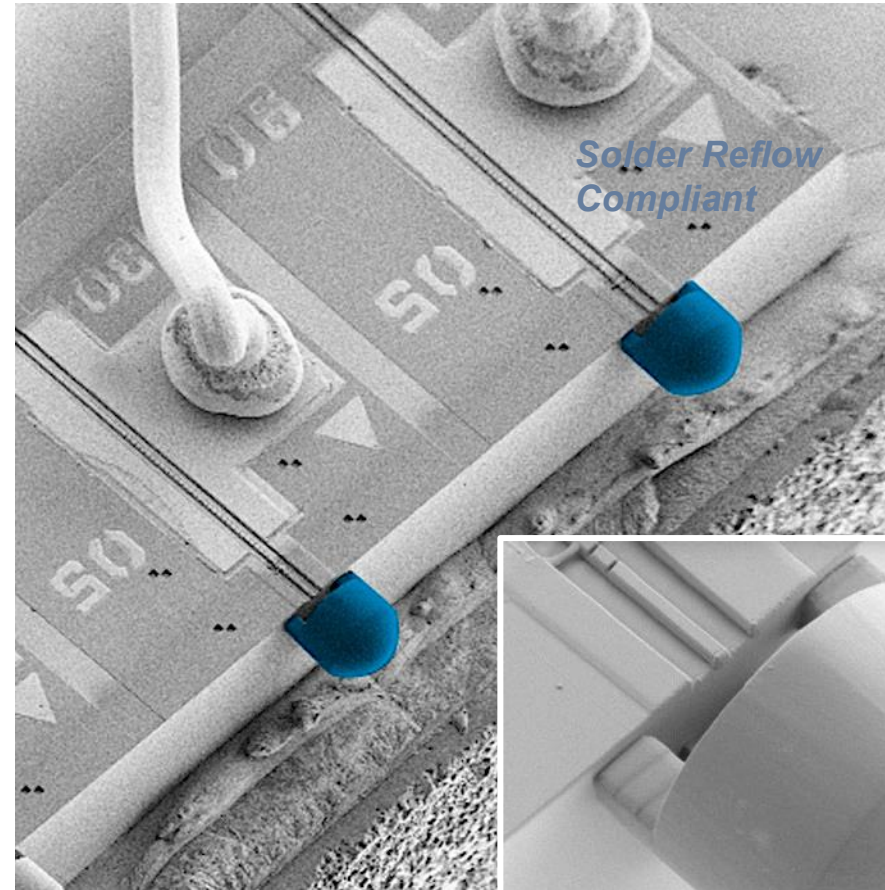


Quantum Device Packaging (cryogenic)

Photonic Integration using Industry-Ready Photonic Wire Bonds and Facet Attached Micro-Lenses
IEEE Transactions on CPMT, August 2025.



3D-Printed Facet-Attached Microlenses for Advanced Photonic System Assembly
Light: Advanced Manufacturing, 2023.



Quantum Device Packaging (cryogenic)

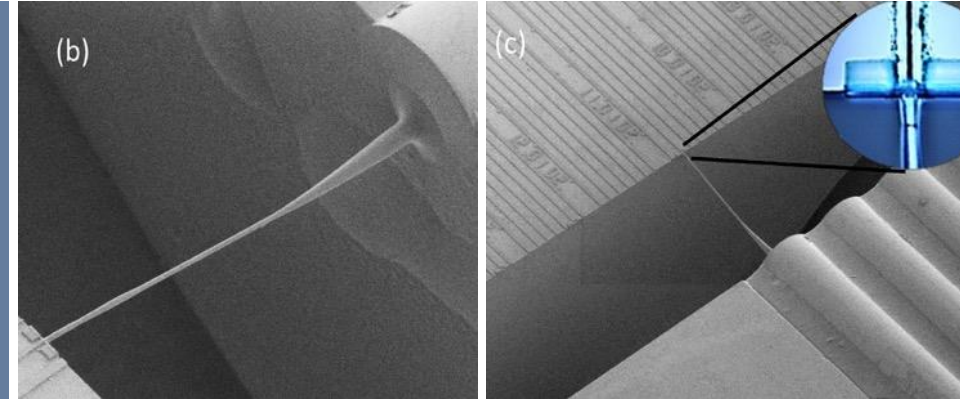
Plug-and-Play Fiber-Coupled Quantum Dot Single-Photon Source via Photonic Wire Bonding

Adv Quantum Technol. 2023, 2300227.

Passive alignment of single-photon sources
to optical fibers via PWB

Measurement of single-photon emission source from a
quantum dot (QD) in a waveguide

Assemblies cooled to 1.6K for more than 1 week



Superconducting nanowire single-photon detector with 3D-printed free-form microlenses

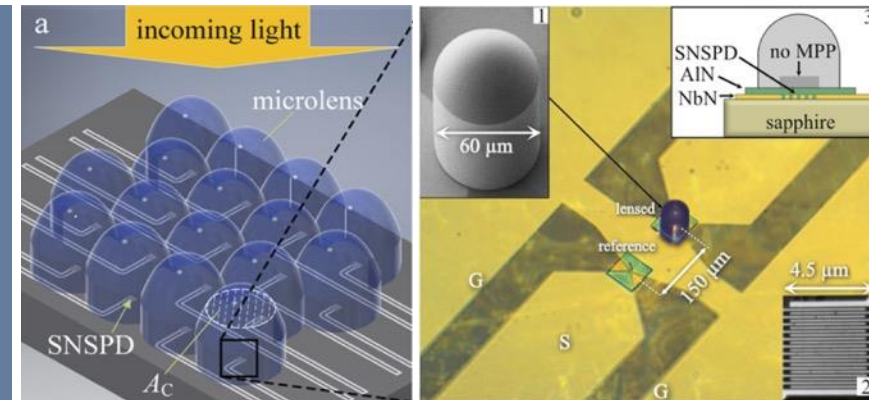
Opt. Express 29, 27708-27731, 2021.

FAMLs operating at cryogenic temperatures down to 4.6K

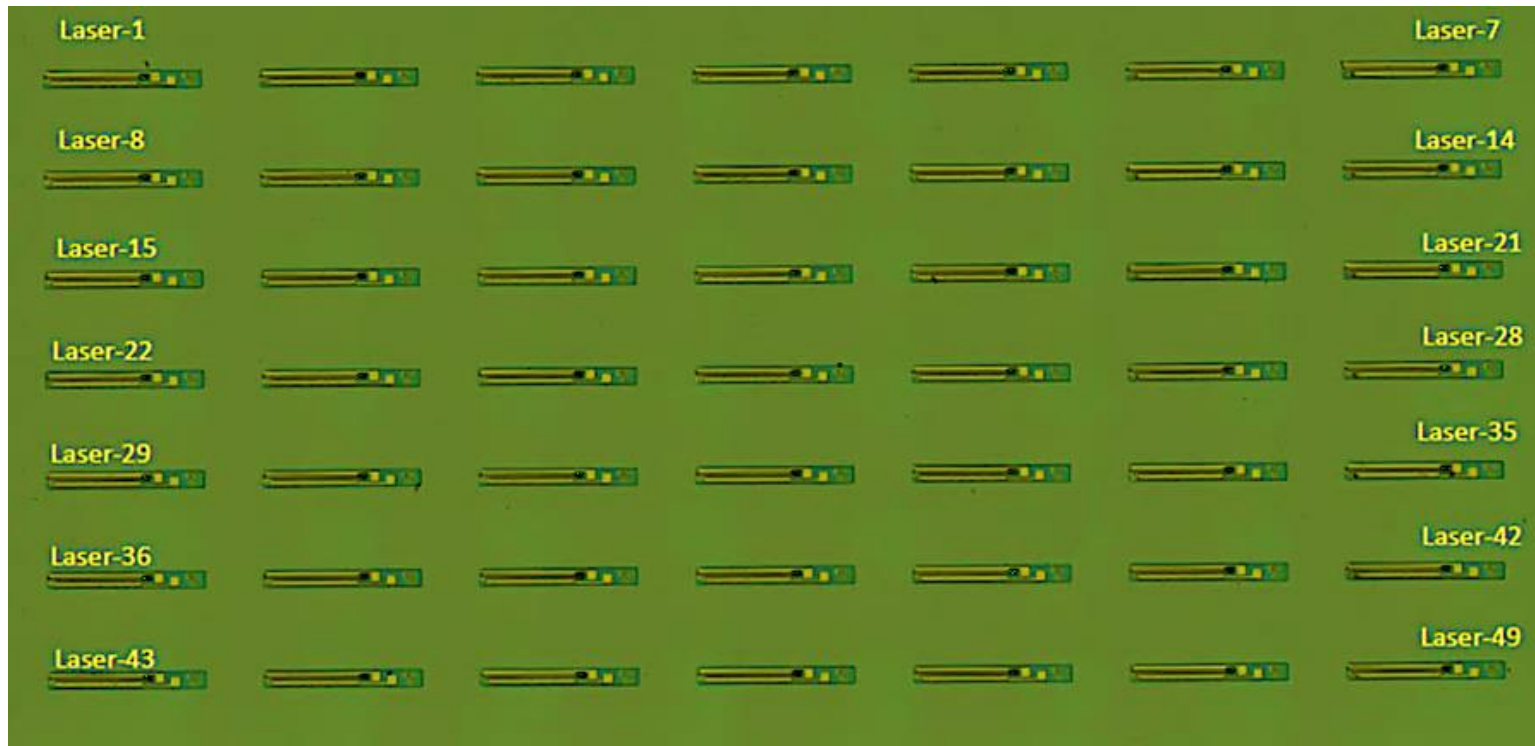
Assemblies undergo 10 cool down cycles

No degradation or delamination observed

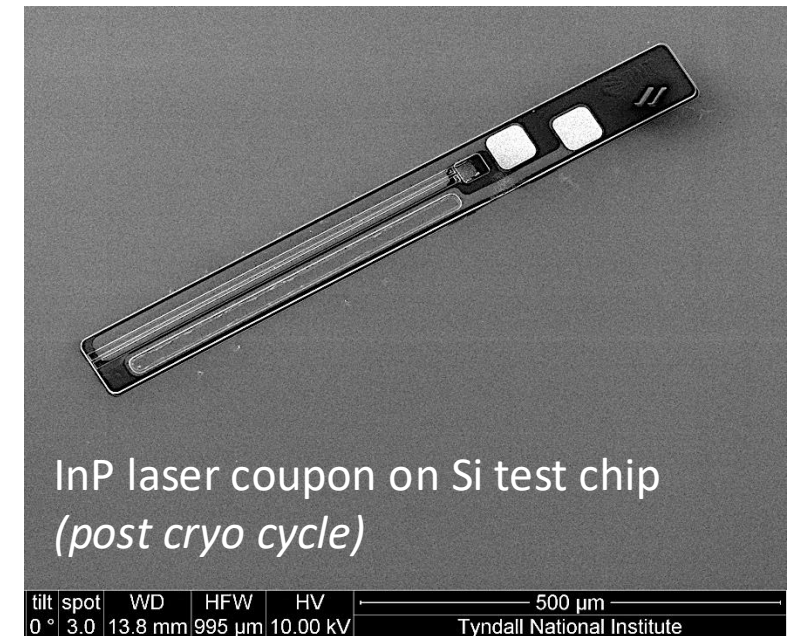
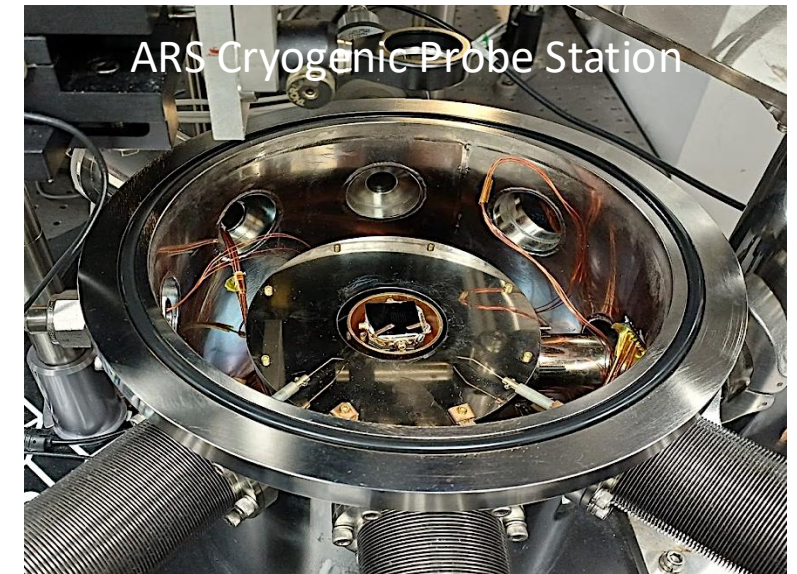
Broadband operating range 530 – 2000 nm



Quantum Device Packaging (cryogenic)



- 7 x 7 InP laser coupons printed on Si test chips
- 80nm of *Intervia* used to bond InP laser coupons to Si test chips
- Samples cooled to 16K and held for 3 hours
- All laser coupons remained bonded (SEM inspection)
- No cracking or visible degradation observed



Device & Package Reliability

Details	JEDEC	Telcordia
Primary Focus	Semiconductor Devices	Telecom Network Equipment
Usage (Optical Context)	Chip & Package Reliability	Optical Engine & Telecom Deployment Qualification
Industry Scope	Consumer, Industrial, Computing	Carrier & Telecom Infrastructure
Level of Testing	Component / Chip-level	System & Network-level
Environment Assumption	Controlled Environments	Central Office & Outside Plant
Typical Lifetime Target	10–15 Years	20–25+ Years
Failure Rate Goal	Low Failure	Extremely Low (carrier grade)
Key Standards	JESD47, JESD22 series	GR-468, GR-63, GR-1089, SR-332
Used For (Optical Context)	Chip & Package reliability	Optical Engine & Telecom Deployment Qualification

Device & Package Reliability

GR-468 for Transceivers

Opto-Electronic Device Reliability

- Laser diodes (DFB, VCSEL)
- Photodiodes
- TOSA / ROSA assemblies
- Optical subassemblies



🔥 High Temperature Operating Life (HTOL)

- Operated at elevated temperature & bias
- Accelerates aging mechanisms

⚠ Temperature Cycling

- Repeated -40°C to $+85^{\circ}\text{C}$ (or wider)
- Detects solder fatigue and package cracks

💧 Damp Heat / HAST

- High humidity stress
- Verifies moisture resistance

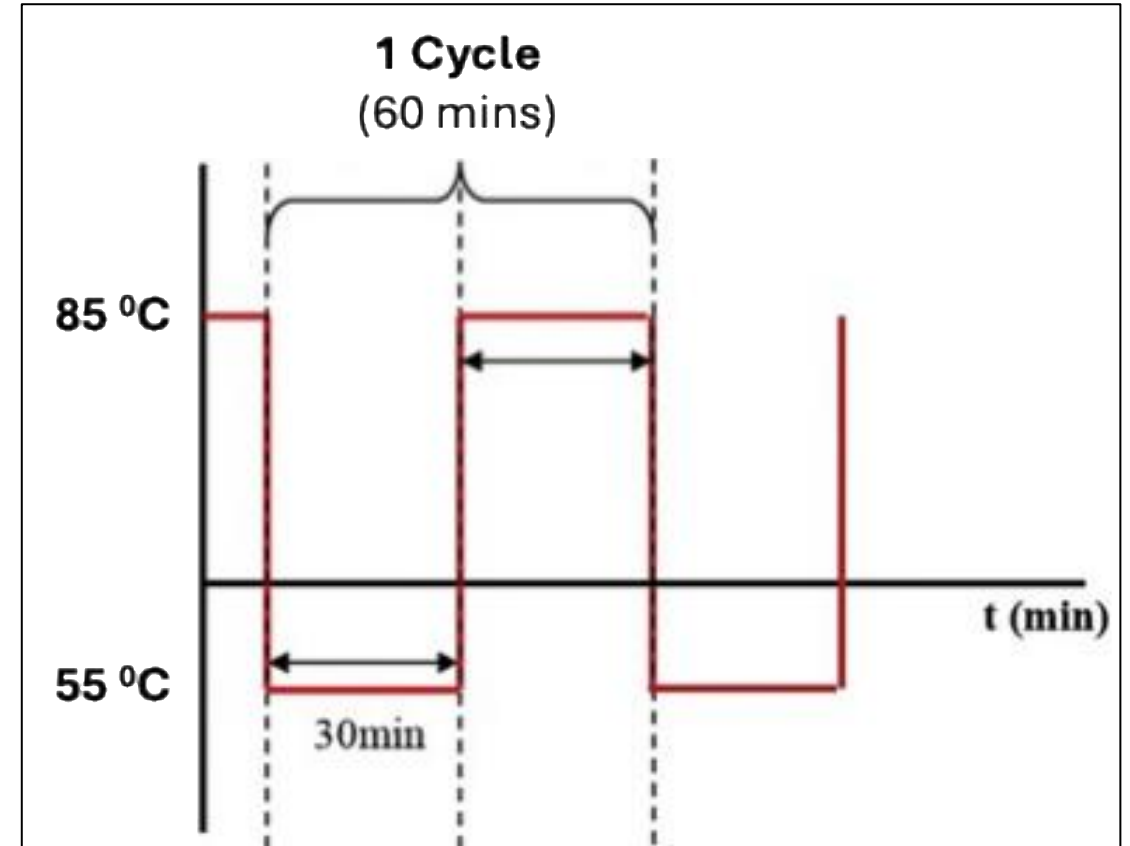
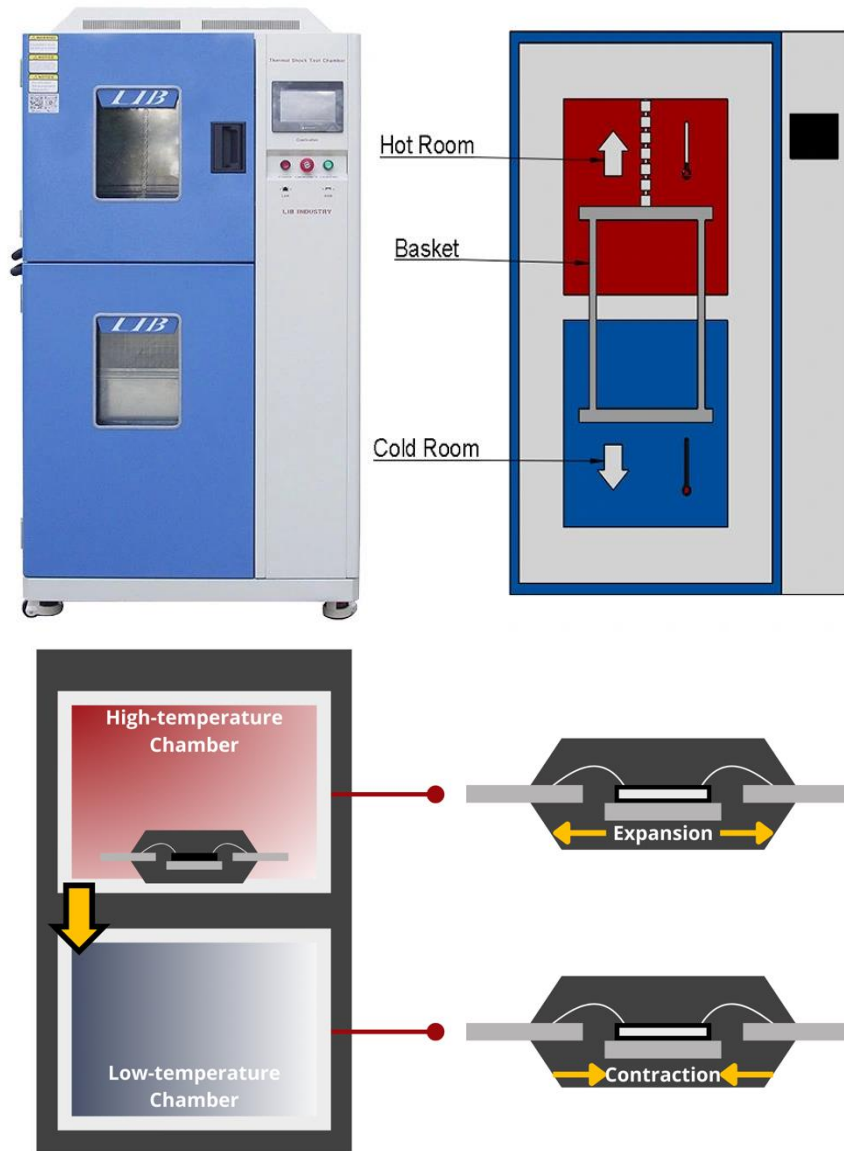
⚡ ESD & Electrical Stress

- Protects against handling damage

🔧 Mechanical Shock & Vibration

- Survivability in central office or field environments

Device & Package Reliability



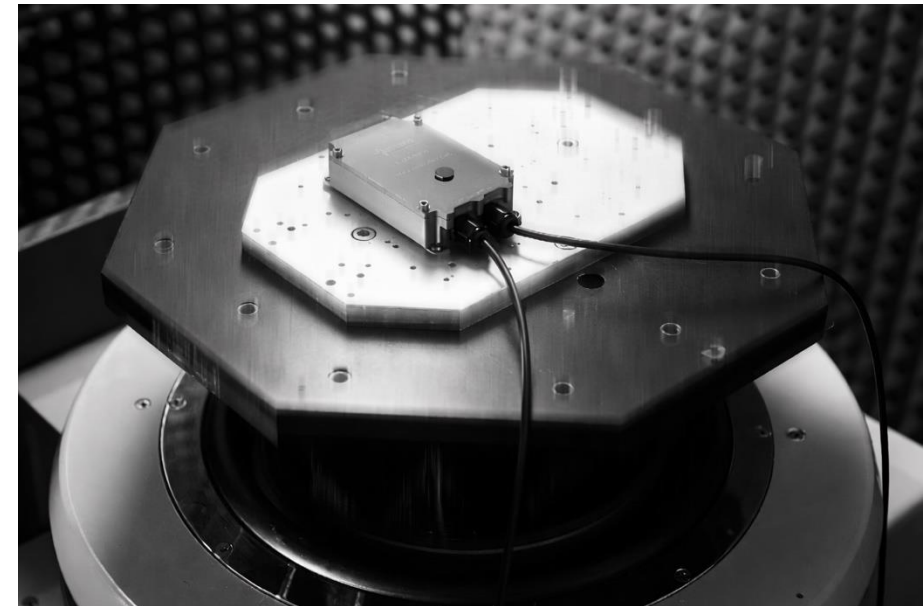
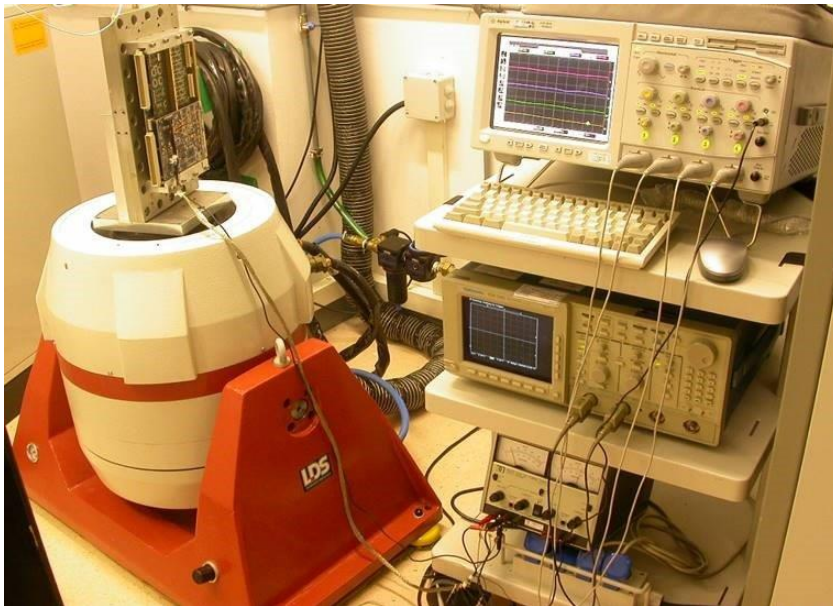
Device & Package Reliability

Sinusoidal Vibration: Sweeps through a frequency range (e.g., 10 Hz to 2,000 Hz) to identify resonant frequencies and evaluate structural integrity under sustained, rhythmic stress.

Random Vibration: Simulates real-world conditions (like transport via truck or rocket launch) by exciting all frequencies simultaneously, often more likely to trigger failures than sine tests.

Mixed-Mode Vibration: Combines types, such as Sine-on-Random (SoR), to replicate complex environments like helicopters or tracked vehicles.

Combined Thermal-Vibration: Simultaneously applies temperature cycles and vibration to assess compounded stresses common in automotive and aerospace applications.



Device & Package Reliability (CPO)

- CPO integrates high-power electronic ASICs and sensitive photonic components in a single package.
- Reliability challenges are fundamentally multi-physics: electrical, thermal, mechanical, and optical.
- Failure mechanisms are often gradual and performance-degrading rather than catastrophic.
- Optical performance stability over lifetime is as critical as electrical functionality

Device & Package Reliability (CPO)

- High ASIC power density creates strong local temperature gradients within the package.
- CTE mismatch between logic die, photonic die, interposer, and fiber attach structures induces stress.
- Repeated power and temperature cycling leads to accumulated mechanical fatigue.
- Micron-scale deformation can cause optical misalignment and coupling efficiency loss.
- Thermal stress accelerates degradation of lasers, modulators, and photodetectors.

Device & Package Reliability (CPO)

- Electrical interconnects (micro-bumps, hybrid bonds, RDLs) experience thermo-mechanical fatigue.
- Fine-pitch interconnects are susceptible to electromigration under high current density.
- Optical interfaces are extremely sensitive to positional drift and mechanical relaxation.
- Fiber-to-waveguide attach is a critical long-term reliability risk point.
- Small alignment shifts can significantly increase insertion loss and BER



**European Chips Act
Photonics Pilot Line**

PIX•Europe

400M Euro Investment
(European Union & Member States)

EU Chips Act (Pilot Line Concept)

PIX Europe



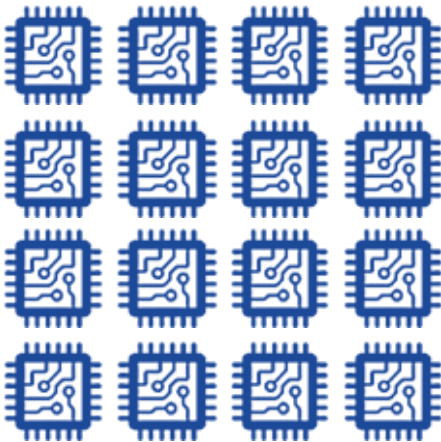
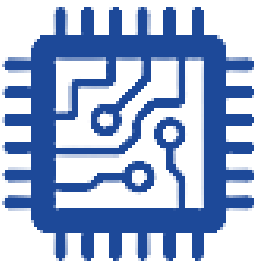
Concept

Research

Prototype

Pilot

Manufacture



Technology Transfer (European Pilot Line)

Optimise Materials, Process & Equipment

Standardise the Process

Scale the Process

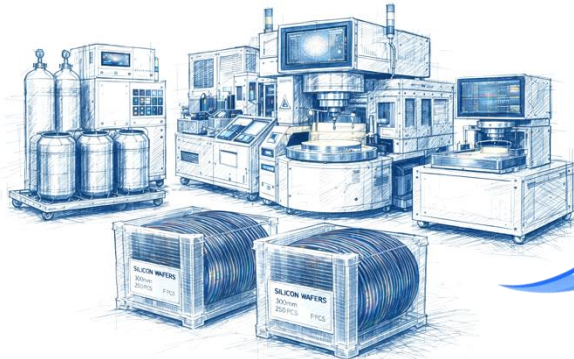
Validate Production

Transfer the Process

Train the Workforce



European Research



European Suppliers



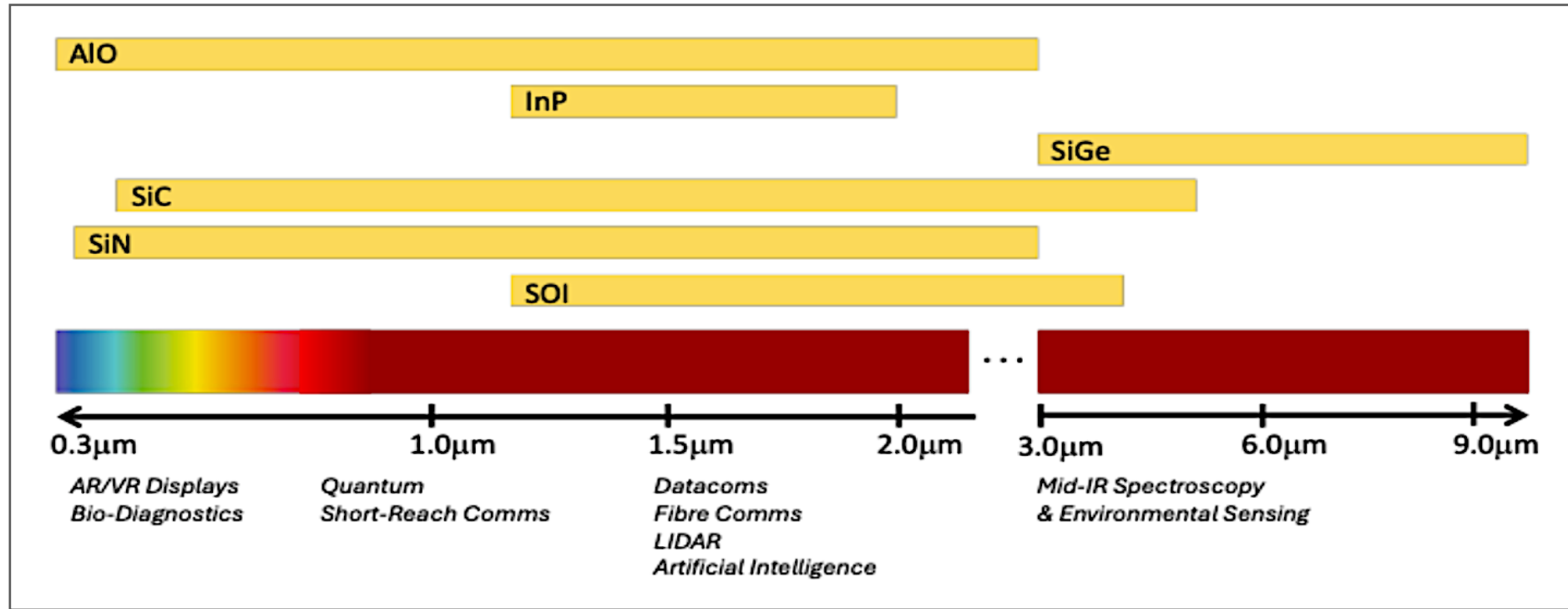
European Pilot Line



European Manufacturing

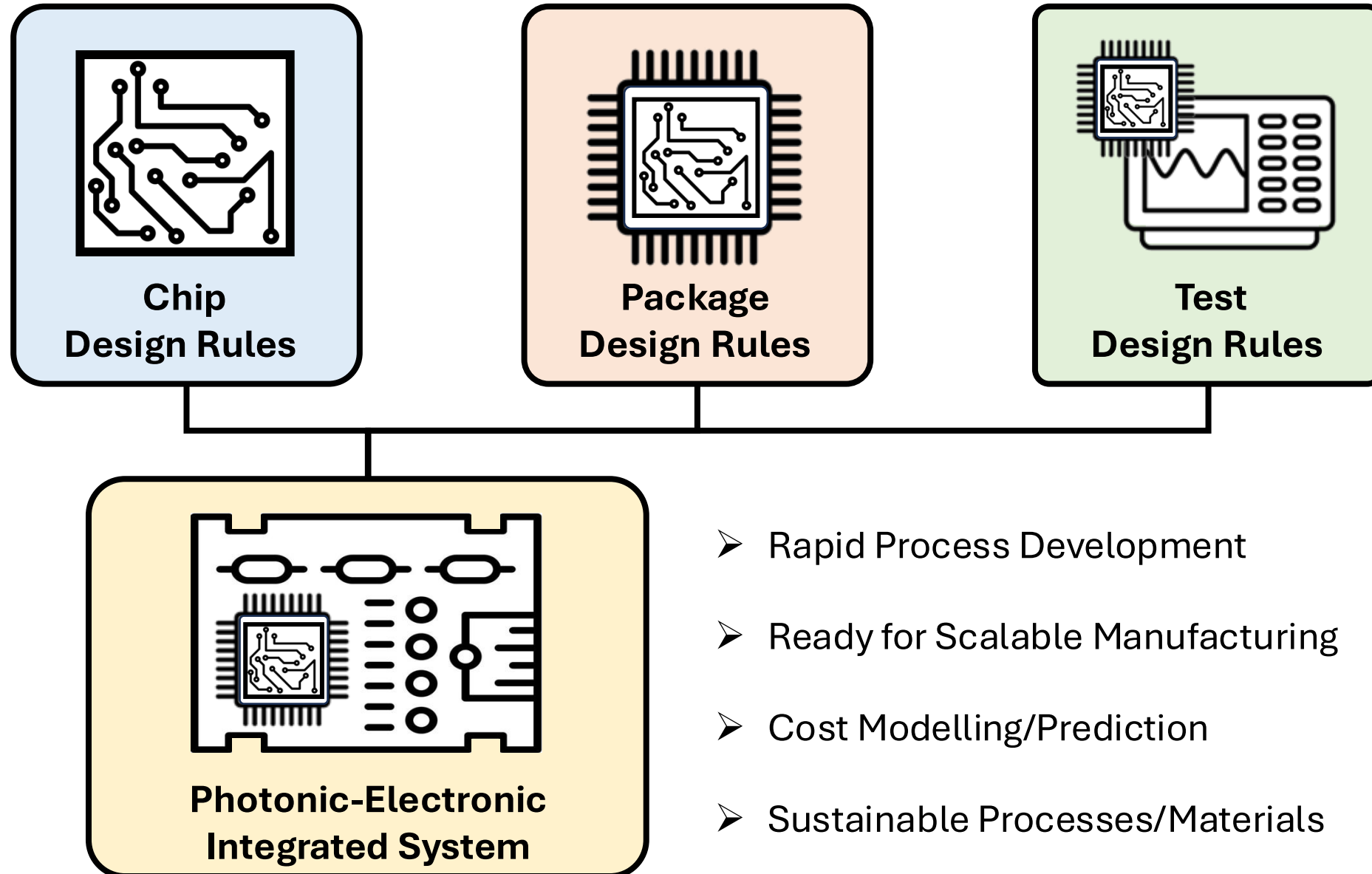


EU Chips Act (Technologies)



- **New optical packaging processes**
replace UV-cure epoxy with solder (metal & glass) bonding & direct fibre fusion
- **Scaling of 3D printing technology**
- **Standardised quantum packaging design rules & processes**

EU Chips Act (Design Standards)





PHOTONHUB[®] EUROPE

 **European Commission**

New European Academy to boost the skills and know-how of industry in exploiting opportunities in the €615B global photonics sector

Summary

- Photonic devices becoming more complex (optical, electrical, thermal, mechanical)
- Packaging design rules must be followed (software ADKs)
- Active device integration via hybrid and heterogeneous integration
- Co-packaging with electronics is an essential (2.5 & 3D integration)
- Interposers are a vital technology for co-packaging (different material choices)
- Pilot Lines are a step towards volume manufacturing (research transition & training)
- Large-scale Pilot Lines starting to better align with OSATs for volume packaging