
Solid-liquid interdiffusion (SLID) – A novel interconnection method for MEMS, power and RF devices

Professional development course
IEEE ESTC 2026

Table of contents

- Introduction:
 - Packaging/Advanced Packaging
 - Interconnects – Challenges, solutions, gap between FC and HB
- Solid liquid interdiffusion (SLID) bonding
 - Introduction
 - Thermomechanical stresses
 - SLID metallurgy and contact metallization
- SLID electrical performance – Electromigration and RF
- Application areas:
 - SLID for MEMS – Contact metallization, process development, hermeticity, challenges and solutions
 - SLID for Power Electronics – Die attach, double sided cooling, thermomechanical stresses, electrical
- Conclusion

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Advanced Packaging

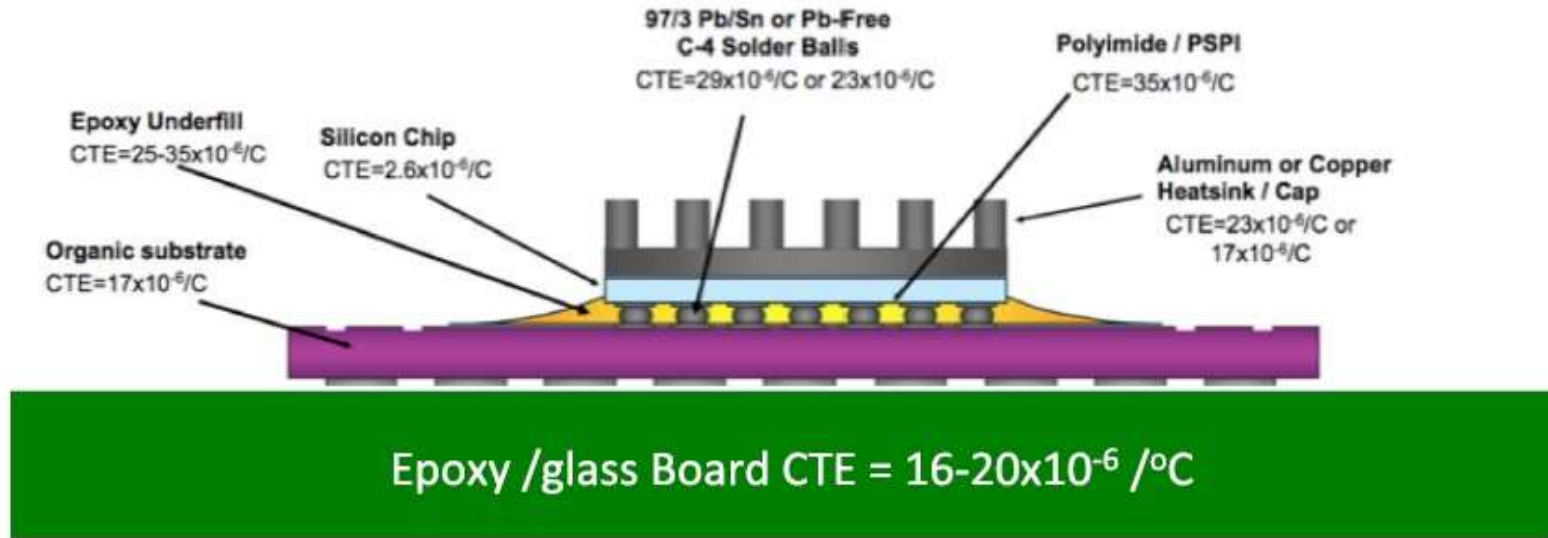
Interconnects – Challenges, solutions, gap between
Flip-Chip and Hybrid Bonding

What is packaging?



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What is packaging?

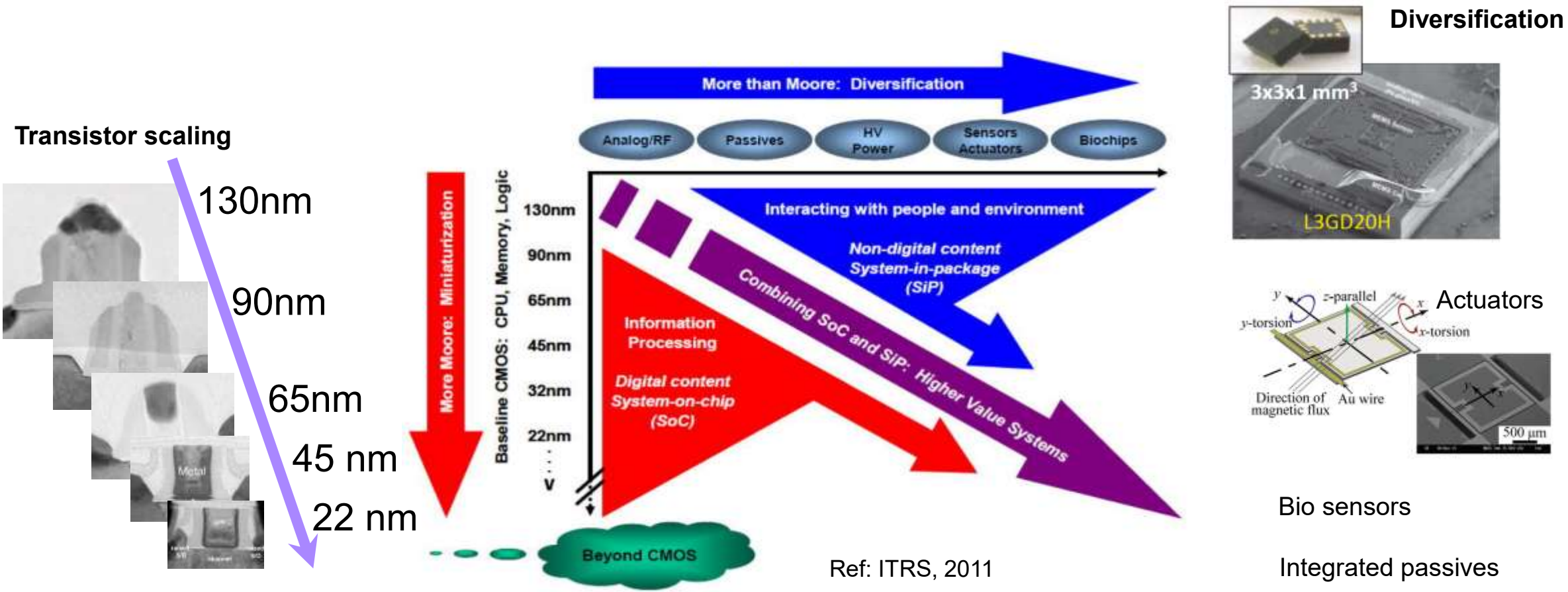


S. S. Iyer, IEEE TCPMT, vol. 6, pp. 973-982, 2016

- **Functions:**
 - Mechanical support
 - Protection from external environment
 - Electrical connections
 - Routing of I/Os via space transformation
 - Thermal management
- **Electrical performance should not deteriorate** – Signal integrity and power integrity
- **Several materials with different CTE values** – Thermomechanical reliability

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Microelectronic technologies – The present

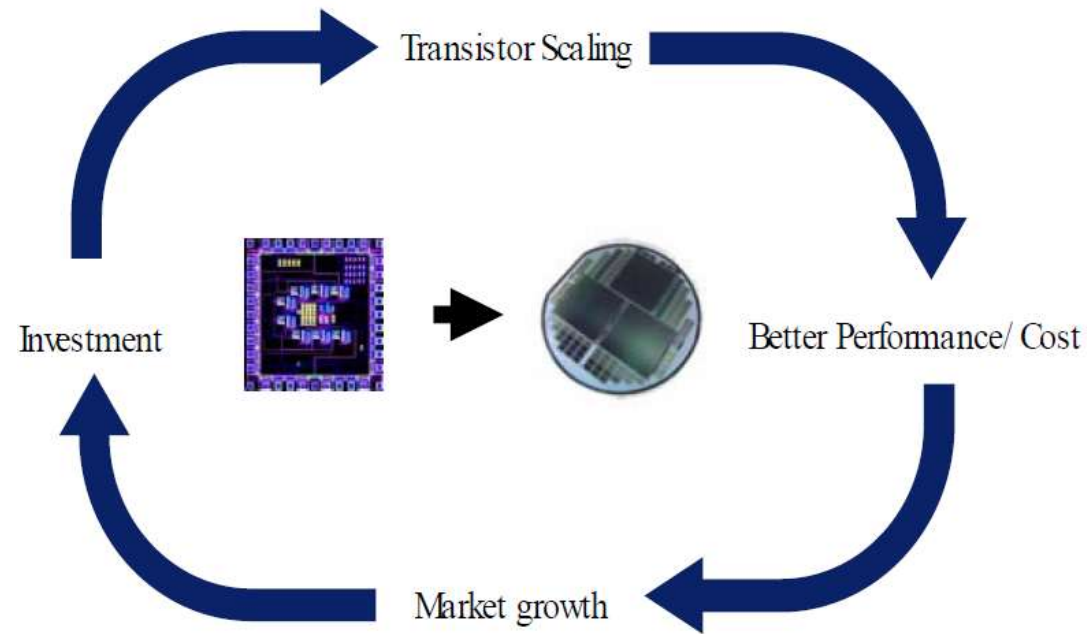


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Ref: IEEE Internet of Things – The Hardware Enablers for the Internet of Things – Part II (More than Moore) ONLINE

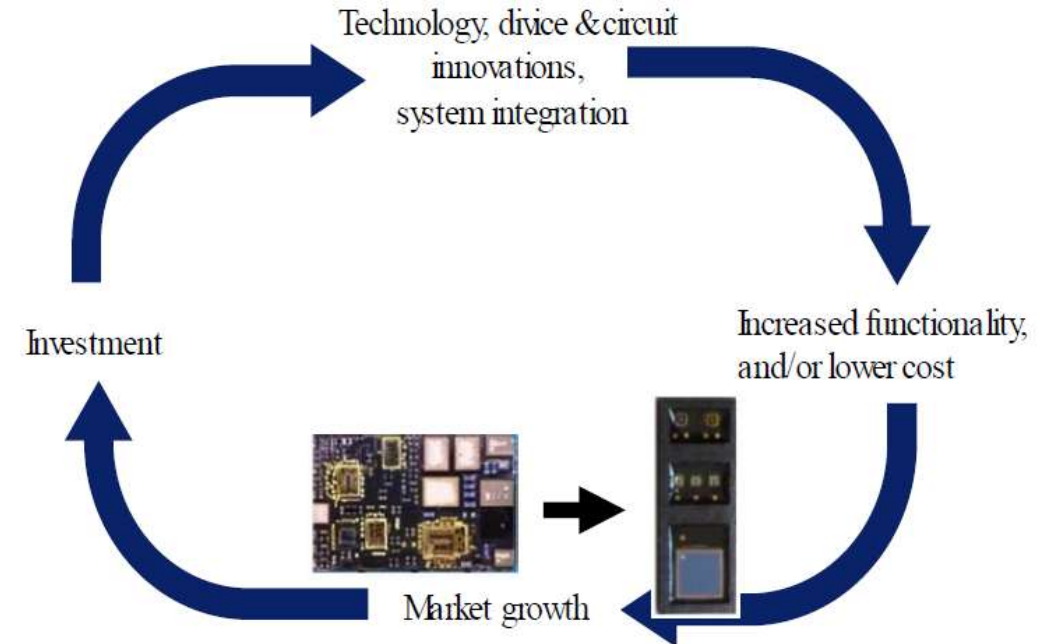
Ref: IEEE-Sensors 2013 – Design and Analysis of MEMS Gyroscopes

Transistor focus vs System focus



Transistor Focus

Integration with a transistor focus



System Focus

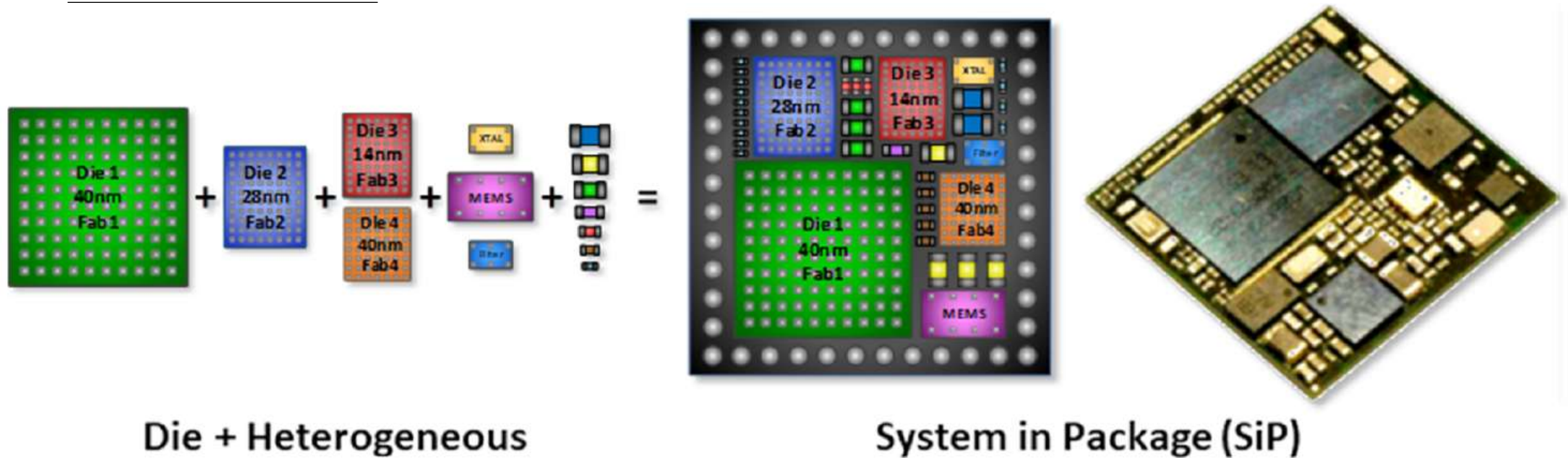
Integration with a system focus

A!

Ref: Heterogeneous Integration Roadmap 2019 Edition Chapter 1 Overview

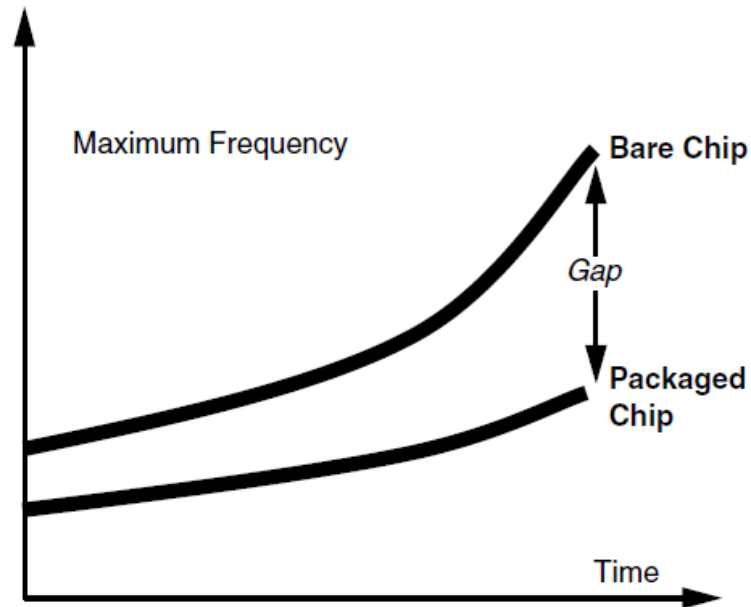
Heterogeneous Integration?

- It refers to the integration of separately manufactured components into a higher-level assembly (System in Package – SiP) that, in the aggregate, provides enhanced functionality and improved operating characteristics.



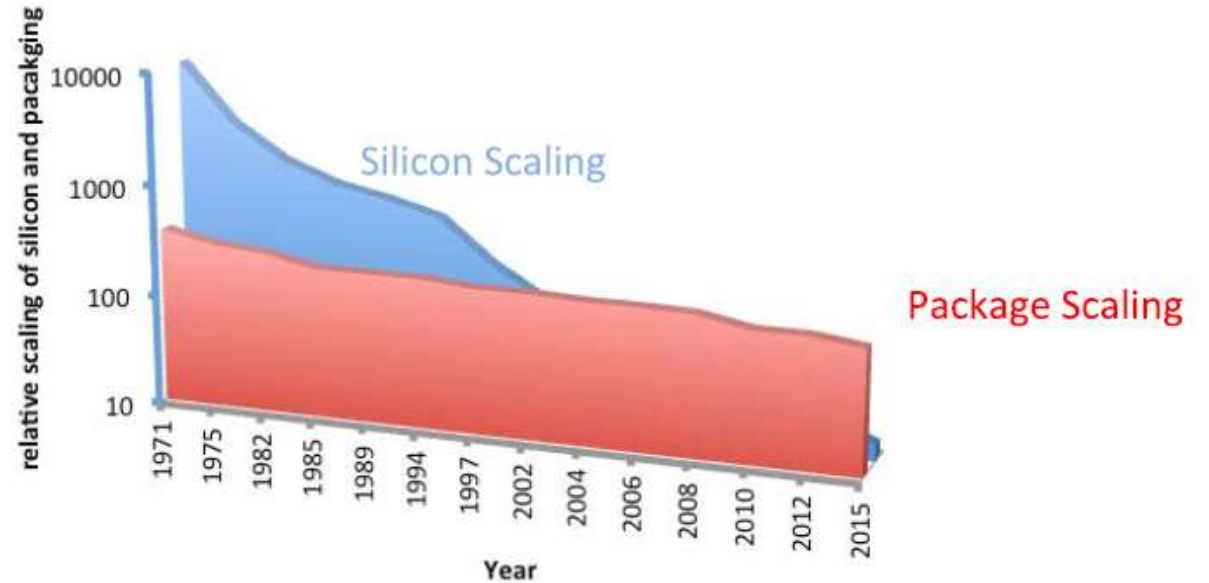
A!

Heterogeneous integration challenges



IC Packaging performance gap

Rao Tummala, "Fundamentals of Microsystems Packaging", 1st edition, McGraw Hill, 2001

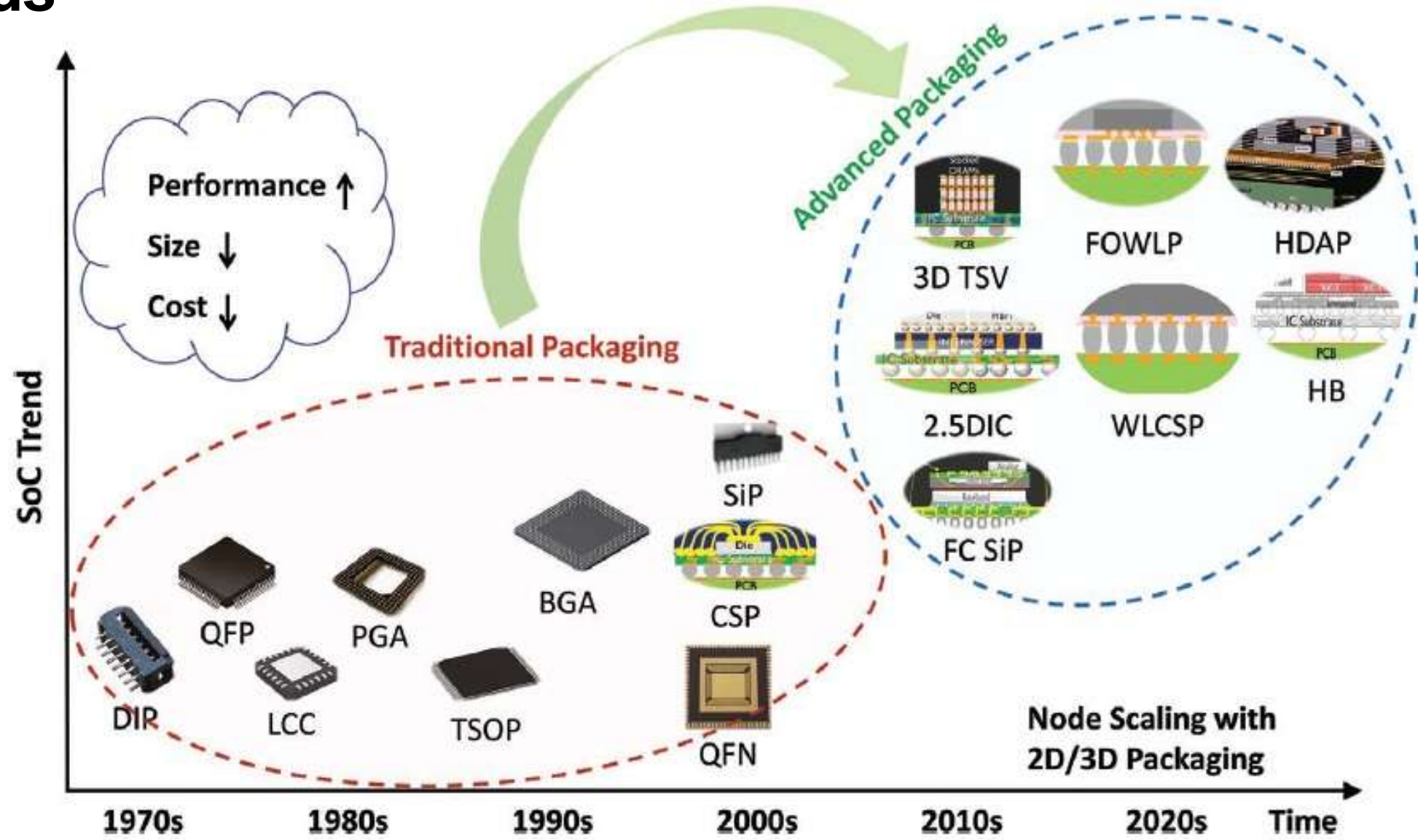


S. S. Iyer, IEEE TCPMT, vol. 6, pp. 973-982, 2016

1. Electrical performance of the chips in a package should be within the specifications
2. Dense architectures requires significant consideration of the bandwidth, signal integrity, power integrity, crosstalks, losses, EMI/EMC etc.

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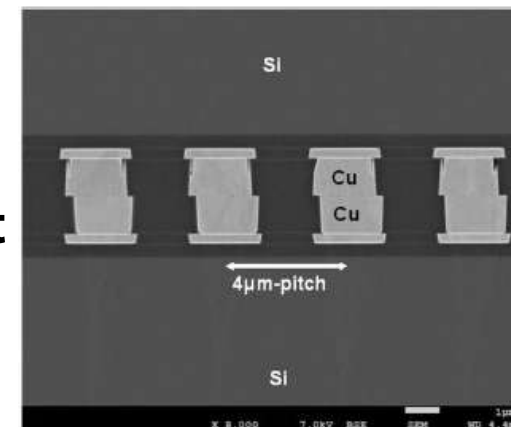
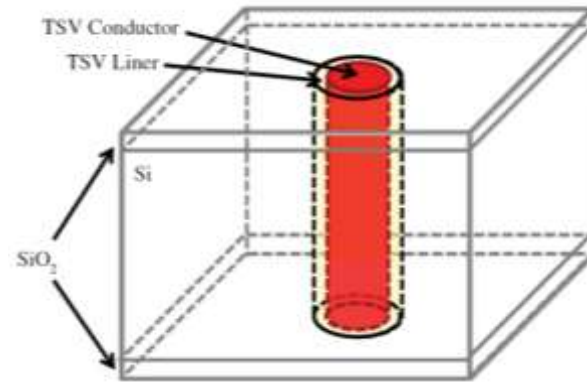
Trends



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Interconnections

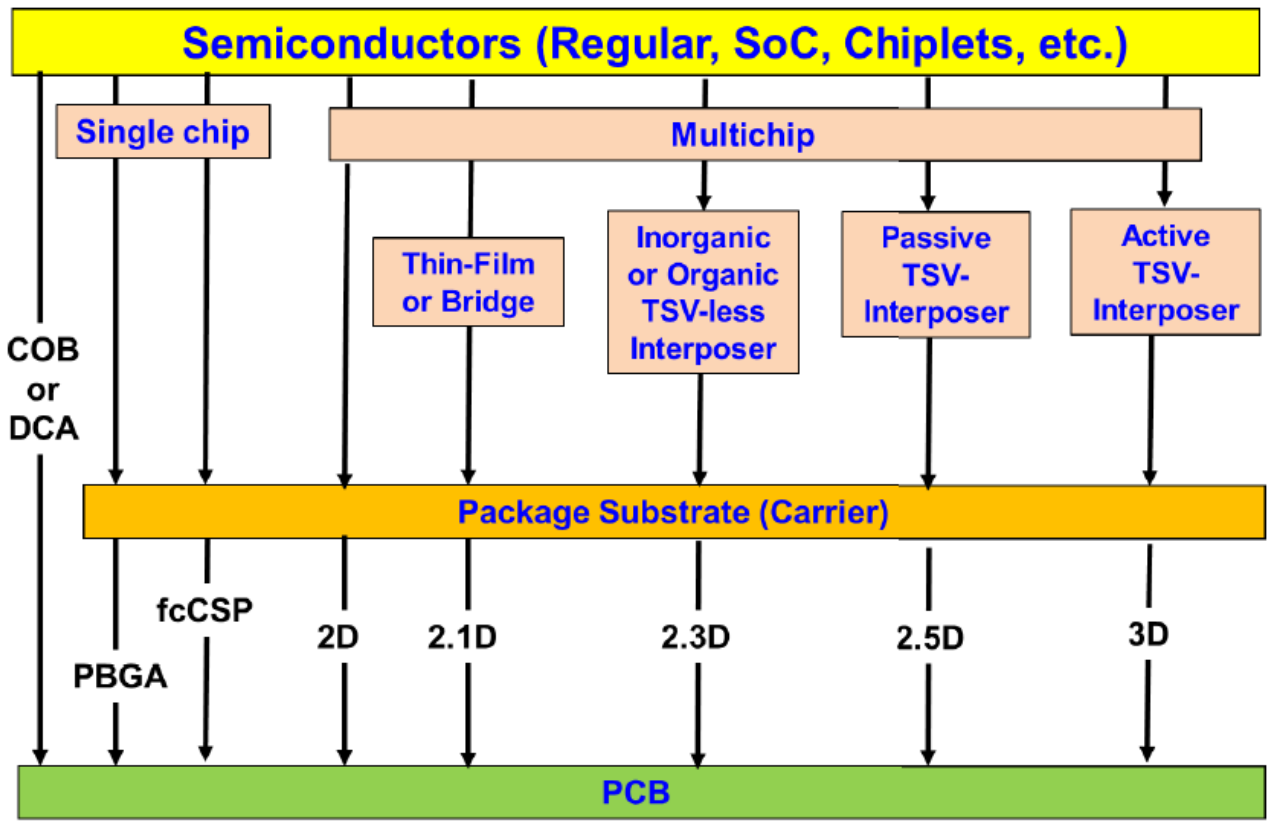
- Wirebonds
- Solder balls – Ball Grid Array (BGA)
- Flip chip – C4
- Through silicon vias
- Bumpless/hybrid bonds/direct bond interconnect



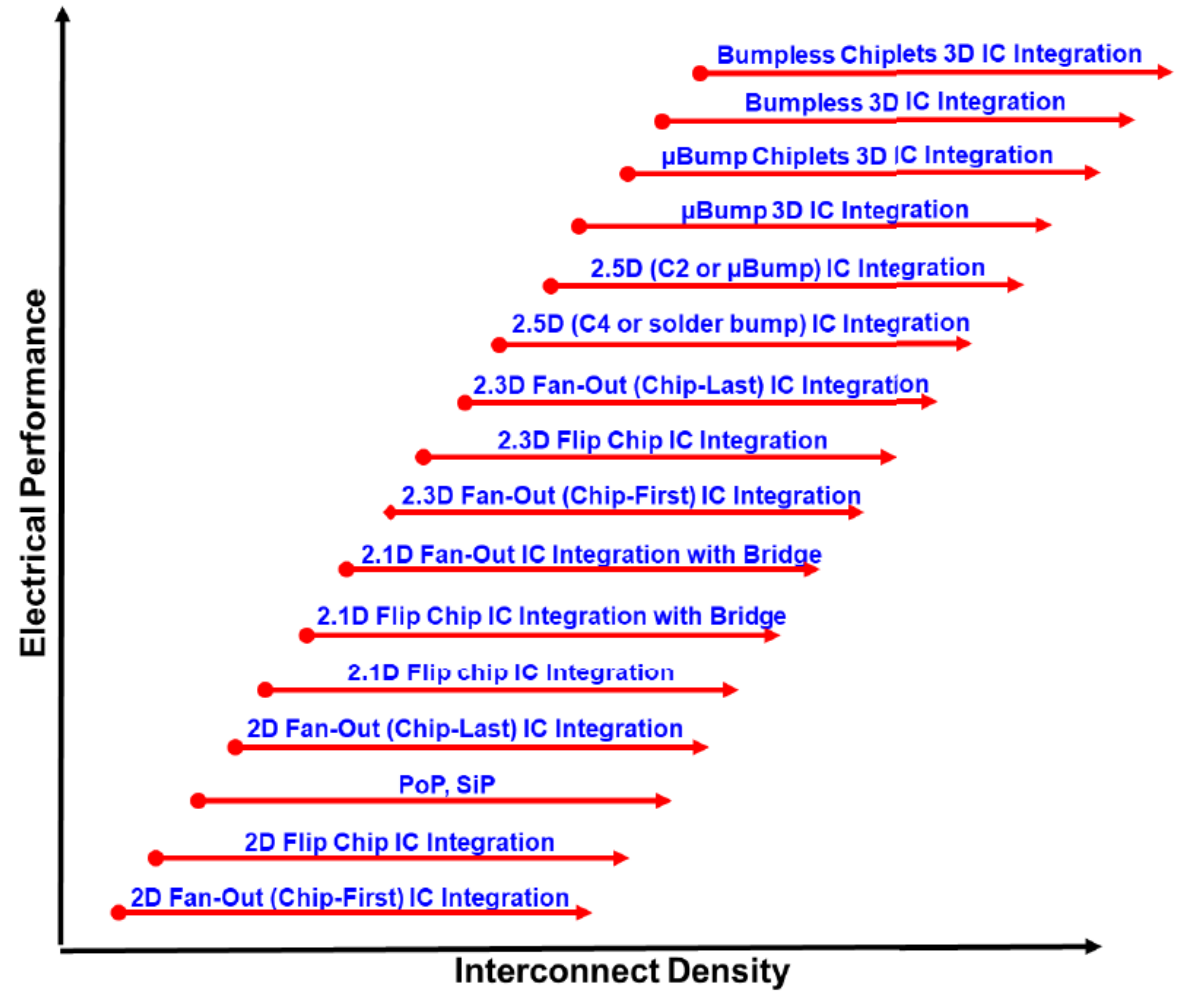
**Interconnect
density
increases**

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Advanced packaging groups and ranking



Groups of Advanced Packaging

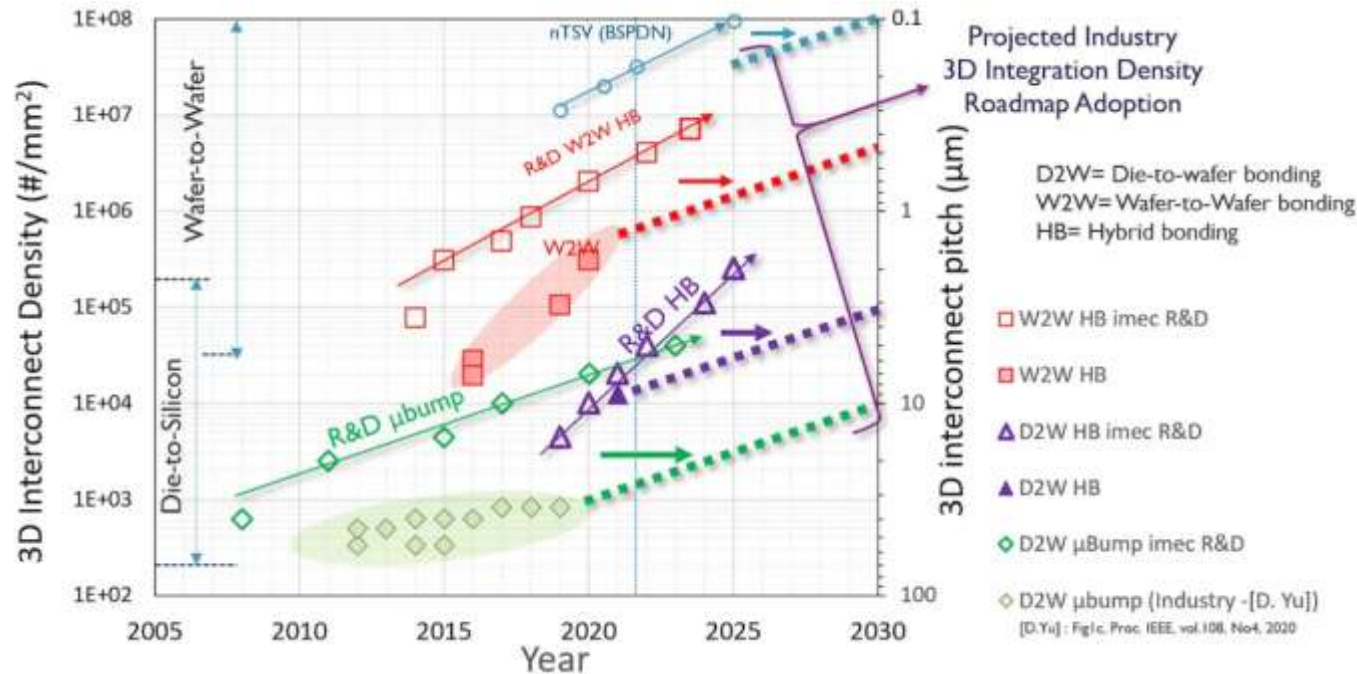


Advanced Packaging ranking according to interconnect density and electrical performance

Bonding technologies

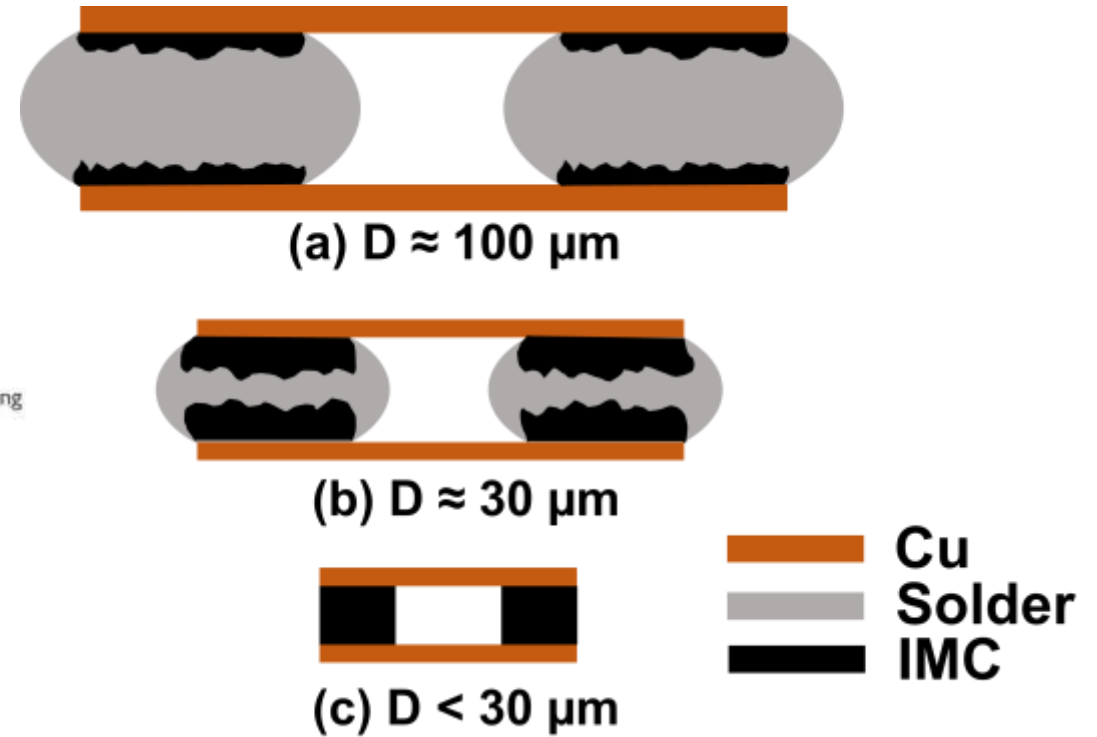
- **Stacking chips requires bonding technologies**
 - **MEMS chips often requires hermetic encapsulation**
 - **Requirements are low bonding temperature, low process dependent thermomechanical stresses, high electrical and thermomechanical reliability**
 - **Several types:**
 - Direct bonding
 - Anodic bonding
 - Glass frit bonding
 - Thermocompression bonding
 - Solid liquid interdiffusion bonding
- Requires high temperature $\approx 400\text{ }^{\circ}\text{C}$ or more
-
- Low temperature bonding possible
 - Metallic bonds – functions as interconnects
 - Hermetic encapsulation
 - Favorable for high temperature applications

Interconnects roadmap, issues and potential solutions



The 3D interconnect IMEC R&D roadmap

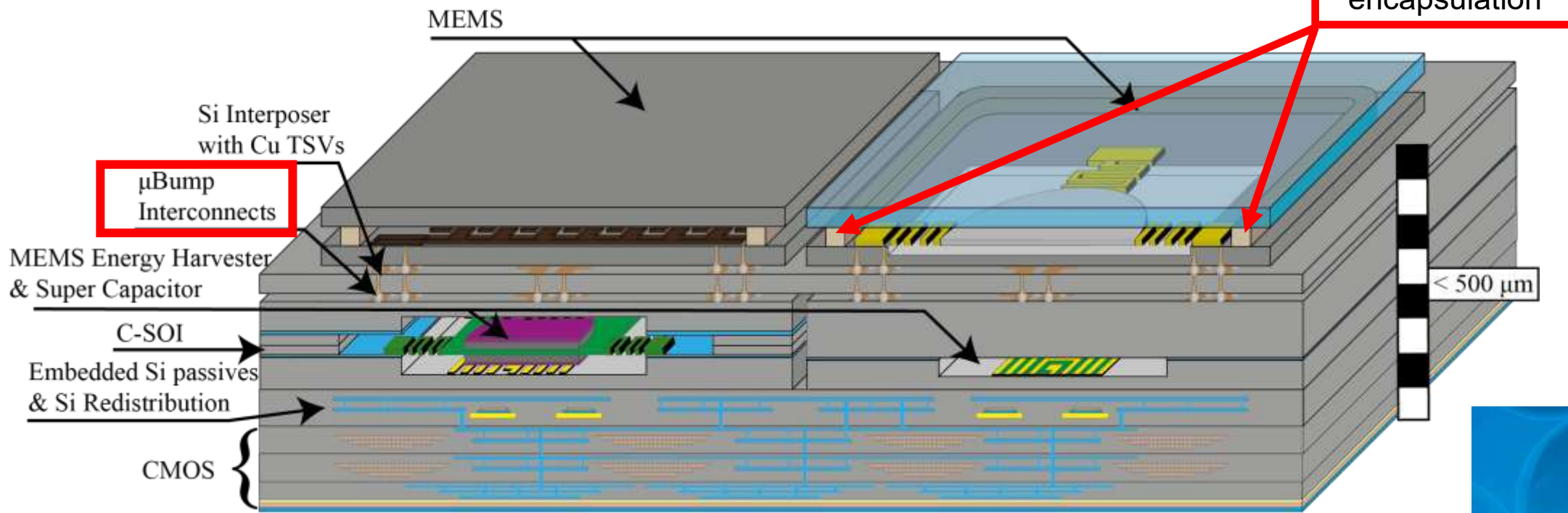
Ref: [A view on the 3D technology landscape | imec \(imec-int.com\)](https://imec-int.com)



Ref: N. Tiwary et al., *IEEE Trans. Electron Dev.*, vol. 70, pp. 222-229, 2023

- **SLID μbumps** offers possibilities to fill the gap between FC μbumps and hybrid bond
- **Advantages:** wafer-level bonding, low resistance, higher EM reliability, hermetic encapsulation, lower bonding temperature, lower thermomechanical stress
- **Attractive technology for 3D HI**

Motivation – “all-silicon package”



➤ How to reliably bond materials with dissimilar thermomechanical properties?

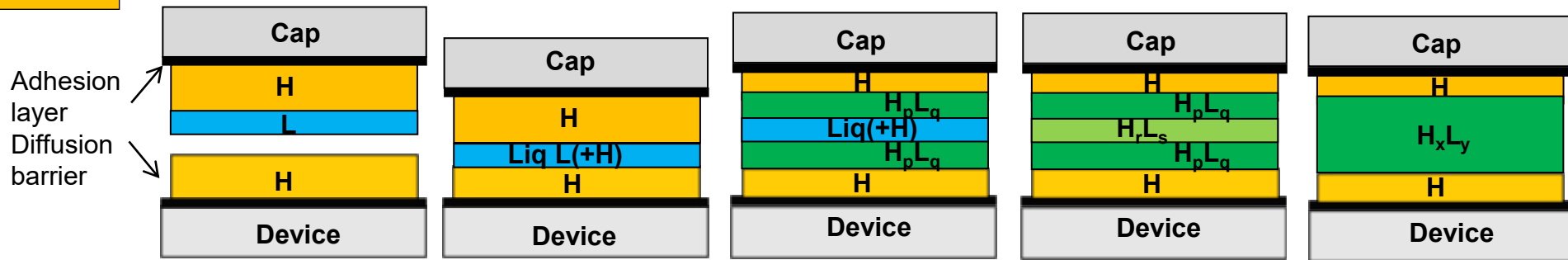
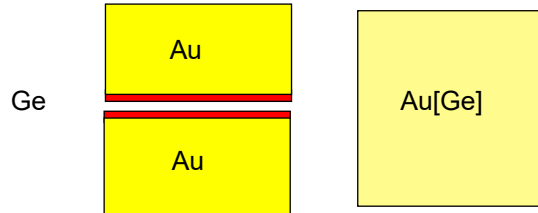
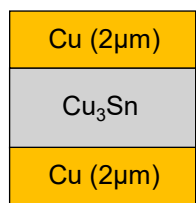
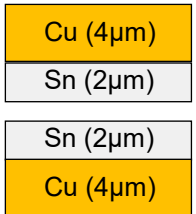
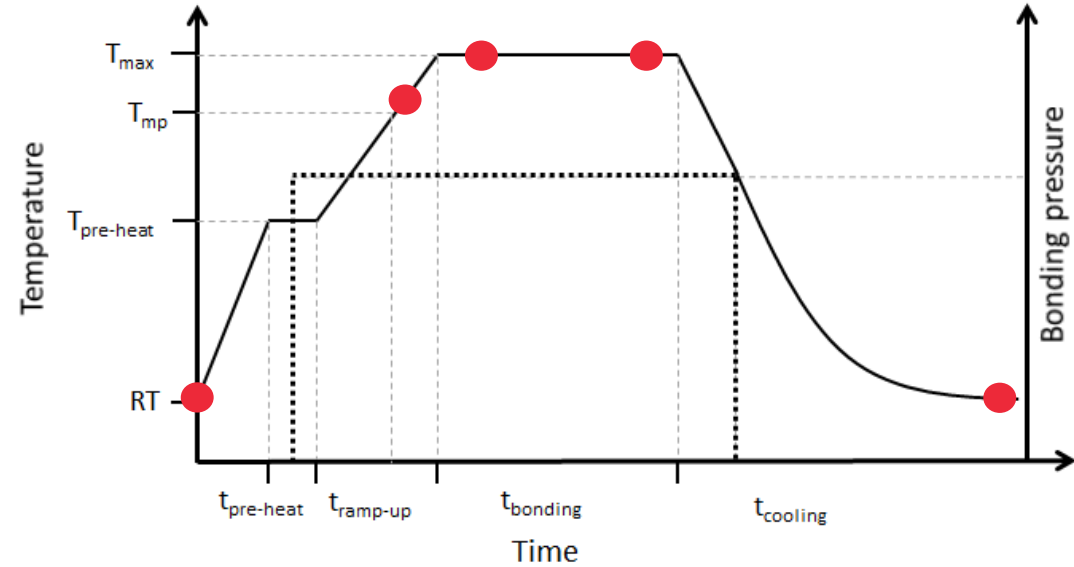
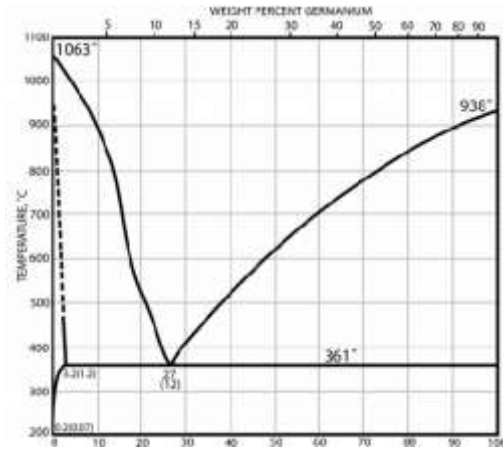
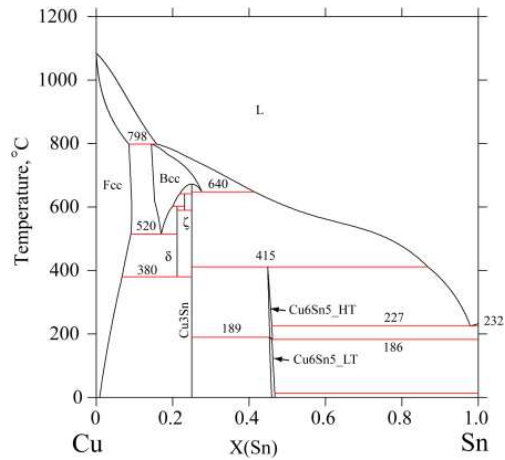
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Ref: Handbook of Si MEMS, 3rd edition



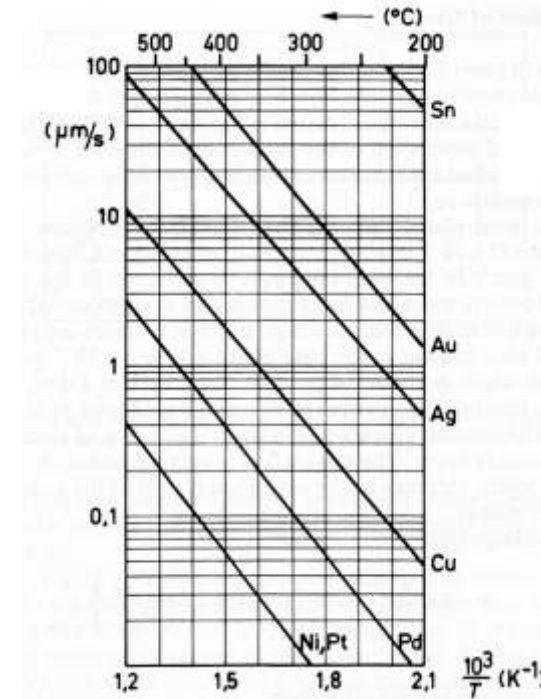
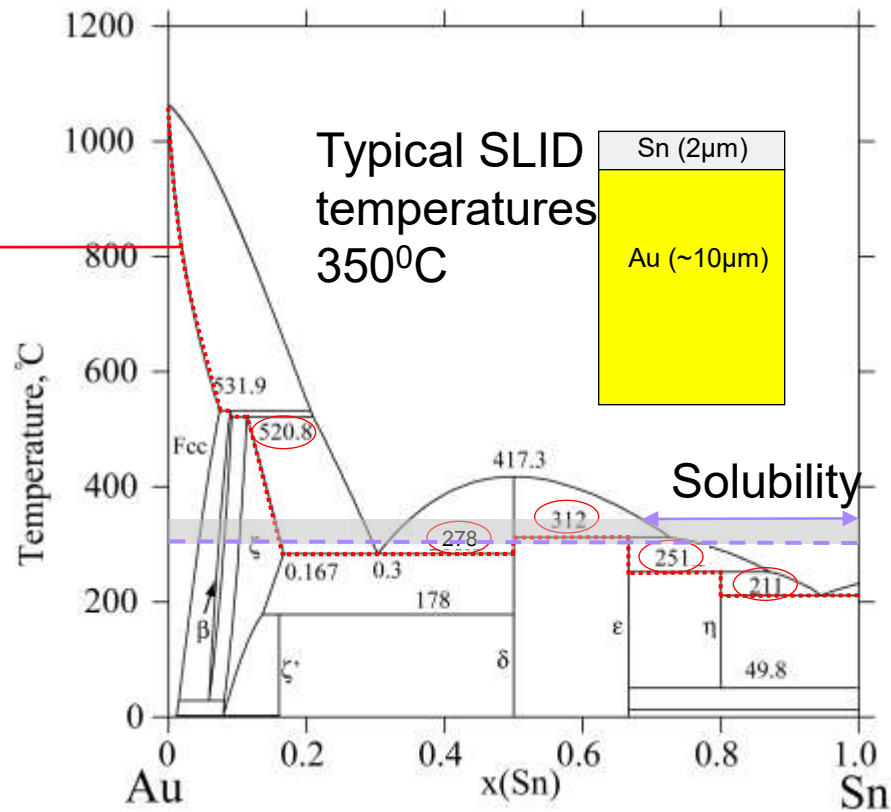
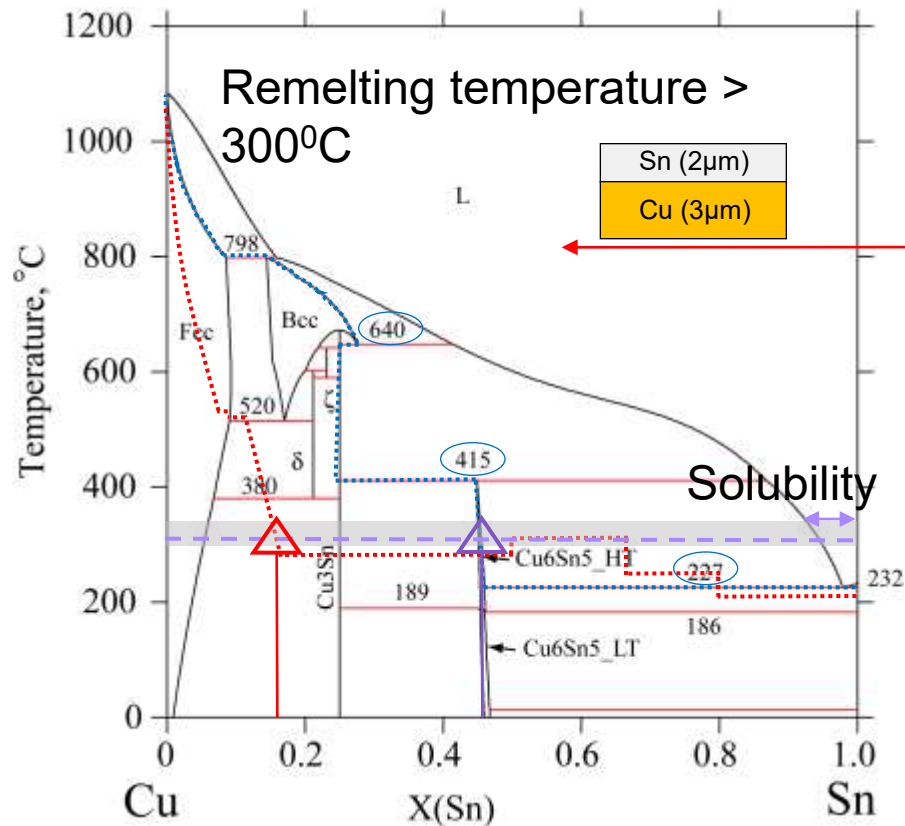
SLID introduction

What is Solid Liquid Interdiffusion SLID/TLP bonding? aka. Diffusion soldering



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The most commonly used Cu-Sn and Au-Sn metallurgies- “HT-SLID”



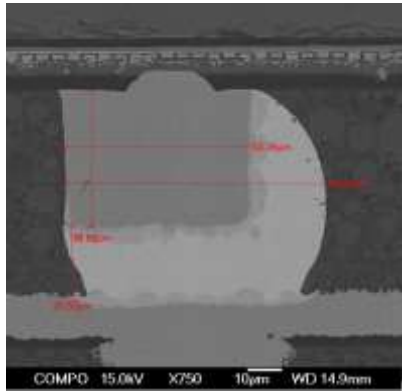
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SLID/TLP bonding - Where & Why?

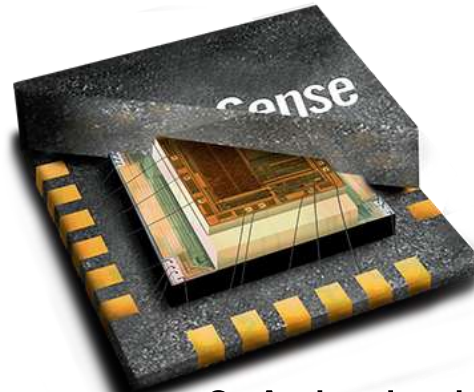
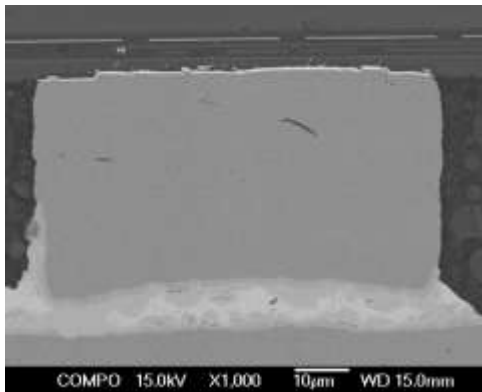
μ -bonds/ μ -bumps

MEMS/MOEMS

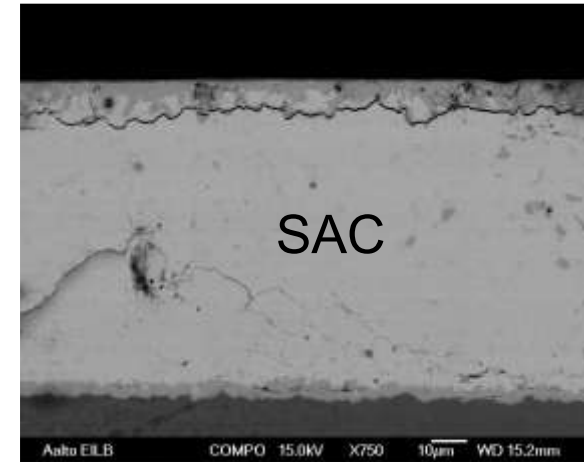
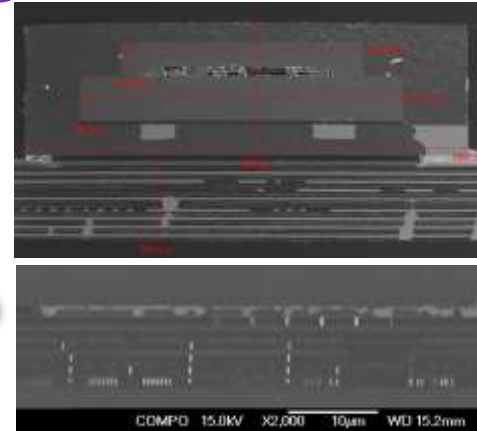
Power electronics



S8 processor & FBAR



9-Axis device
invensense.tdk.com



	T_{mp}	E	H	CTE	k	ρ
Sn	232°C	41GPa	41MPa	23ppm	63W/mK	$11.5 \times 10^{-8} \Omega m$
Cu	1083°C	117GPa	369MPa	17ppm	398W/mK	$1.7 \times 10^{-8} \Omega m$
Au	1064°C	77GPa	216MPa	14ppm	301W/mK	$2.4 \times 10^{-8} \Omega m$
Cu ₃ Sn	640°C (415°C)	108GPa	~3400MPa	19ppm	70W/mK	$8.9 \times 10^{-8} \Omega m$
Au ₅ Sn	522°C (278°C)	~70GPa	745MPa	18ppm	57W/mK	$16.4 \times 10^{-8} \Omega m$ (eut)

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WL+

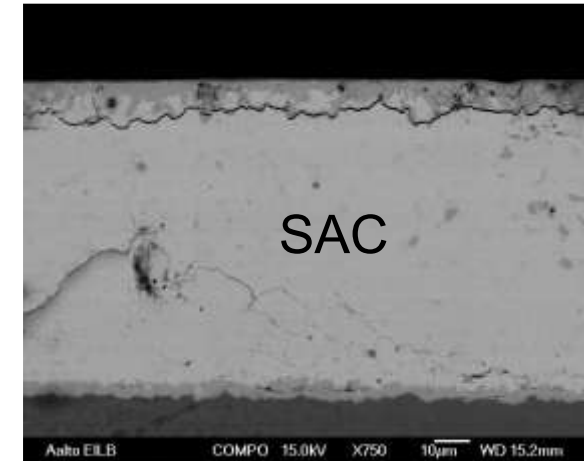
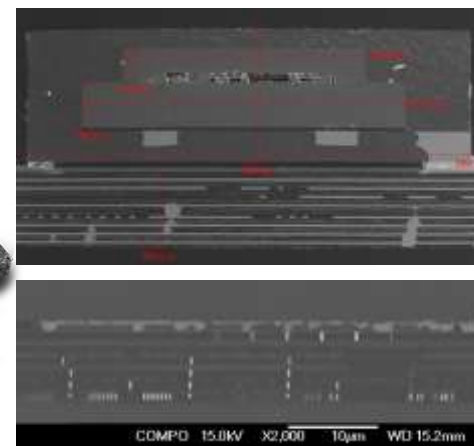
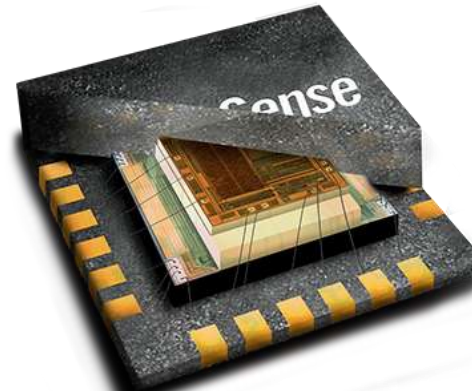
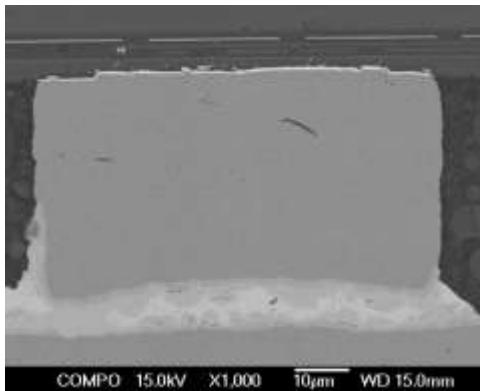
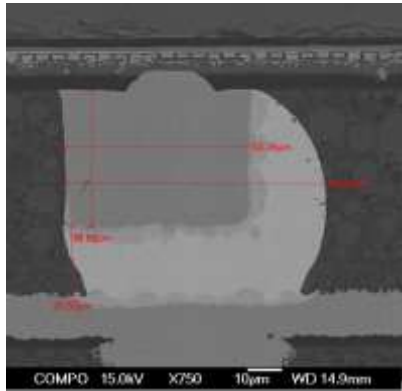
Small footprint, tolerance for topographies and surface contaminations, excellent hermeticity

Where & Why? – High thermal stability

μ -bonds/ μ -bumps 3D integration

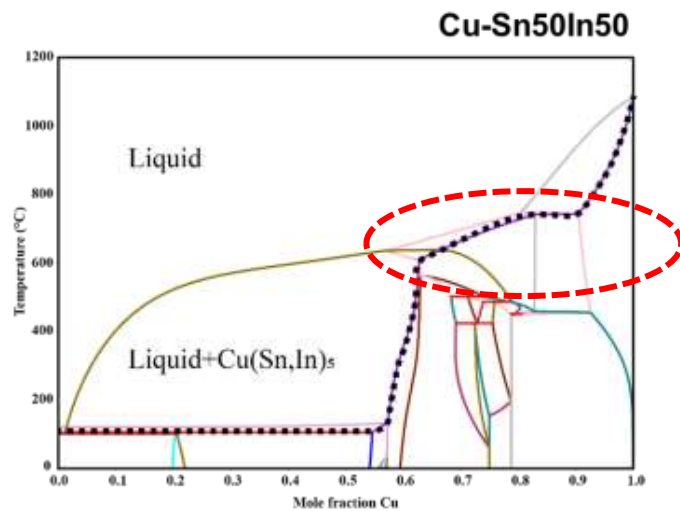
MEMS/MOEMS

Power electronics –
Die attach

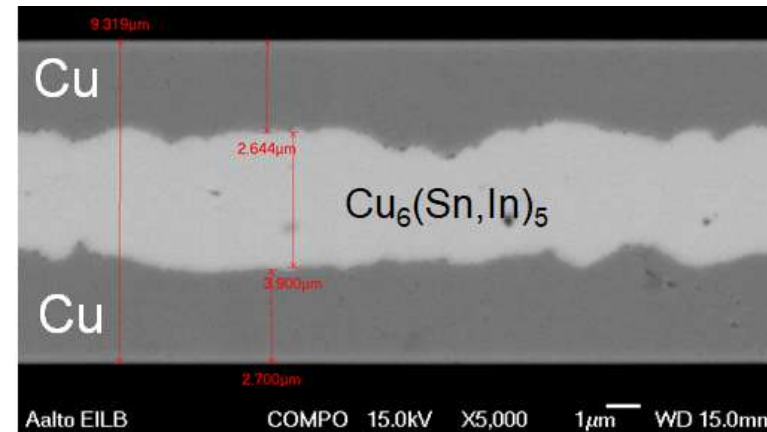


S8 processor & FBAR

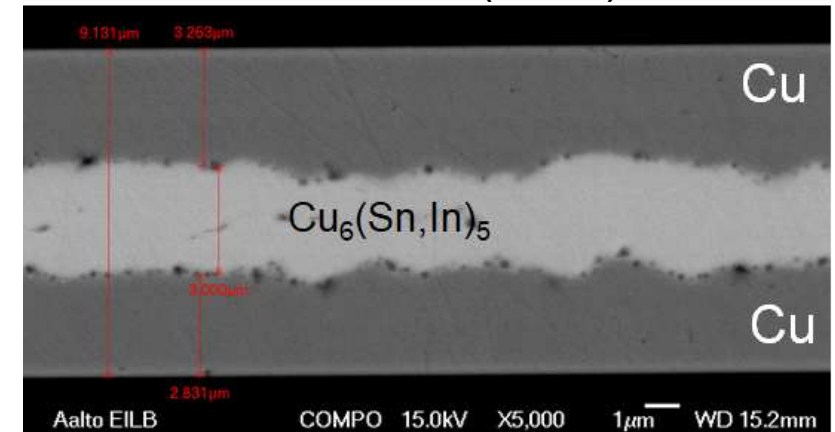
9-Axis device



As bonded (60min@200°C)



HTS 150°C for 21d (504h)

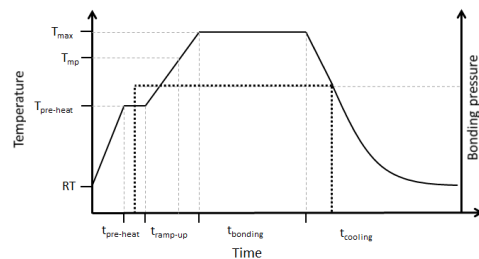
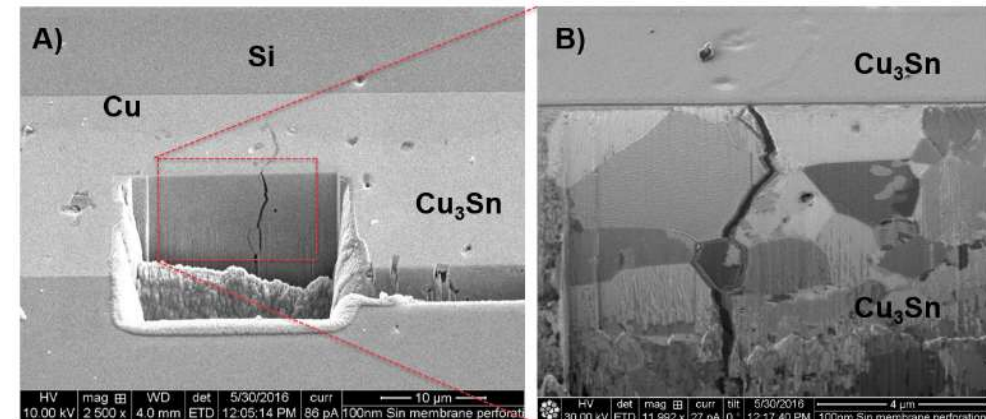
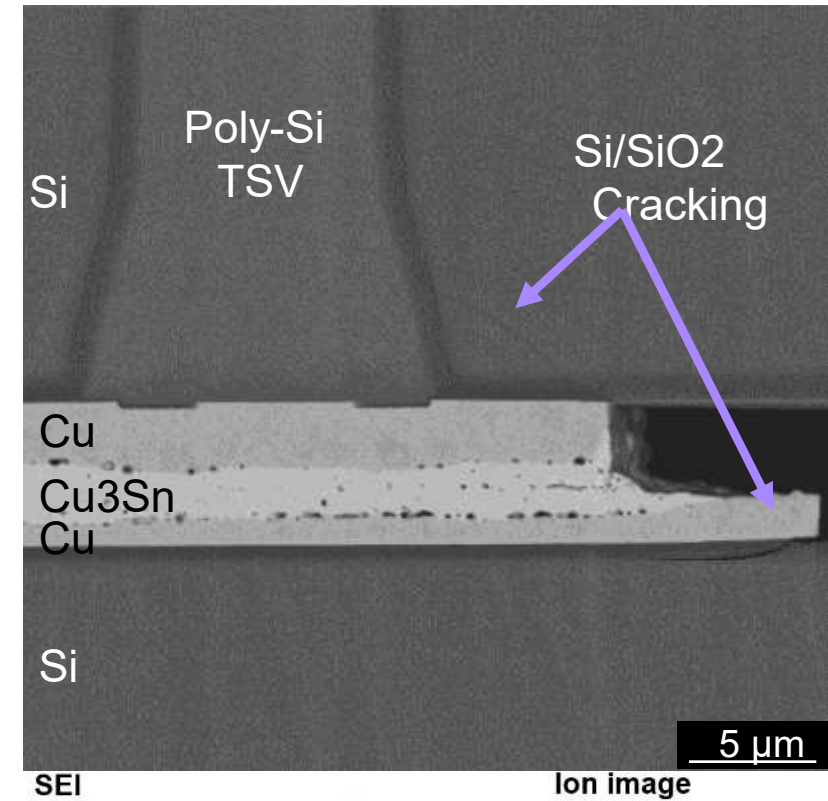
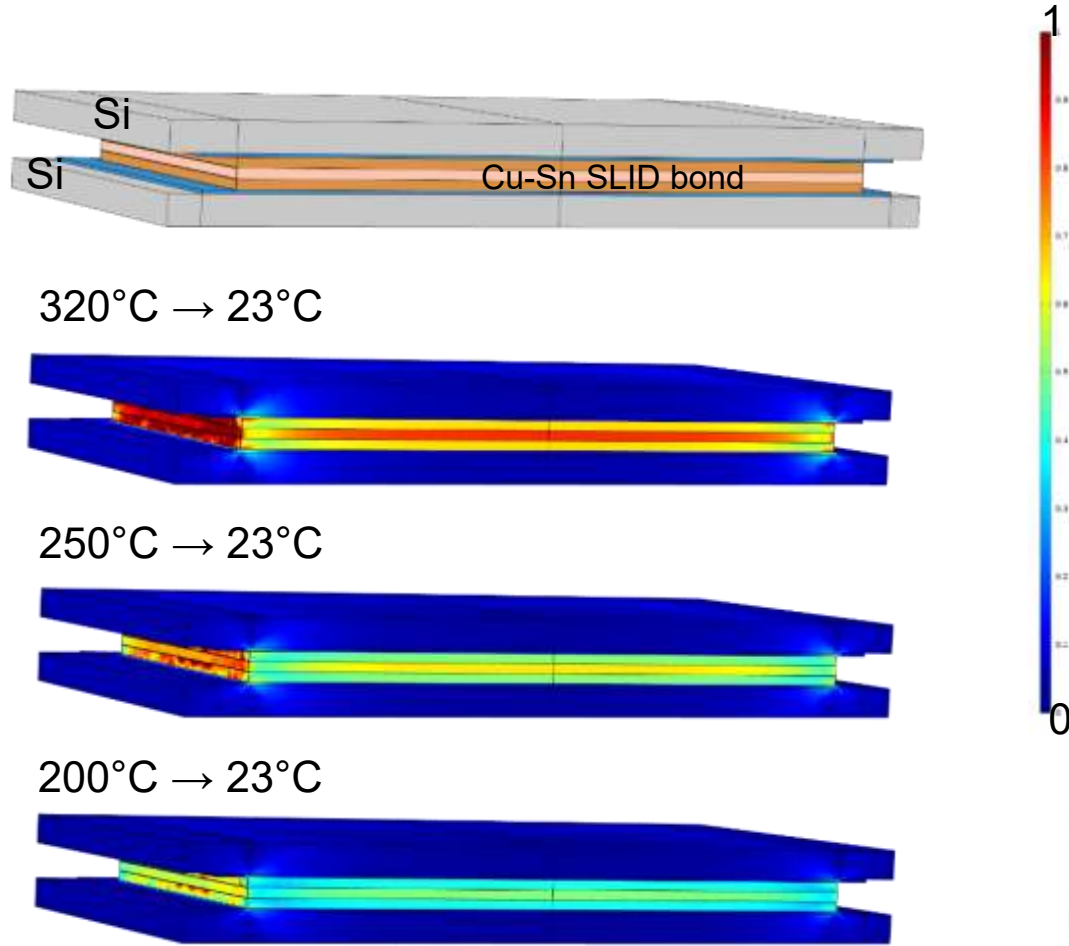


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Small footprint, tolerance for topographies and surface contaminations, excellent hermeticity

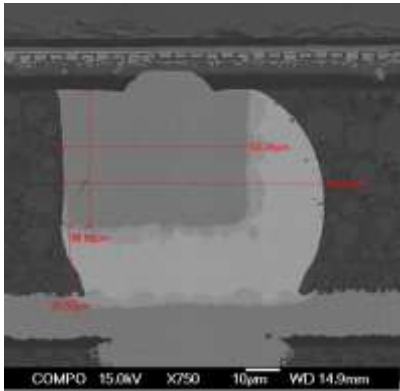
Thermomechanical challenges of “HT-SLID”



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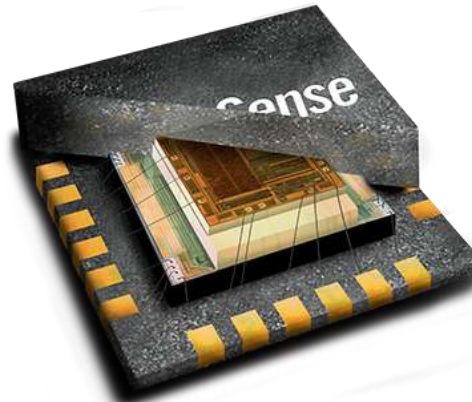
Where & Why? – Low processing temp.

μ -bonds/ μ -bumps 3D integration

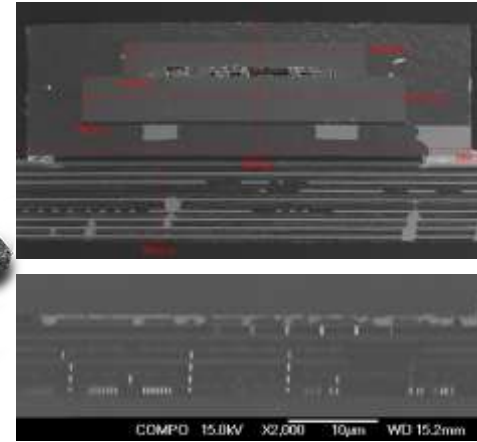


S8 processor & FBAR

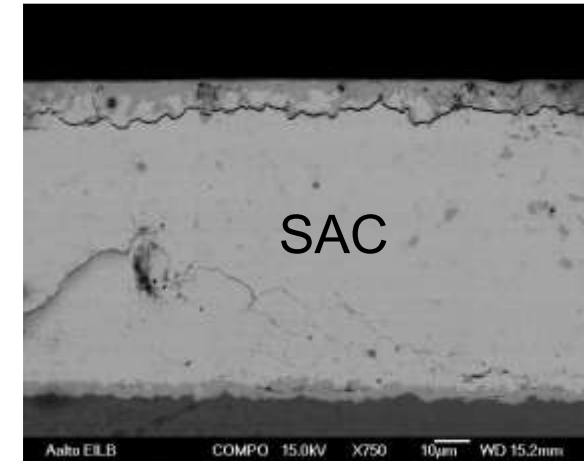
MEMS/MOEMS



9-Axis device

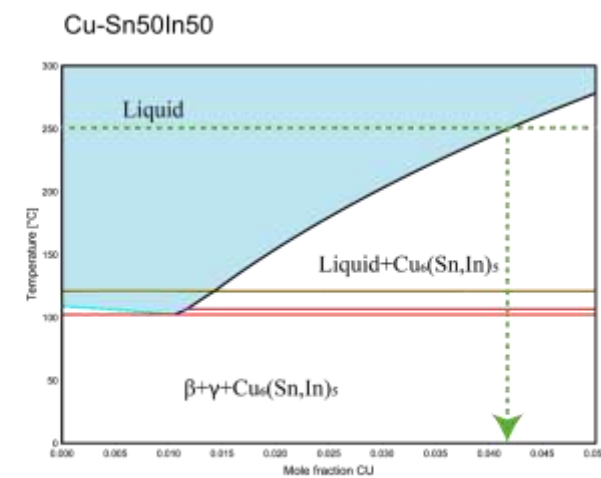
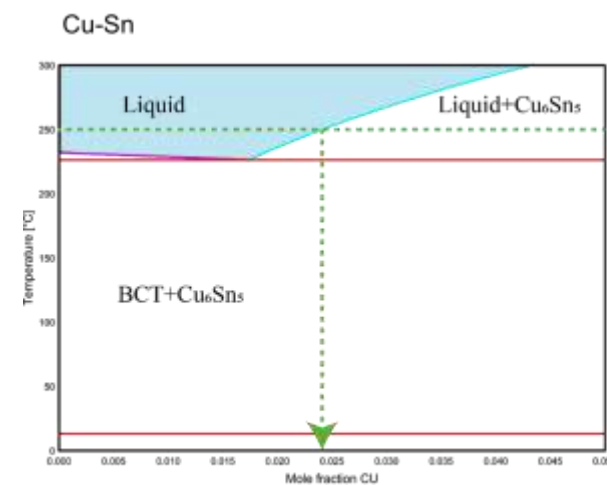
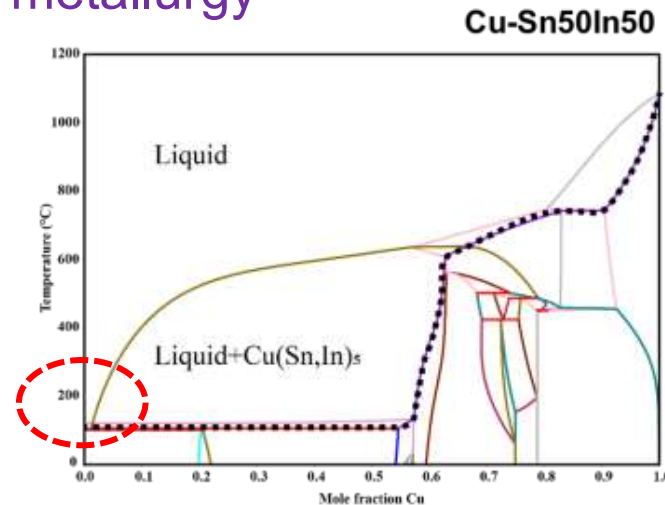
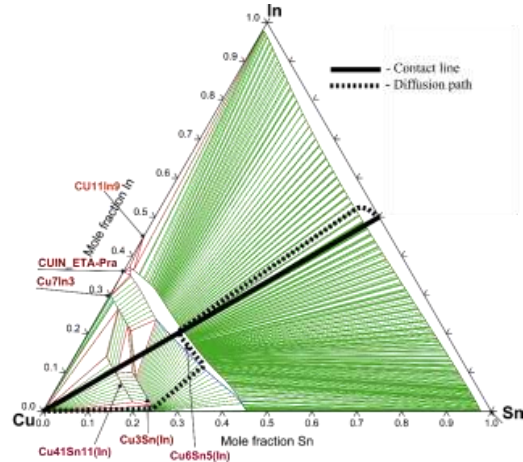


Power electronics –
Die attach



SAC

Cu-In-Sn metallurgy



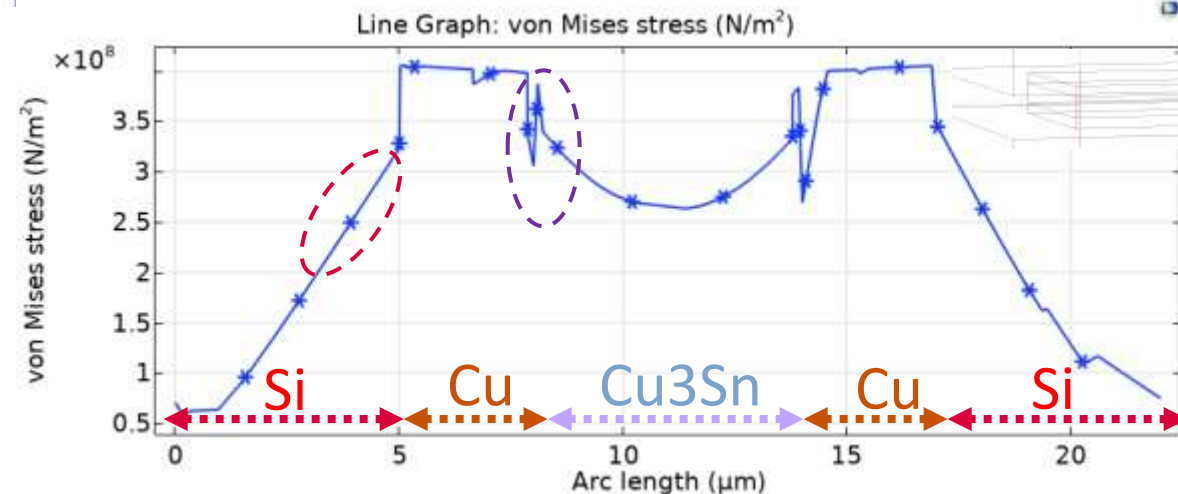
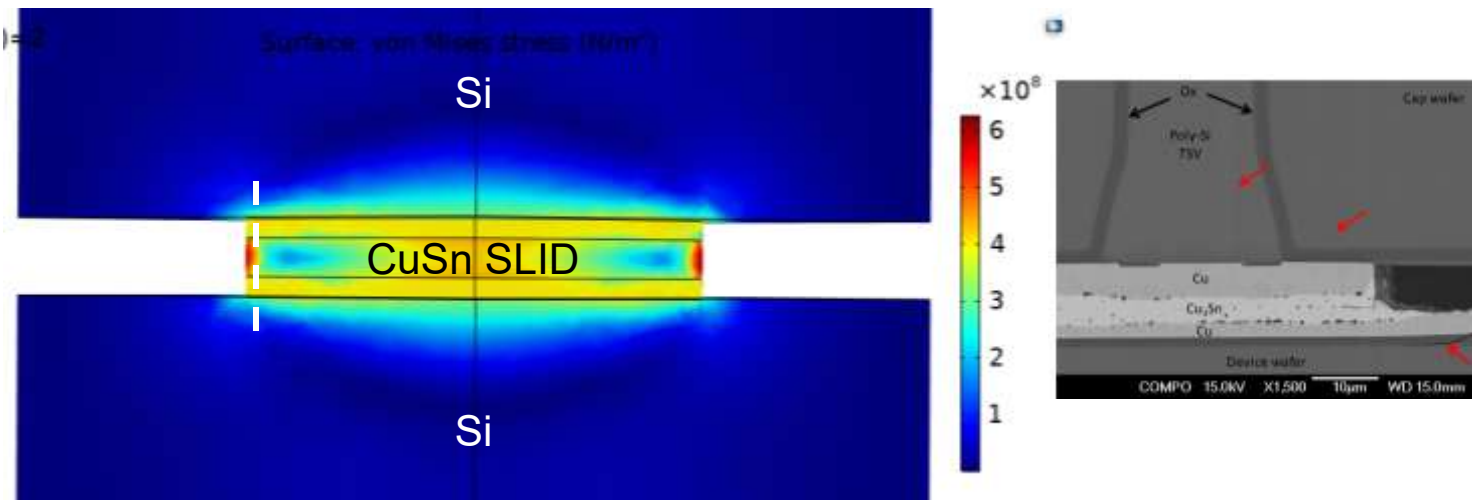
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Ref: V. Vuorinen, G. Ross, A. Klami, H. Dong, M. Paulasto-Kröckel, T. Wernicke, A. Pönninger, Demonstrating 170°C Low Temperature Cu-In-Sn wafer level Solid Liquid Interdiffusion Bonding, IEEE Components, Packaging and Manufacturing Technology, pp. 1-8, 2021

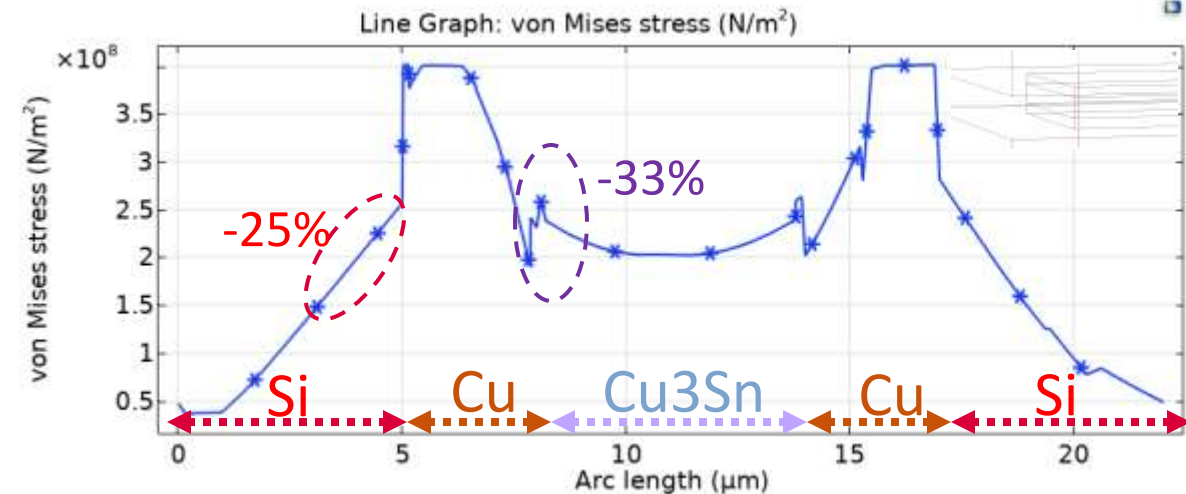
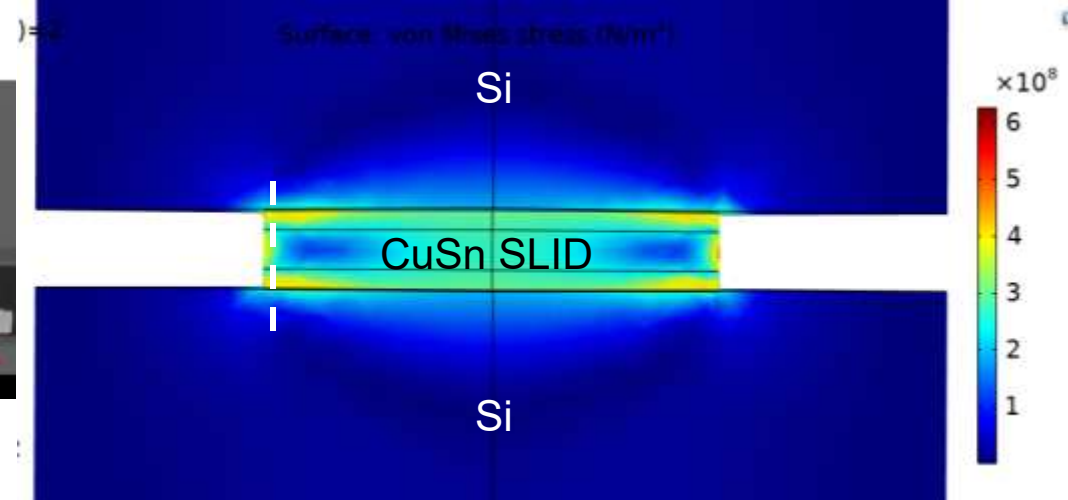
FE Simulations of LT-SLID bonding process

- Simulate the LT-SLID wafer bonding process (Si-Si, Si-Glass, Si-DBC, etc.) to understand the residual stress formation on bonding parameters such as, temperature, pressure and ramp-rate.
- Crucial for reliability analysis of interconnects, hermetic encapsulation, SiP and heterogeneous SoC solutions for power electronics, MEMS and optical modules.

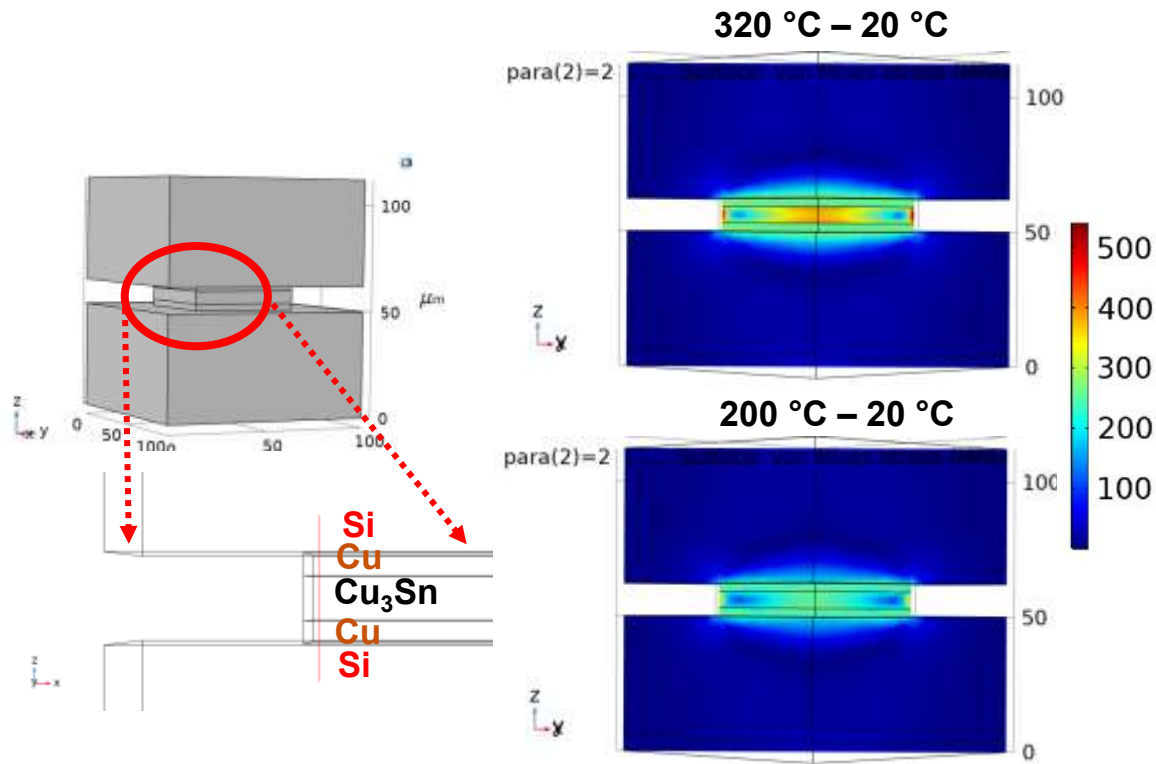
320°C → 20°C



200°C → 20°C



Low temperature (LT) SLID

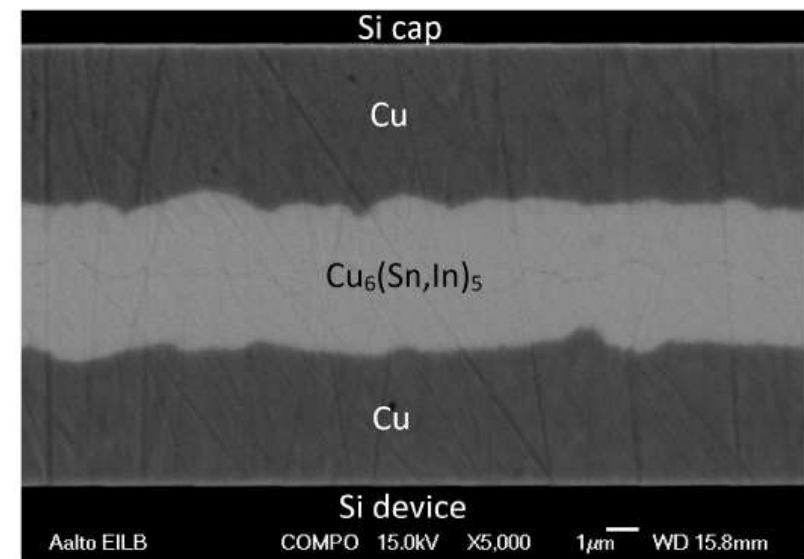


Ref: N. Tiwary *et al.*, *IEEE Trans. Comp. Packag. Manufac. Technol.*, vol. 12, pp. 847-856, 2022

Importance of LT-SLID:

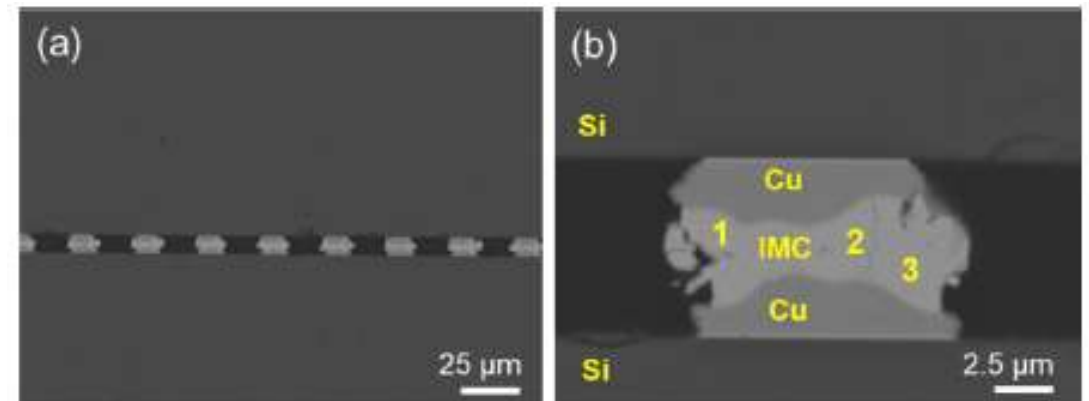
- Reduced bonding temperature -> reduced stresses
- Higher reliability

A!



Cu-Sn-In LT-SLID bonding demonstrated at 170 °C

Ref: V. Vuorinen *et al.*, *IEEE Trans. Comp. Packag. Manufac. Technol.*, vol. 12, pp. 446-453, 2022

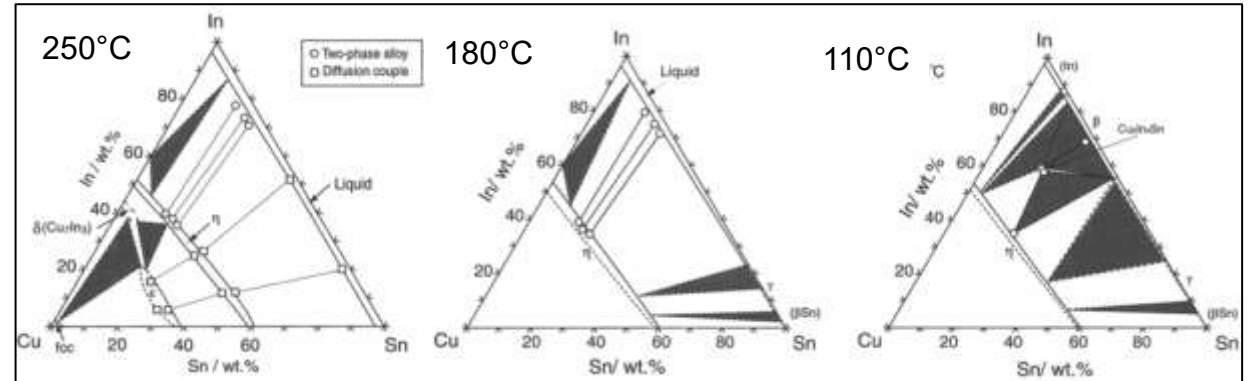
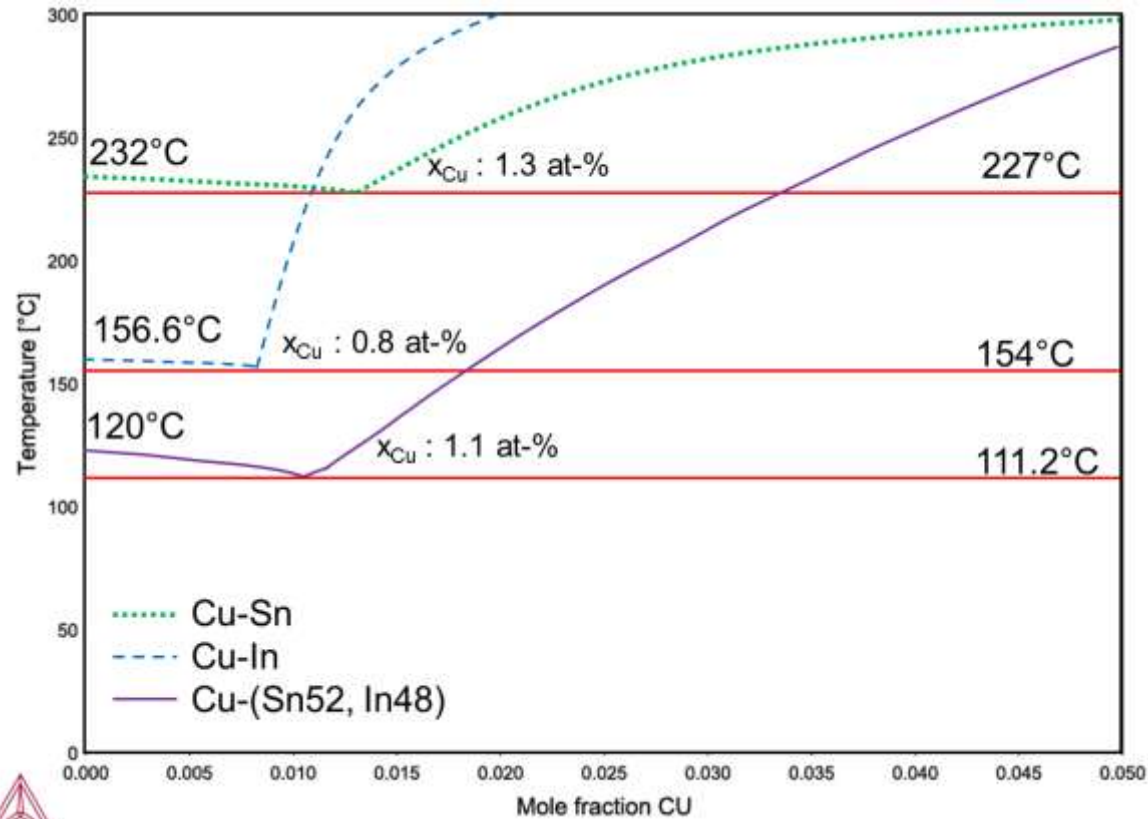


Cu-Sn-In LT-SLID bonding demonstrated at 150 °C

Ref: O. Golim *et al.*, *Scripta Materialia*, vol. 222, 114998, 2023

SLID metallurgy and contact metallizations

CuSnIn TLP System | Introduction

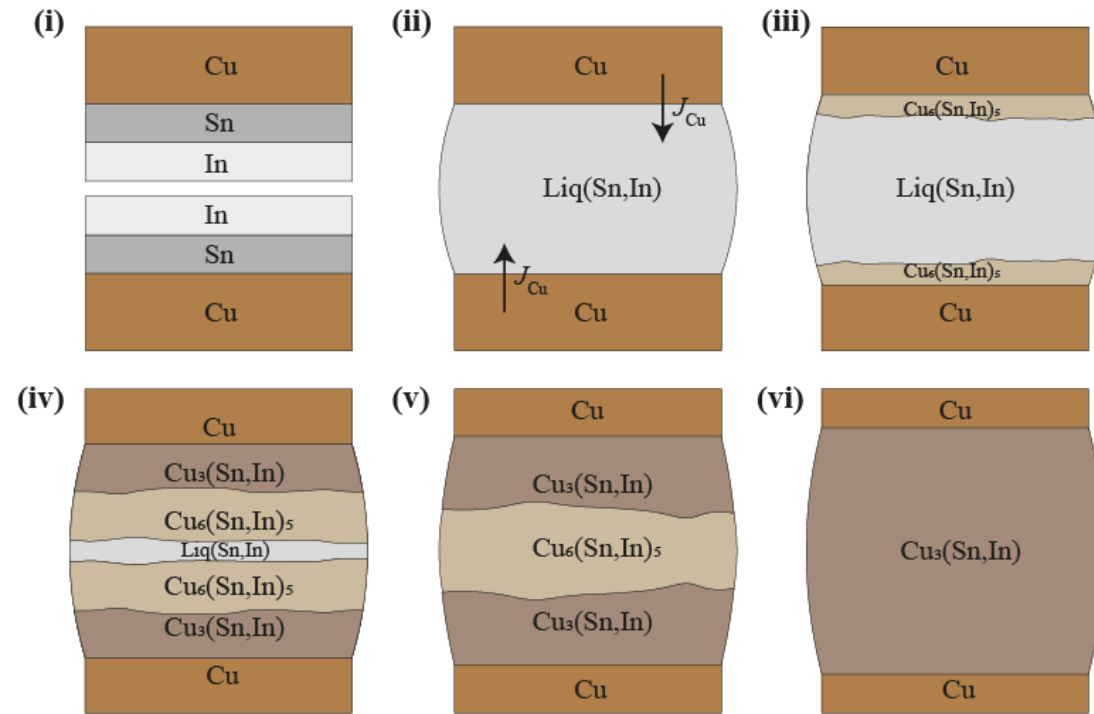
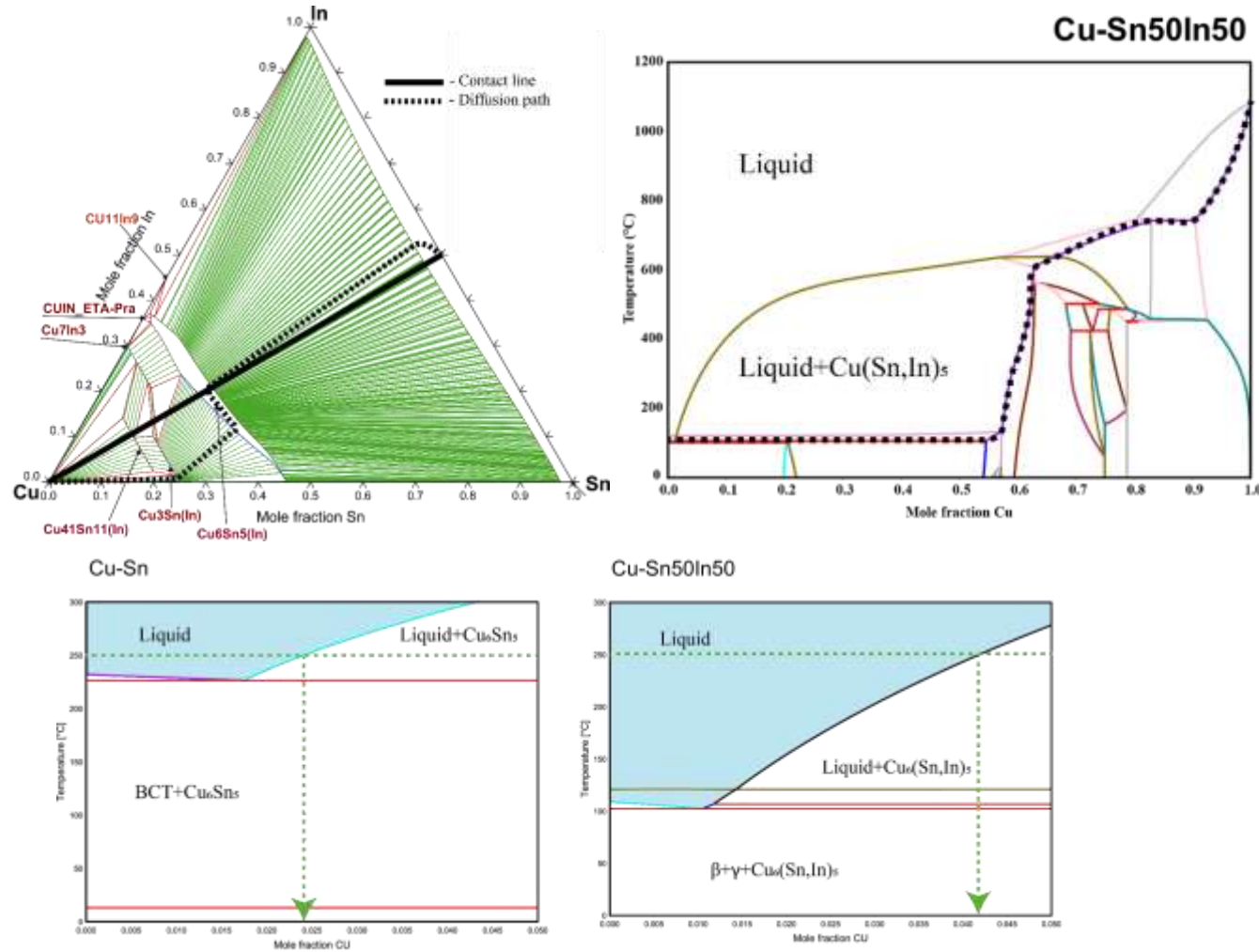


Liu, 2001

- Sn-In Eutectic behaviour reduces bonding temperature
- Addition of In stabilizes phase in $\eta\text{-Cu}_6(\text{Sn},\text{In})_5$, which has less voids on the interface
- Enlarges the process window by faster formation of IMC

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➤ Indium well known (alloying) element in low-temperature lead-free solders



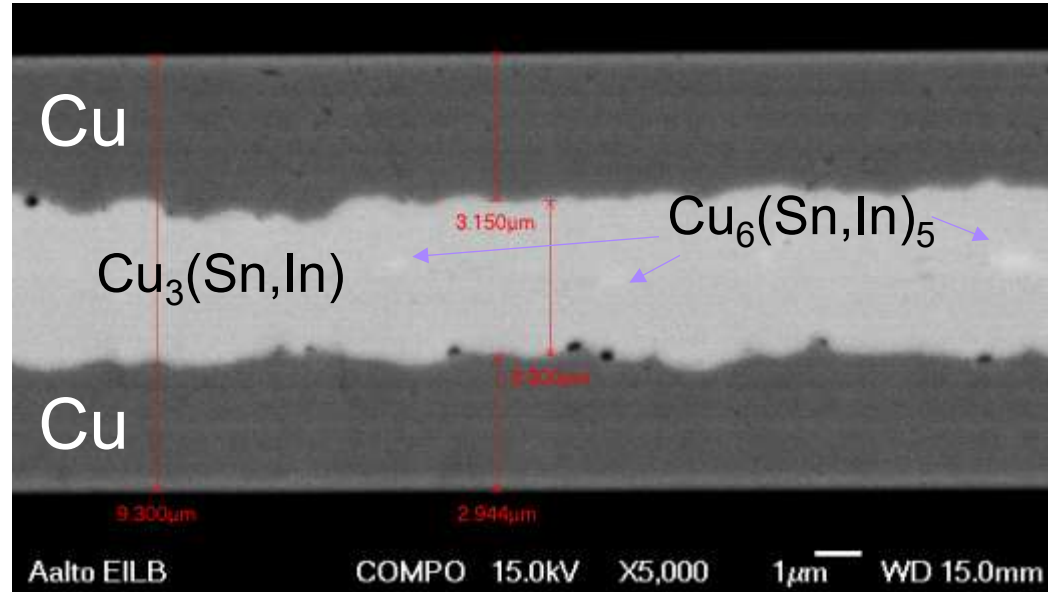
A!

Ref: TD assessment from: W. Gierlotka, Thermodynamic Description of the Quaternary Ag-Cu-In-Sn System, Journal of ELECTRONIC MATERIALS, Vol. 41, No. 1, 2012

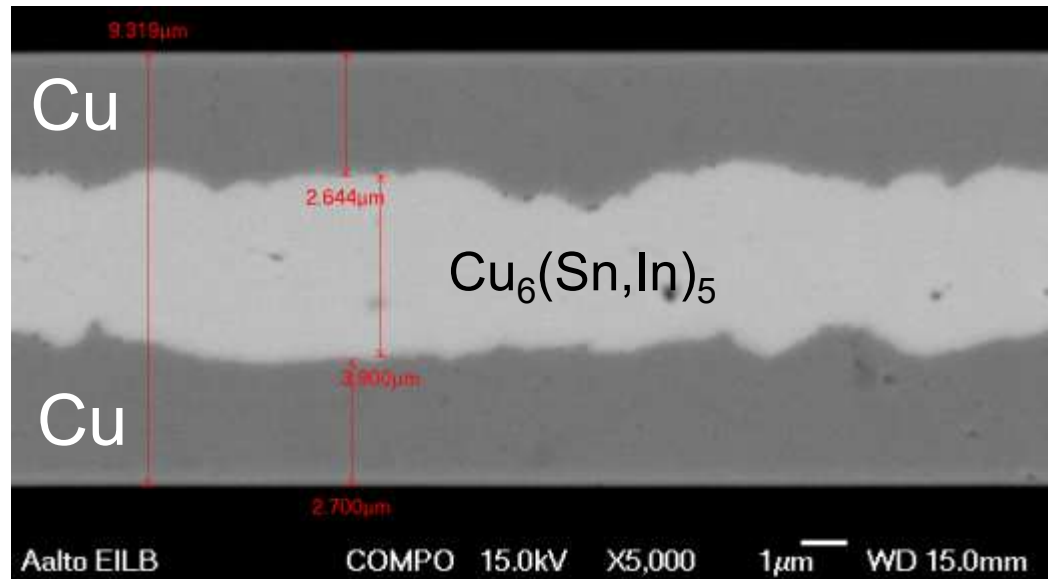
Results

As bonded (60min)

250°C

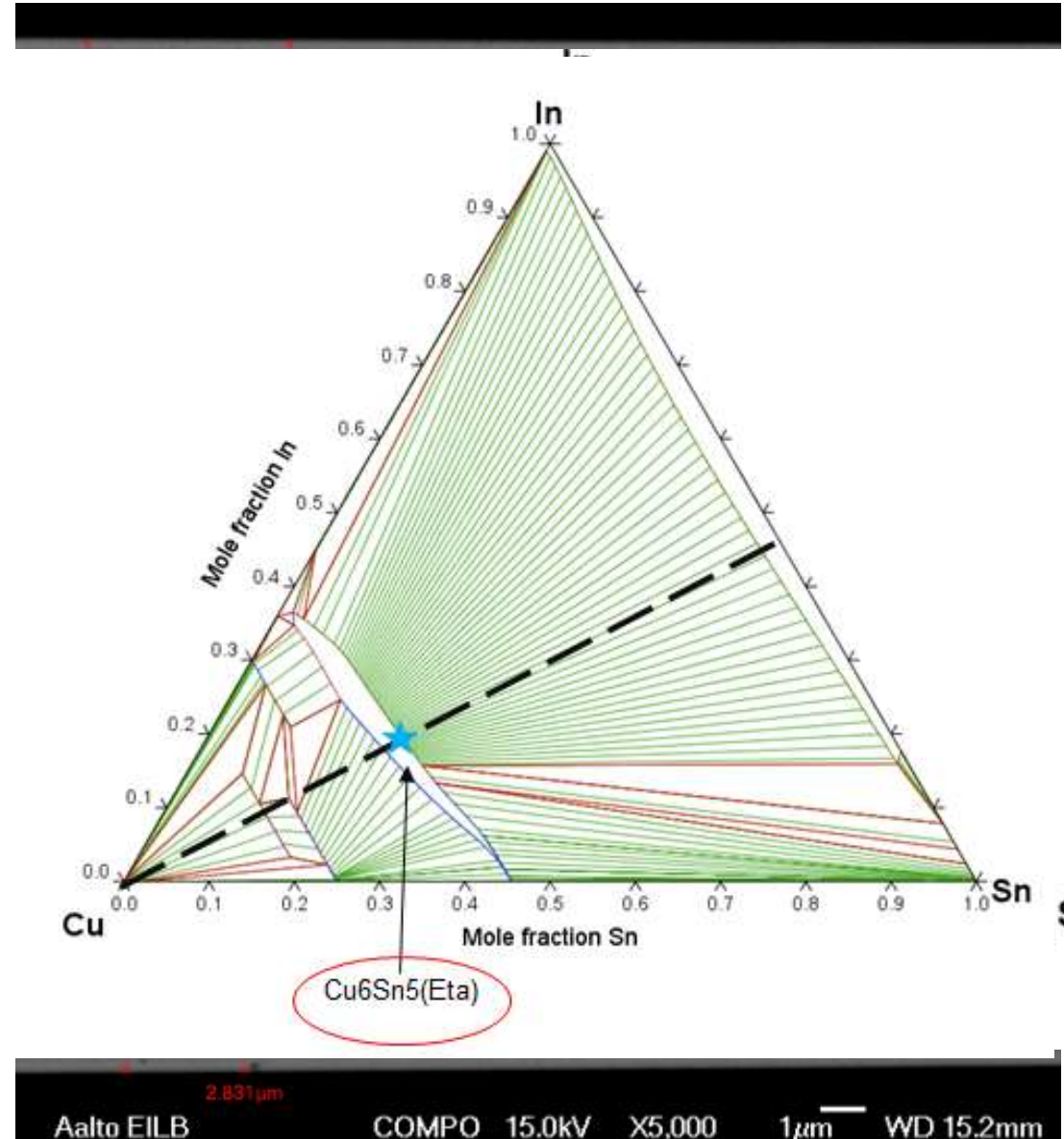


200°C

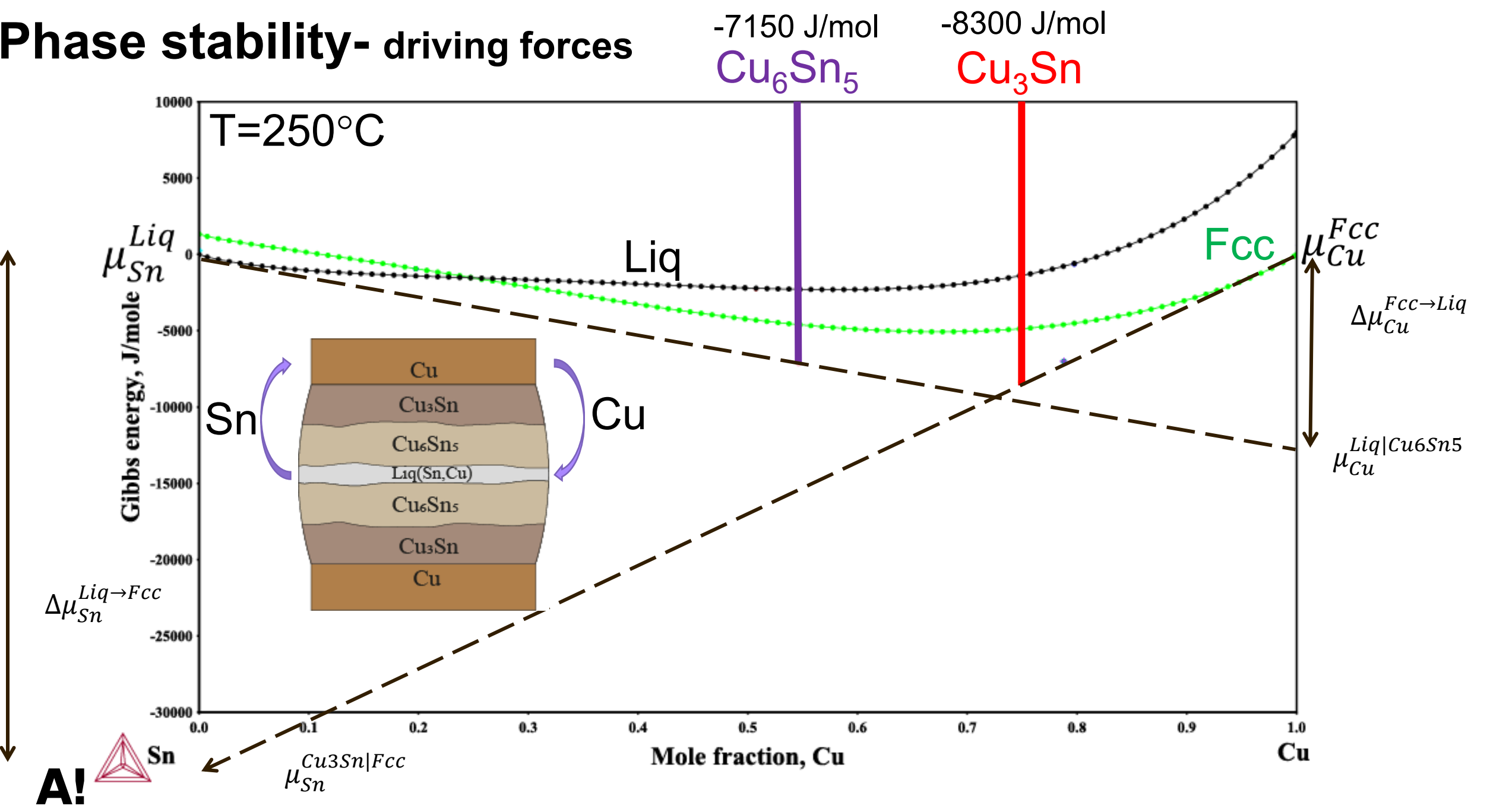


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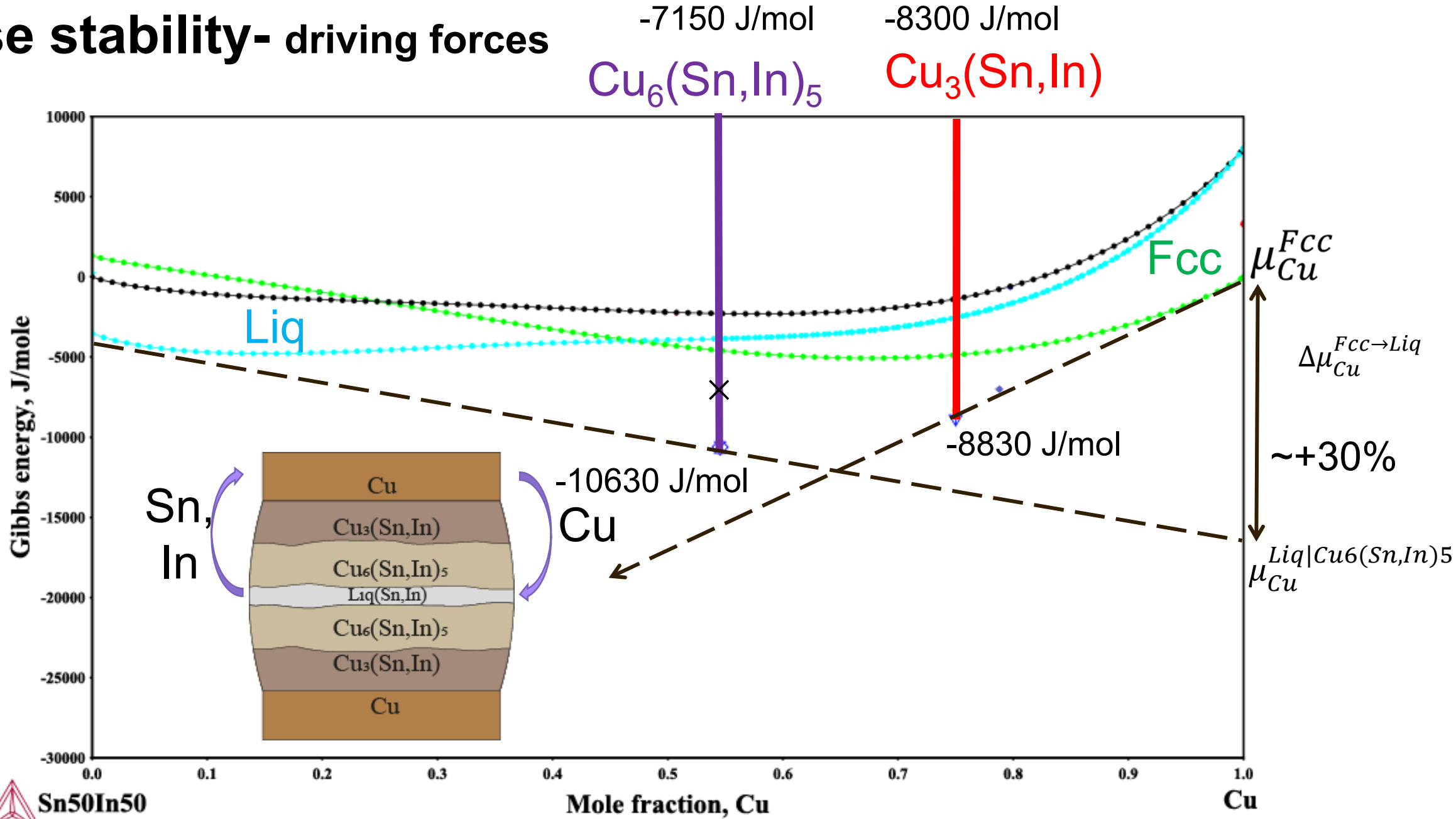
HTS 150°C for 21d (504h)



Phase stability- driving forces



Phase stability- driving forces



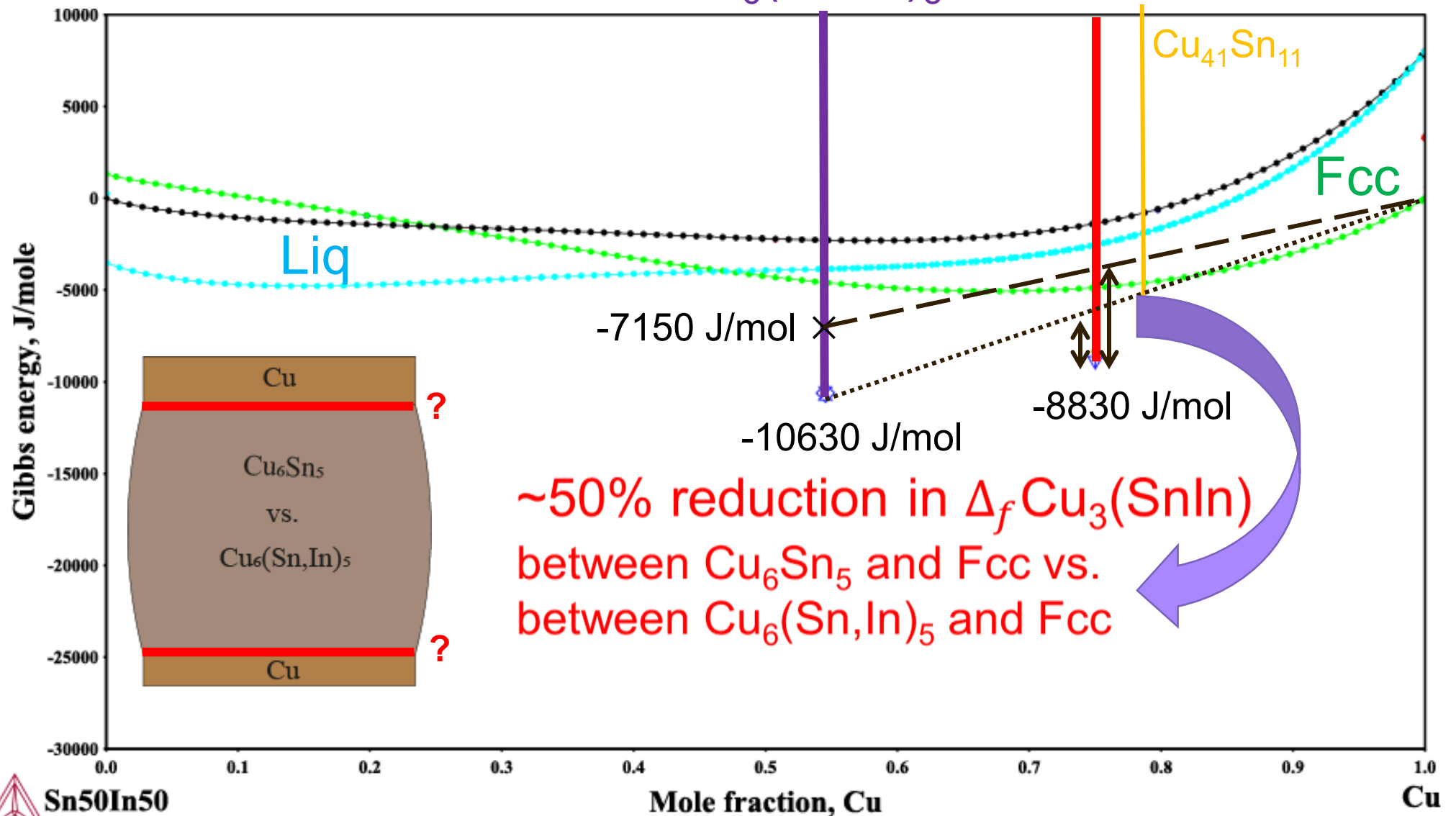
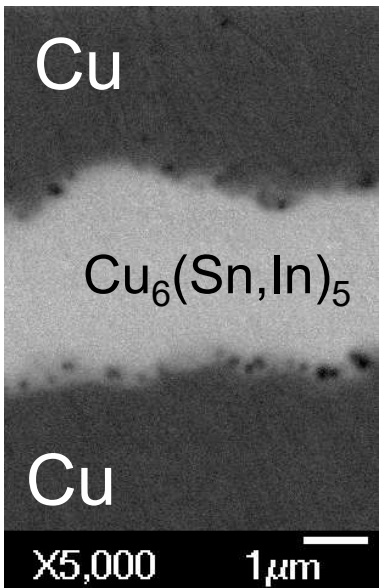
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Sn50In50

Mole fraction, Cu

Cu

Phase stability- Cu_3Sn

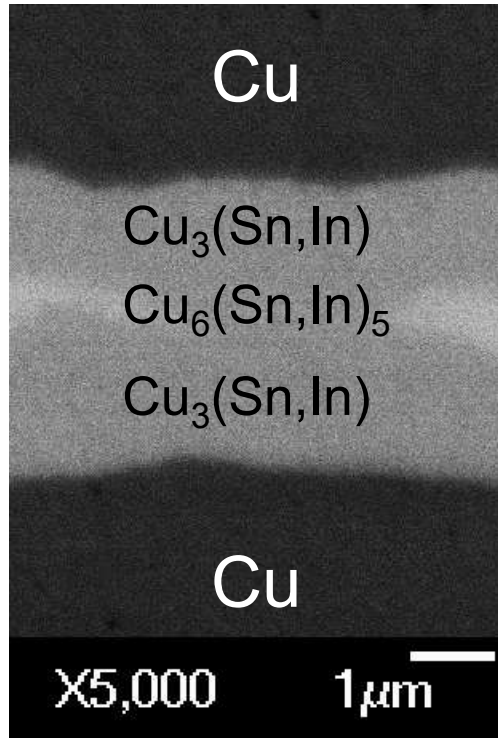


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Phase stability- $\text{Cu}_{41}\text{Sn}_{11}$

250°C (60min)+ 504h@150°C

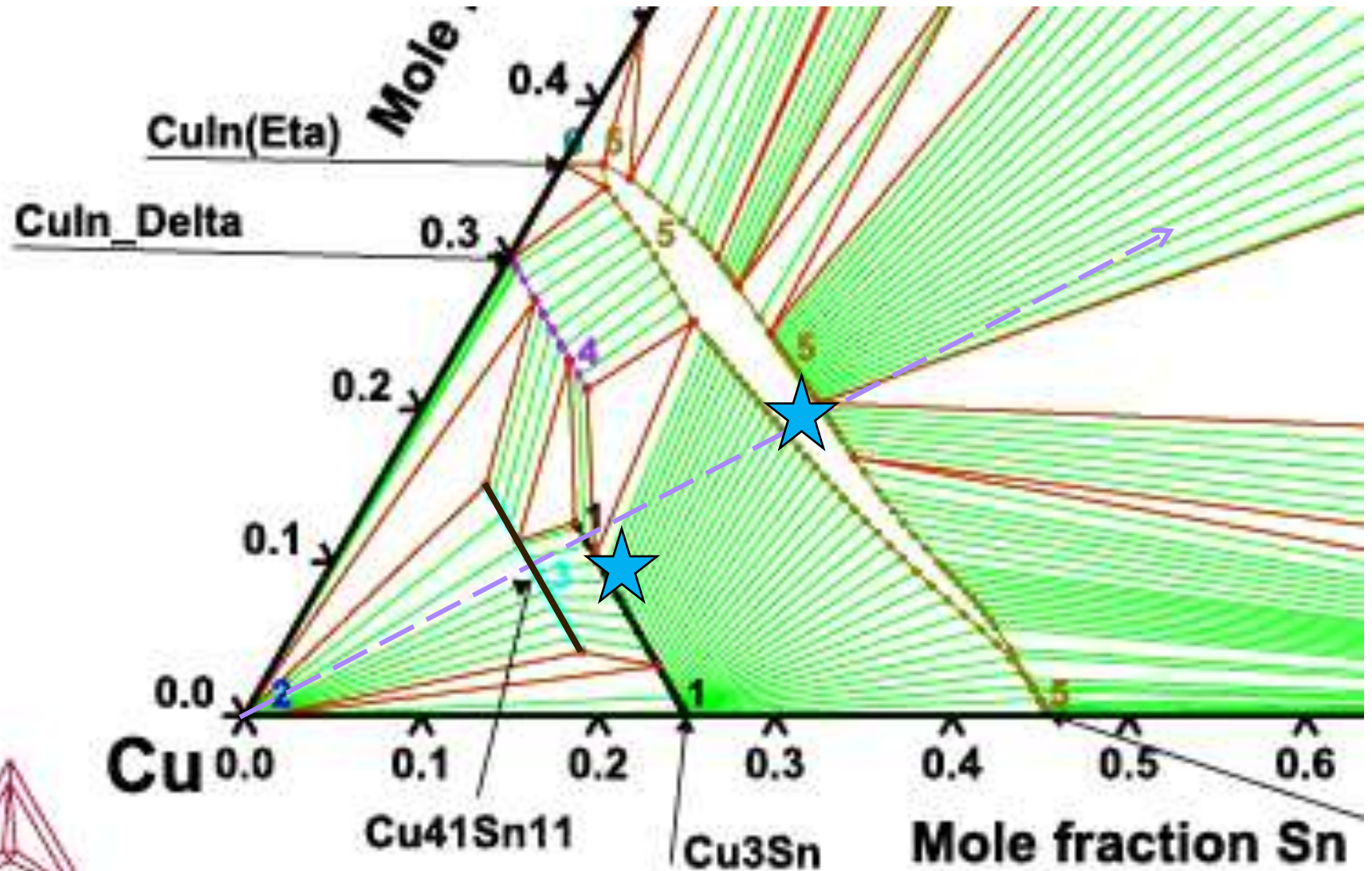


?

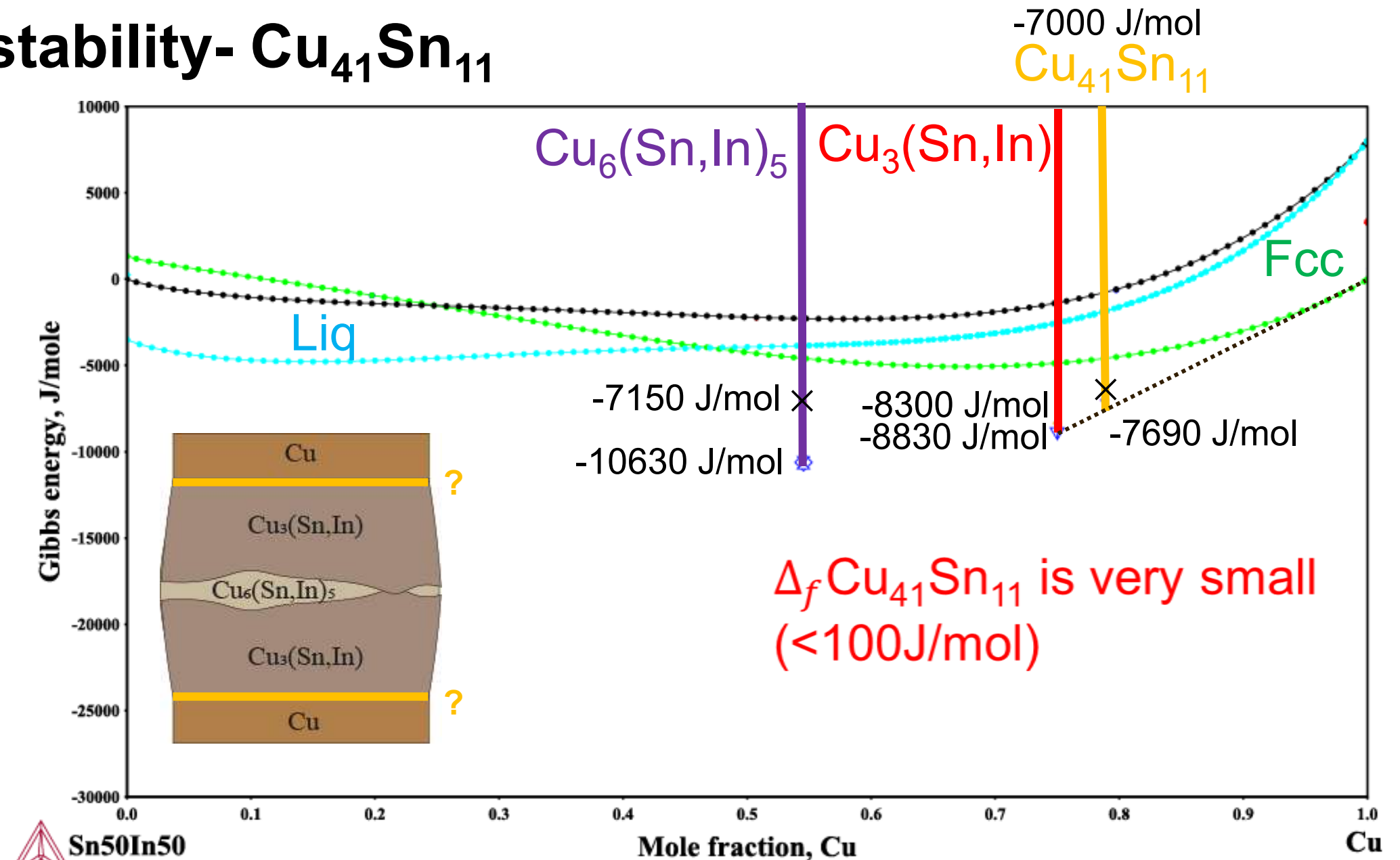
?

Cu 73.4 ± 0.5 at-%
Sn 14.8 ± 0.5 at-%
In 11.8 ± 0.5 at-%

A!



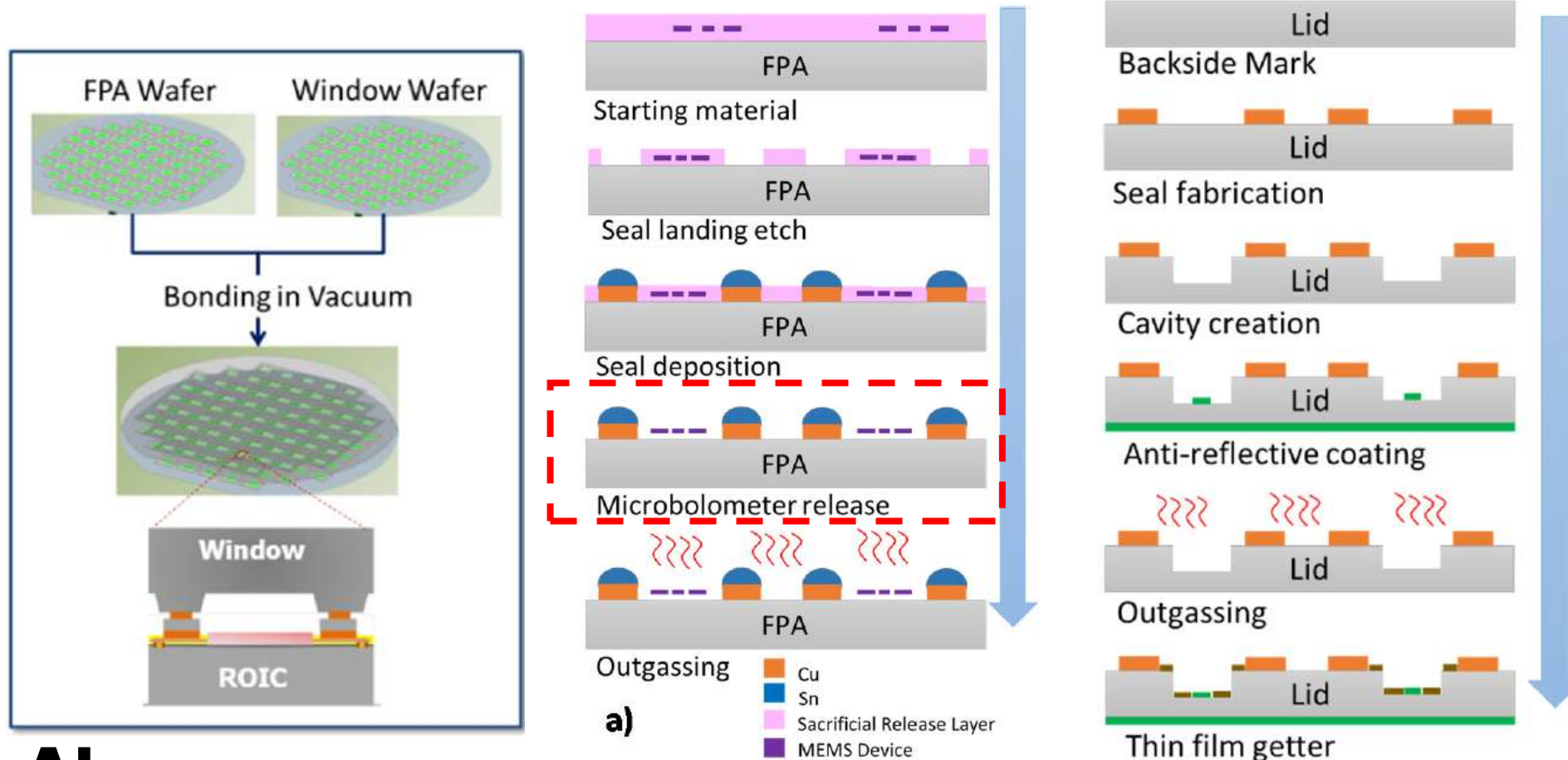
Phase stability- $\text{Cu}_{41}\text{Sn}_{11}$



A!

Process integration | flow example

REF: Allan Hilton et. al, Wafer-level Vacuum Packaging of Microbolometer-based Infrared Imagers

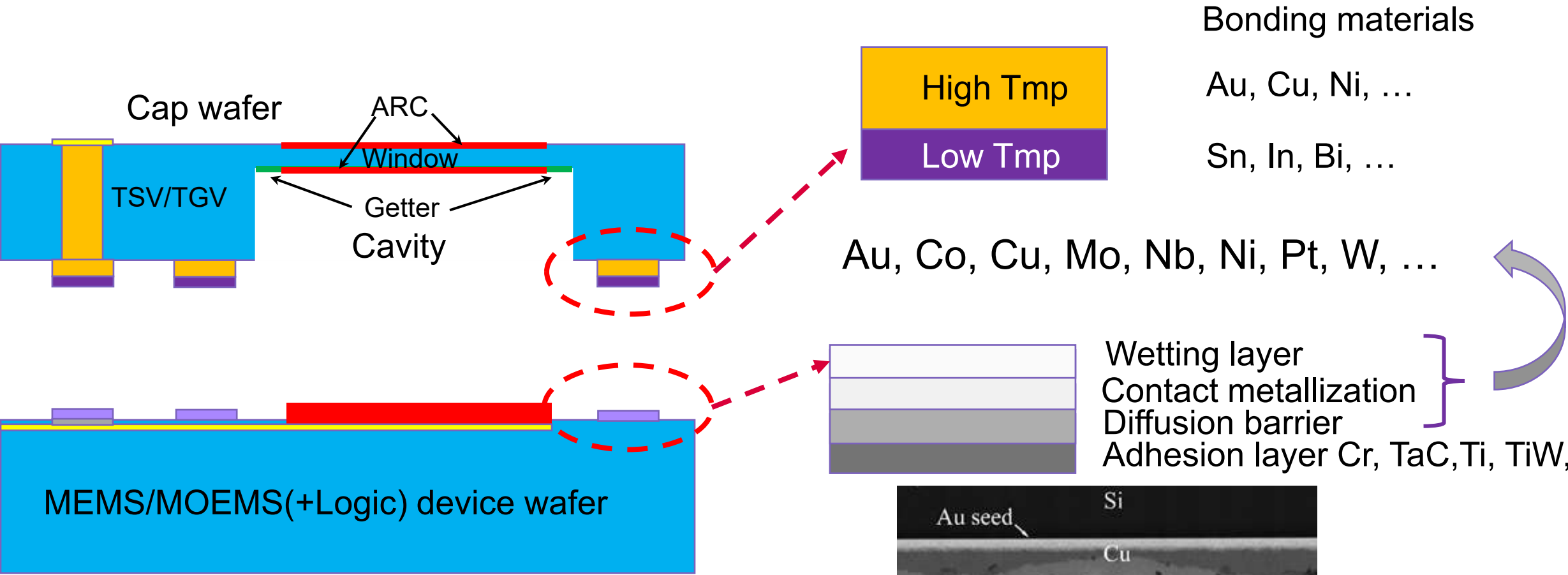


See also: A. Hilton, D. Temple, Wafer-Level Vacuum Packaging of Smart Sensors, in Sensors 2016 & F. Niklaus et.al, Low-Cost Uncooled Microbolometers for Thermal Imaging, in Proceedings of SPIE 2010

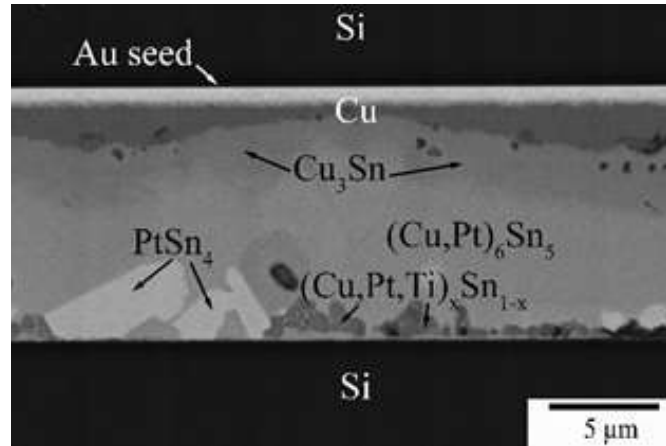
A!

FPA=Microbolometer focal plane array (MEMS+ROIC)

SLID Process integration solutions?



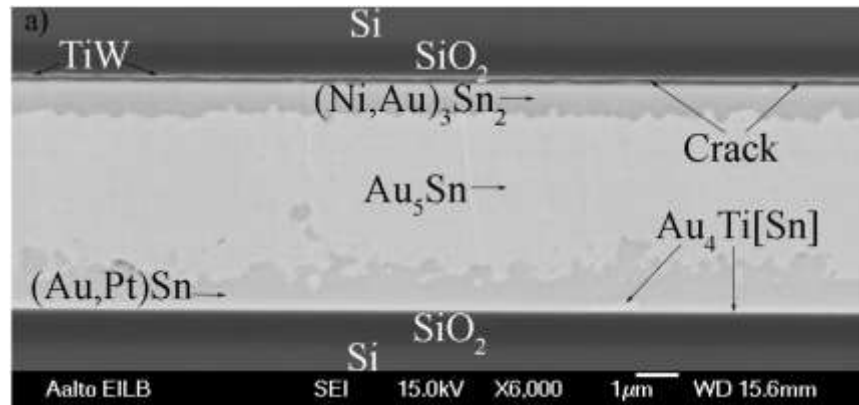
Avoiding “wet chemistry” from device wafer
A!



Design and manufacturing related issues in SLID bonding

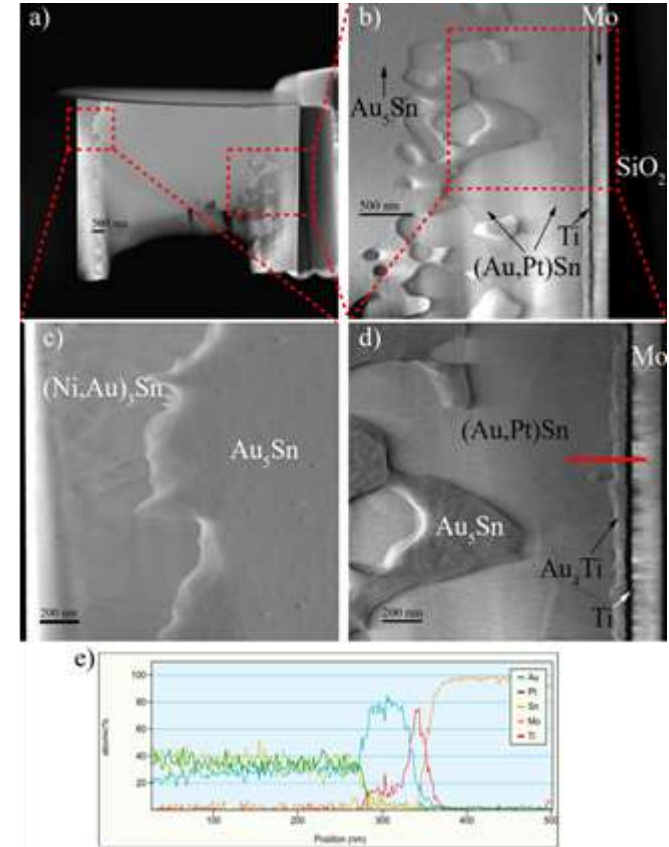
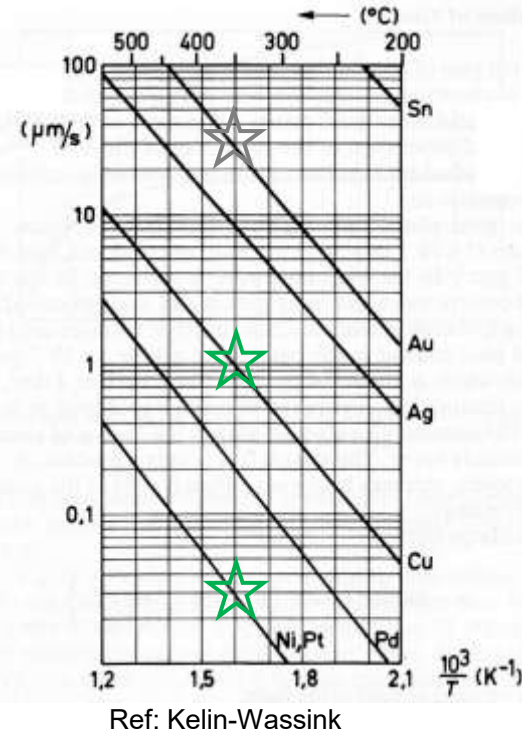
Metallizations for Au-Sn SLID metallurgy

- ✓ Consumption (dissolution) of the metallization during manufacturing processes
- ✓ Further reactions at HT usage
- ✓ "new" interfaces => mechanical reliability?



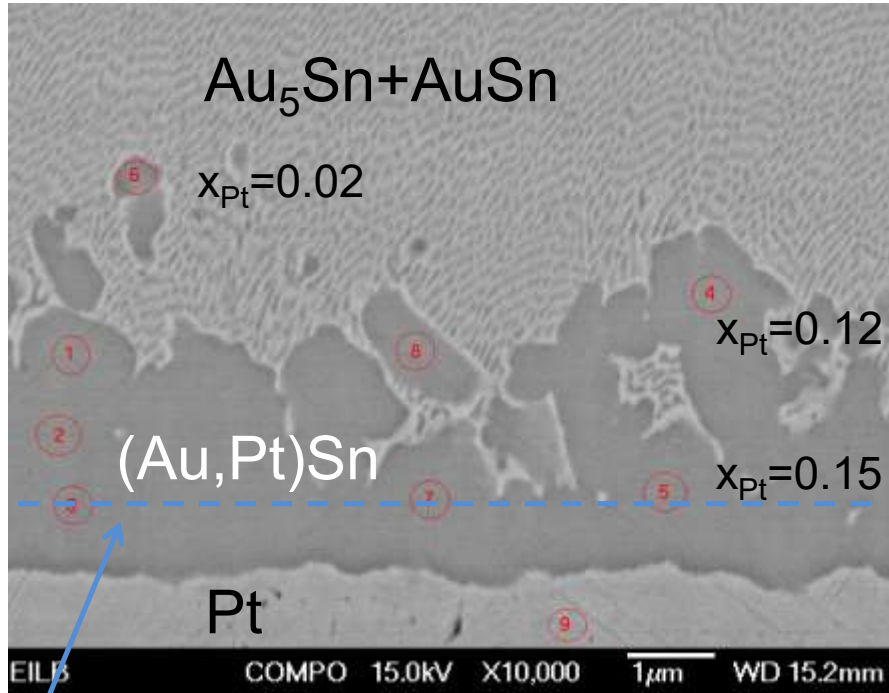
$$\Delta d \propto k \times^{\max} x_M^{Liq} \times t$$

$$k = k_0 e^{-Q/RT}$$



AuSn|Cu,Ni and Pt diffusion couples

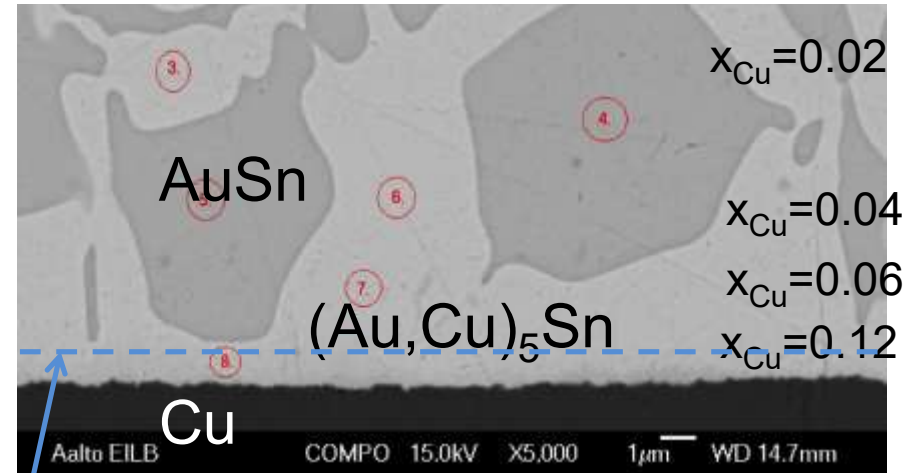
Bonding at 320 °C for 40 minutes



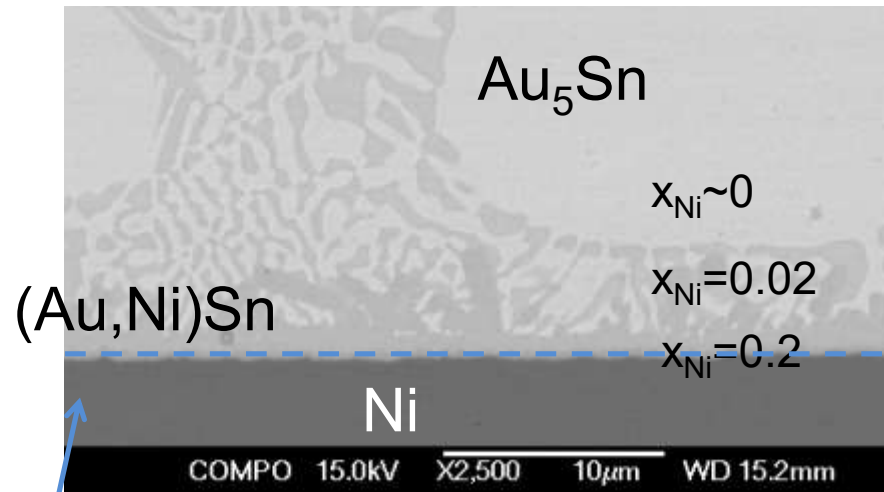
Original interface, $\Delta \sim 400-500nm$

The dissolution rate and consumption of the metallization during bonding is highest with Pt and lowest with Ni metallization

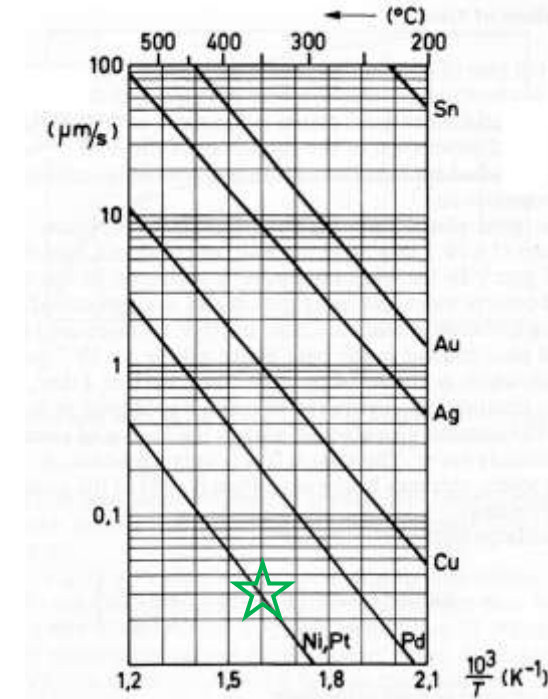
A!



Original interface, $\Delta \sim 200nm$



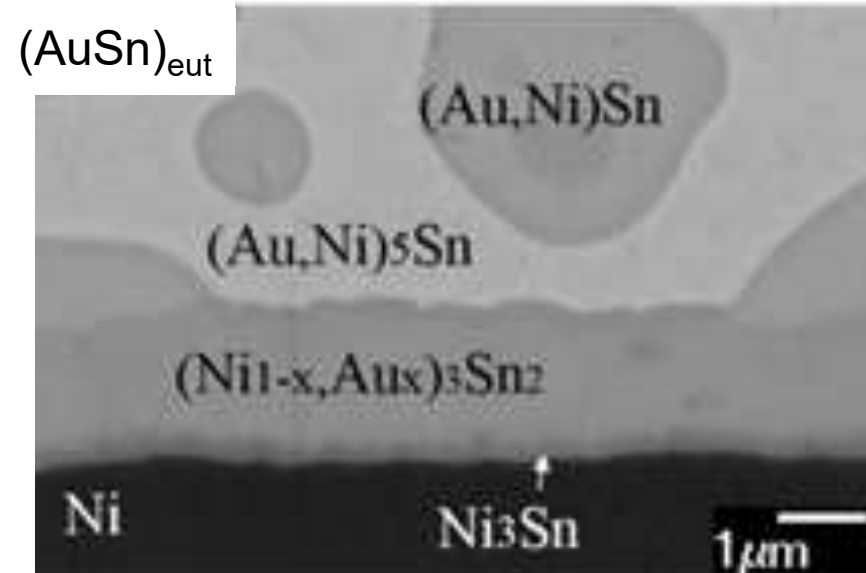
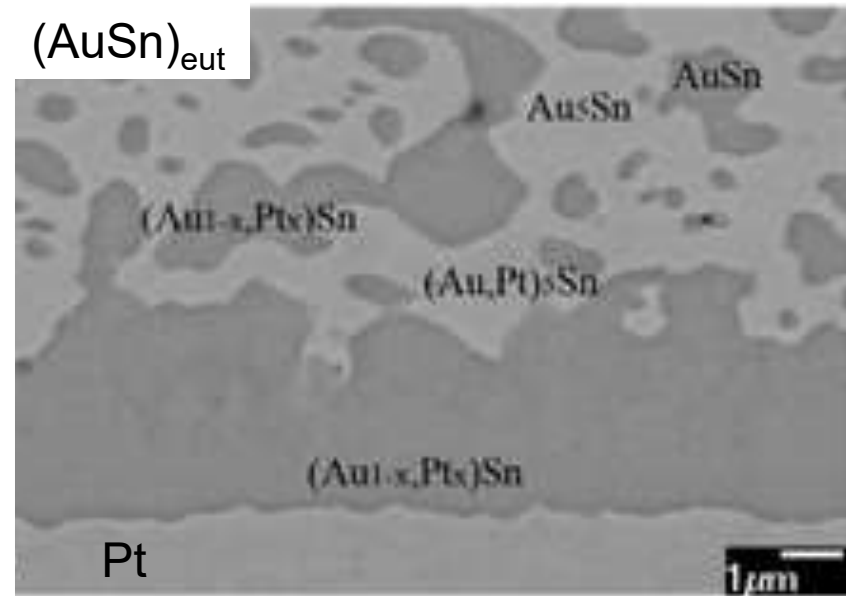
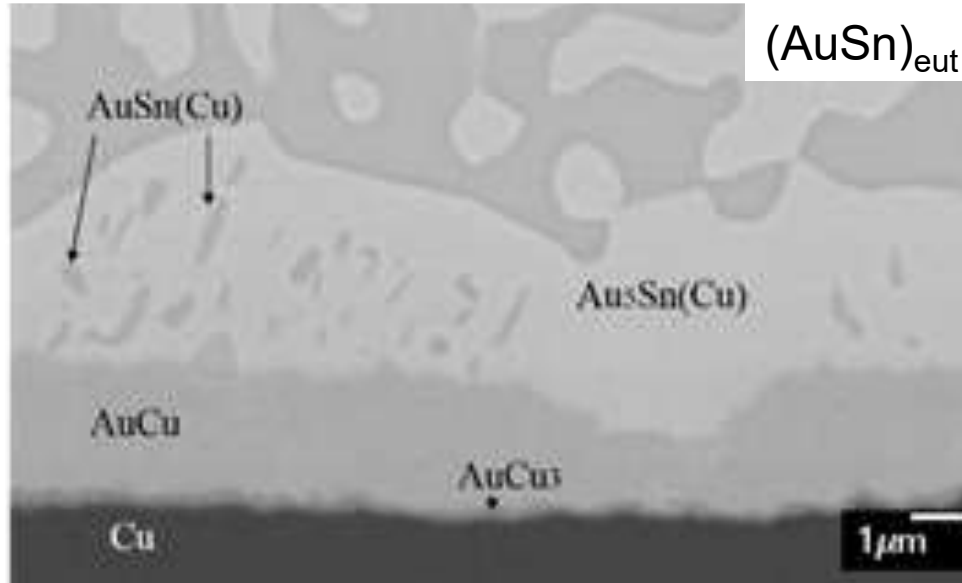
Original interface, $\Delta \sim 100nm$



Ref: Kellin-Wassink

AuSn|Cu,Ni and Pt diffusion couples

Aging at 150°C for 4600 hours

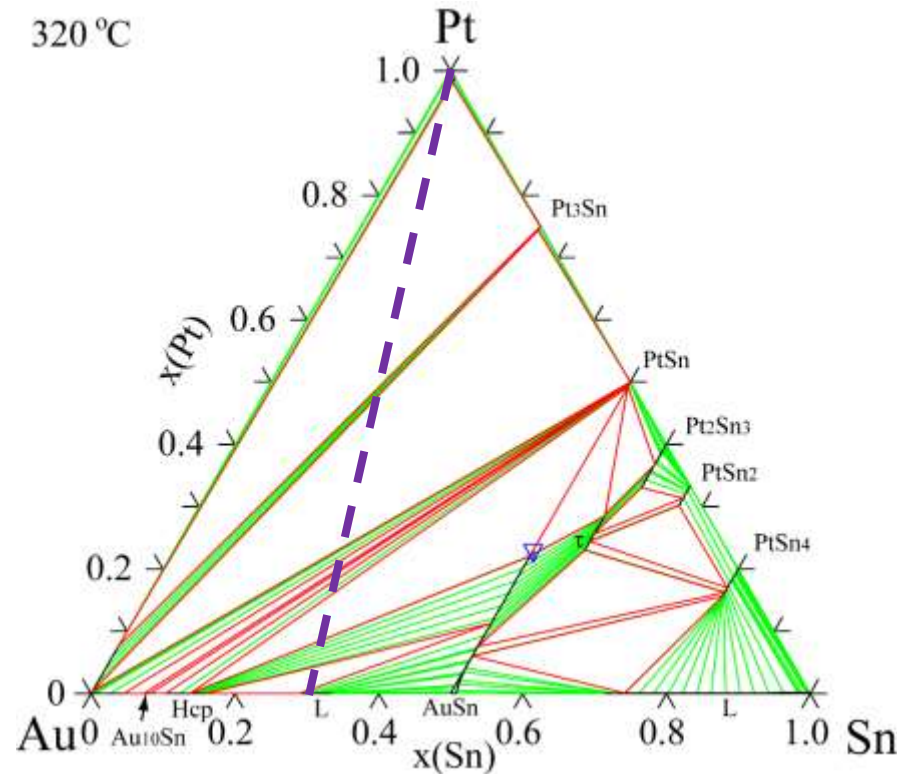


Pt is the most and Cu the least stable metallization under high temperature exposure

A!

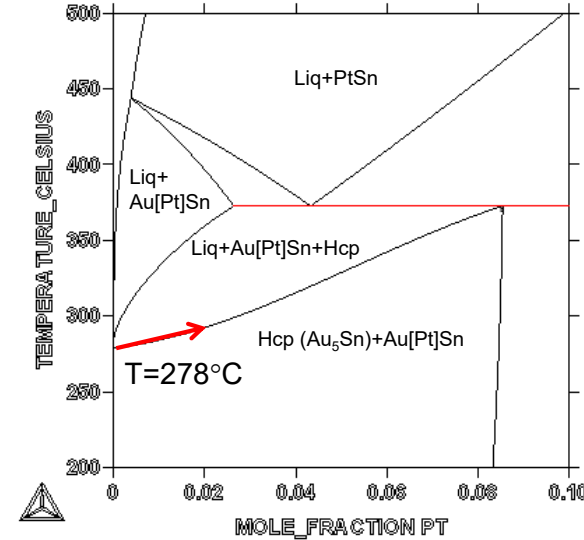
Effect of Pt on the remelting temperature of the bond

On the basis of the thermodynamic description of the Au-Pt-Sn system the effect of the Pt nominal content on the remelting temperature of the bond can be evaluated.



(AuSn)_{eut} or SLID

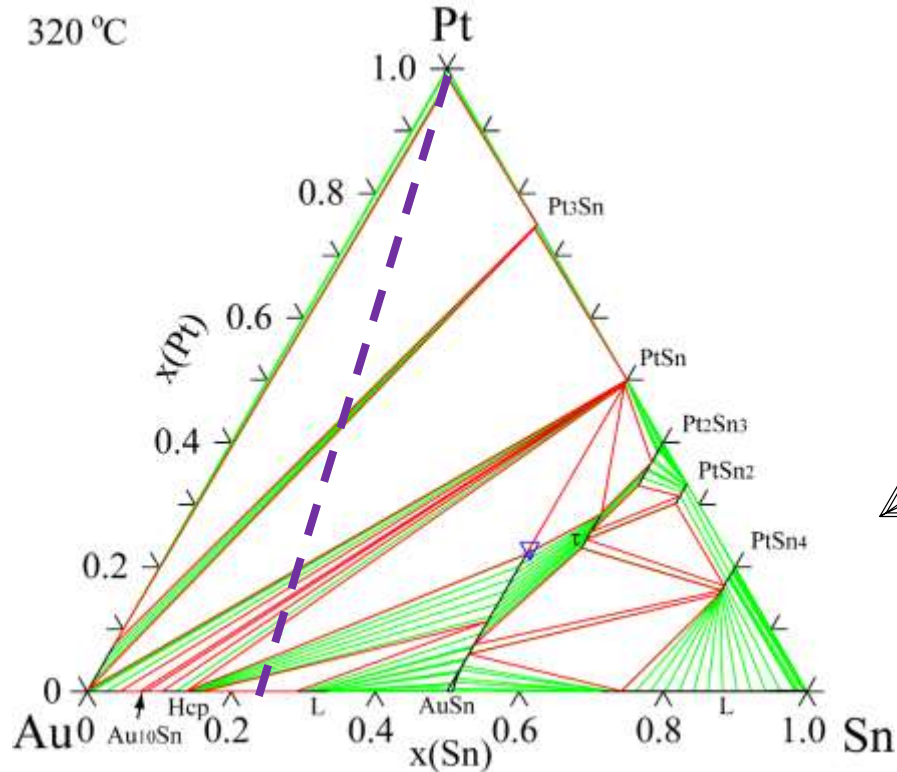
Pt (xμm)
Sn (2μm)
Au (3μm)



Pt thickness [μm]	X _{Pt}	
0,1	0,021	→ T _{mp} ~295°C
0,2	0,041	→ T _{mp} ~320°C
0,3	0,061	
0,4	0,079	
0,5	0,097	→ T _{mp} ~370°C
0,6	0,114	
0,7	0,131	
0,8	0,147	
0,9	0,162	
1	0,177	

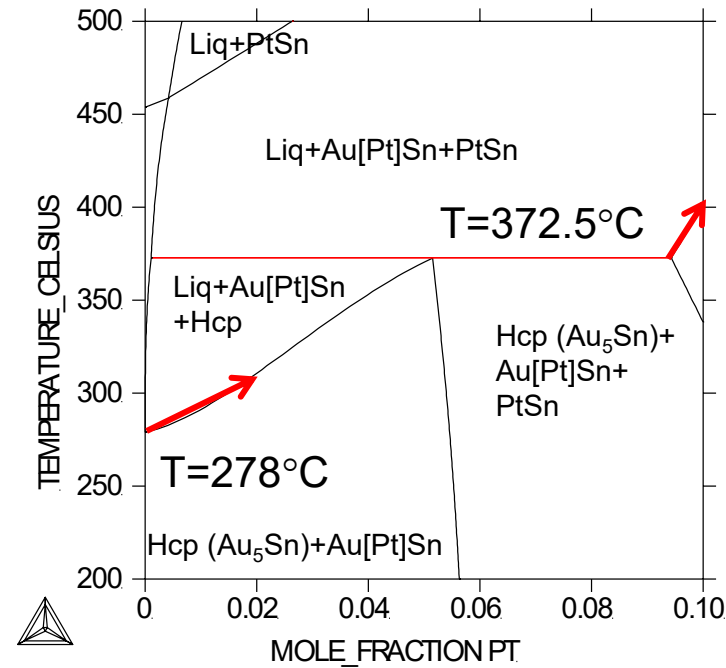
A!

Effect of Pt on the remelting temperature of the bond



(AuSn)_{eut} or SLID

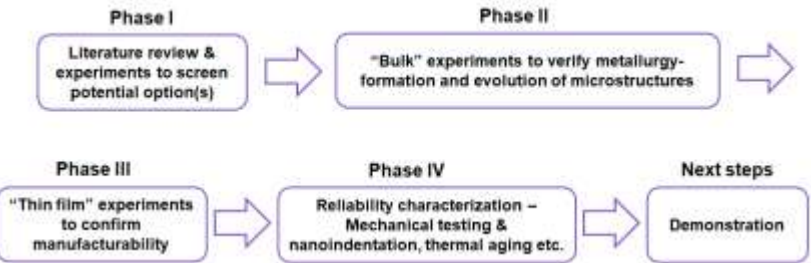
Pt (xμm)
Sn (2μm)
Au (4μm)



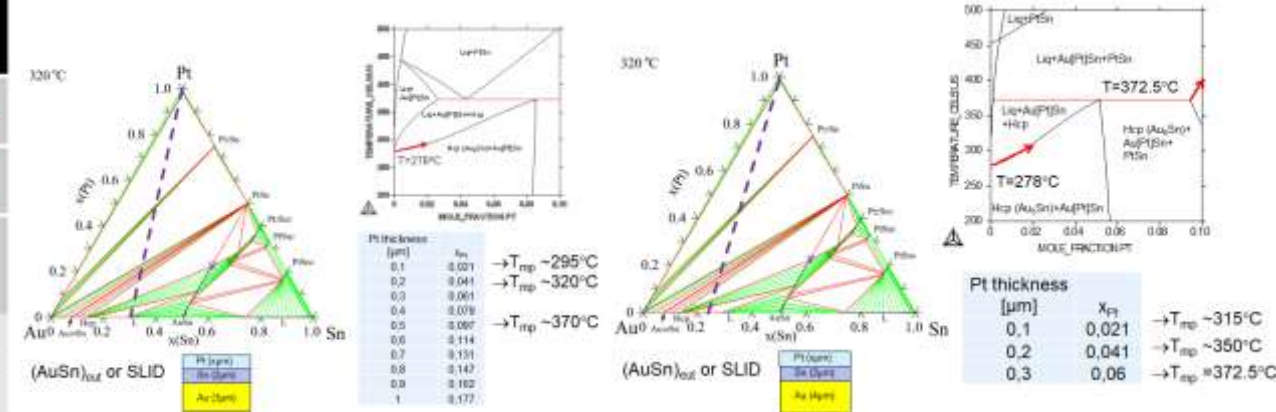
Pt thickness [μm]	x_{Pt}	
0,1	0,021	→ $T_{mp} \sim 315^{\circ}C$
0,2	0,041	→ $T_{mp} \sim 350^{\circ}C$
0,3	0,06	→ $T_{mp} = 372.5^{\circ}C$

A!

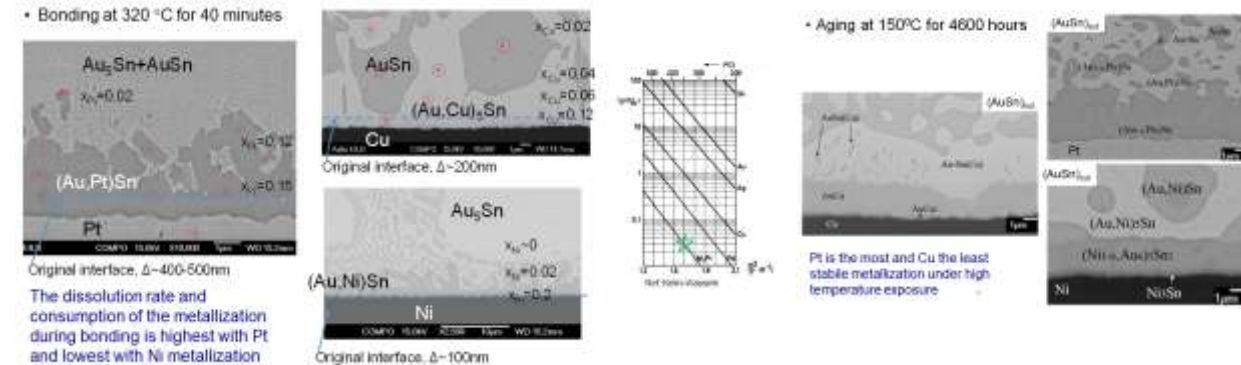
Solutions for contact metallization



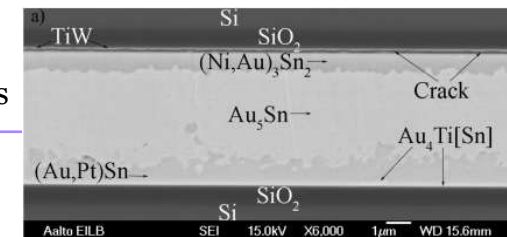
	Solubility Dissolution rate	wettability	Intermetallic components	Problems
Gold(Au)	High	Excellent	AuSn4 (Cu,Au)6Sn5	Wet chemistry, cost, etching
Copper(Cu)	Moderate	good	Cu6Sn5 Cu3Sn	Wet chemistry, storage life
Nickel(Ni)	Low solubility	adequate	(Ni, Cu)3Sn4 (Cu, Ni)6Sn5 (Cu, Ni)3Sn	stable oxide/ hydroxide Worsening wetting
Platinum(Pt)	a dissolution rate less than half that of Ni	good	PtSn4 (Cu, Pt)6Sn5	challenging etching process



	Solubility	Wettability	Intermetallic components	Phase diagram with In or Sn
Molybdenum(Mo)	Negligible	Mo is effectively wetted by tin at 950 °C	Mo-Sn system can form intermetallic compounds	available
Tungsten(W)	The solubility of W in molten Sn is ≈10 ⁻³ at. %. The solubility of W in molten In is ≈ 10 ⁻⁶ at. %.	W is wetted well at 1050 °C	No interaction in solid and liquid states at temp <1680 °C	No diagram plot
Cobalt(Co)	Low solubility	Acceptable wettability for electronic application Contact angle below 32	Cosn3 (Cu, Co)6 Sn5	available
Niobium (Nb)	low (at temperature of 1400 °C about 3% of niobium is present as a solution in tin)	No data	NbSn2, Nb6Sn5, and Nb3Sn	Available
Vanadium (V)			Sn2V and SnV3	Available

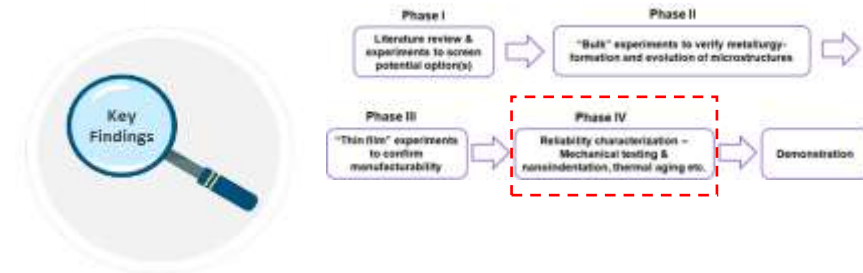
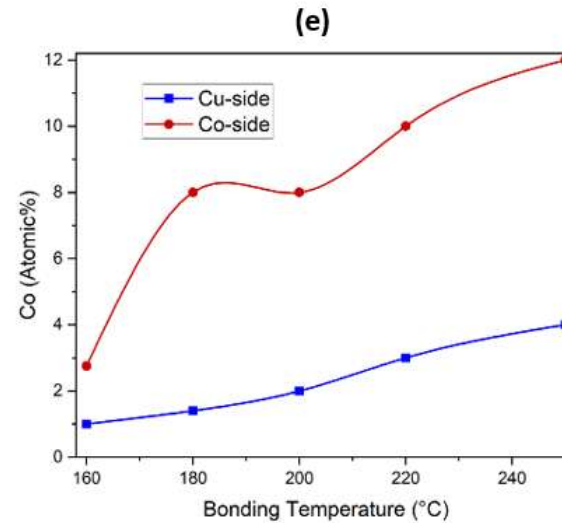
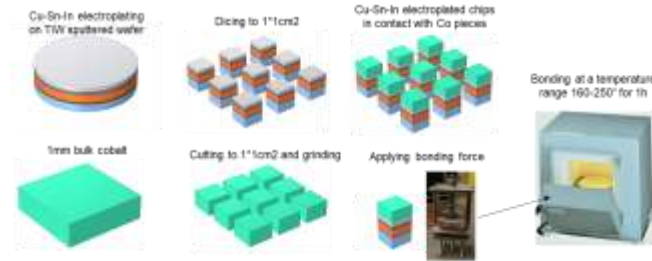
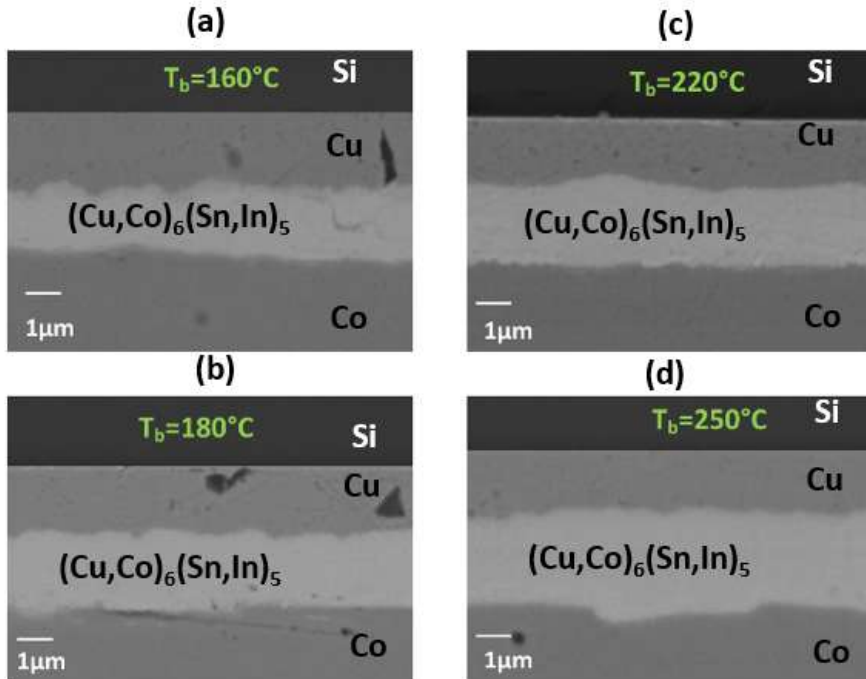


- ✓ Consumption (dissolution) of the metallization during manufacturing processes
- ✓ Further reactions at HT usage
- ✓ "new" interfaces => mechanical reliability?



Co contact metallization for Cu-In-Sn LTSLID

❖ Microstructure



A fully IMCs joint can be obtained at a temperature range of 160-250°C for 1h

Bond line is composed of a single phase $(\text{Cu,Co})_6(\text{Sn,In})_5$

With increasing the bonding temperature, the Co content in the $\text{Cu}_6(\text{Sn,In})_5$ increases

Combination of Co and In shows stronger impact on the inhibition of the Cu_3Sn phase formation

There is no detectable voids in the bondline

Cross sectional BSE-SEM images of Cu-Sn-In/Co joints formed at, (a) 160 ° C, (b) 180 ° C, (c) 220 ° C, and (d) 250 ° C for 1h, and (e) the average atomic percent of cobalt dissolved into $(\text{Cu,Co})_6(\text{Sn,In})_5$ phase (formed in the Cu- and Co-sides) as a function of bonding temperature.

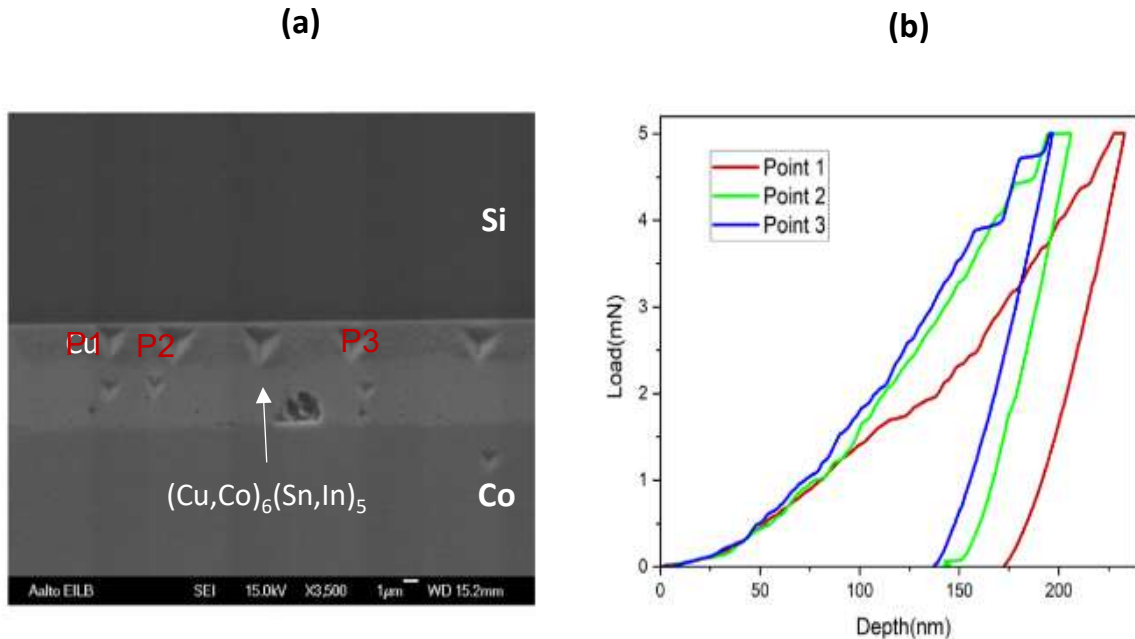
Ref: F. Emadi*, V. Vuorinen, and M. Paulasto-Kröckel; Utilizing Co as a contact metallization for wafer-level Cu-Sn-In SLID bonding used in MEMS and MOEMS packaging, ESTC 2022

A!

Co contact metallization for Cu-In-Sn LTSLID

❖ Mechanical properties

Nanoindentation Analysis



(a) BSE-SEM image of indents on Cu-Sn-In/ Co joint bonded at 200 C for 1h, and (b) the indentation load displacement curves of three different points in the bond area.

	Point1	Point2	Point3	Cu ₆ Sn ₅
H (GPa)	4.6	5.9	6.6	6.7±0.5
Er (Gpa)	95.5	113.1	112.0	103.7±0.4
Ei (GPa)	104.2	125.5	124.1	114.1±1
Ei/H	22.6	21.3	18.8	17
Cu (at%)	49.1	57.6	48.9	55.3
Co (at%)	2.1	2.9	6.2	0
Sn (at%)	21.0	13.9	23.8	44.7
In (at%)	27.8	25.6	21.1	0



Ei/H values: (Cu,Co)₆(Sn,In)₅ > Cu₆Sn₅

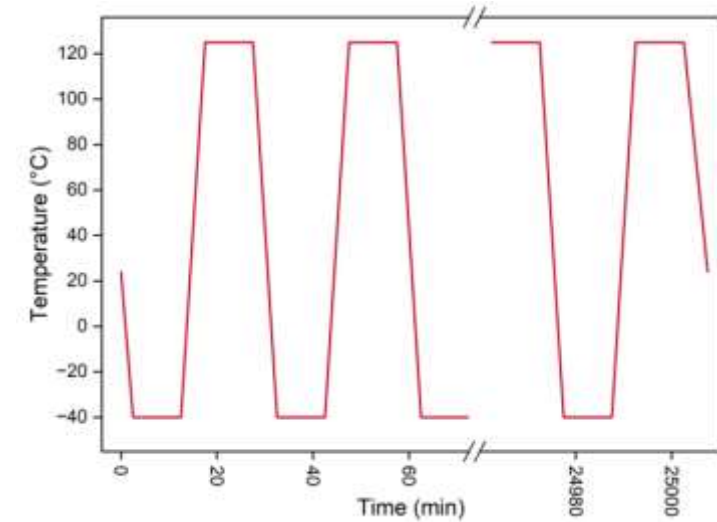
Plasticity: (Cu,Co)₆(Sn,In)₅ > Cu₆Sn₅

Ref: F. Emadi*, V. Vuorinen, and M. Paulasto-Kröckel;
Utilizing Co as a contact metallization for wafer-level
Cu-Sn-In SLID bonding used in MEMS and MOEMS
packaging, ESTC 2022

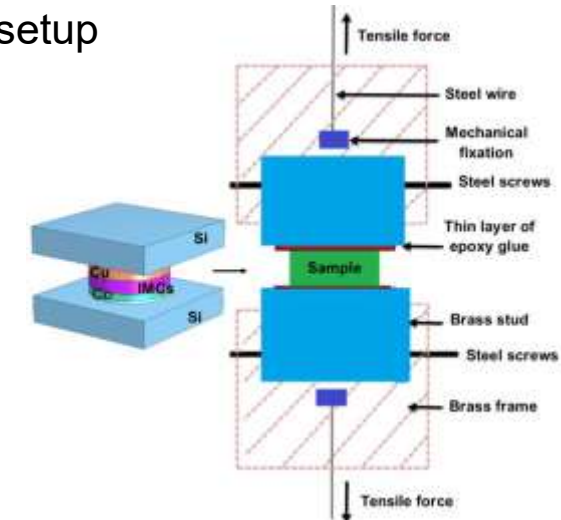
A!

Cu-In-Sn LTSLID reliability

Temperature profile for the thermal shock test



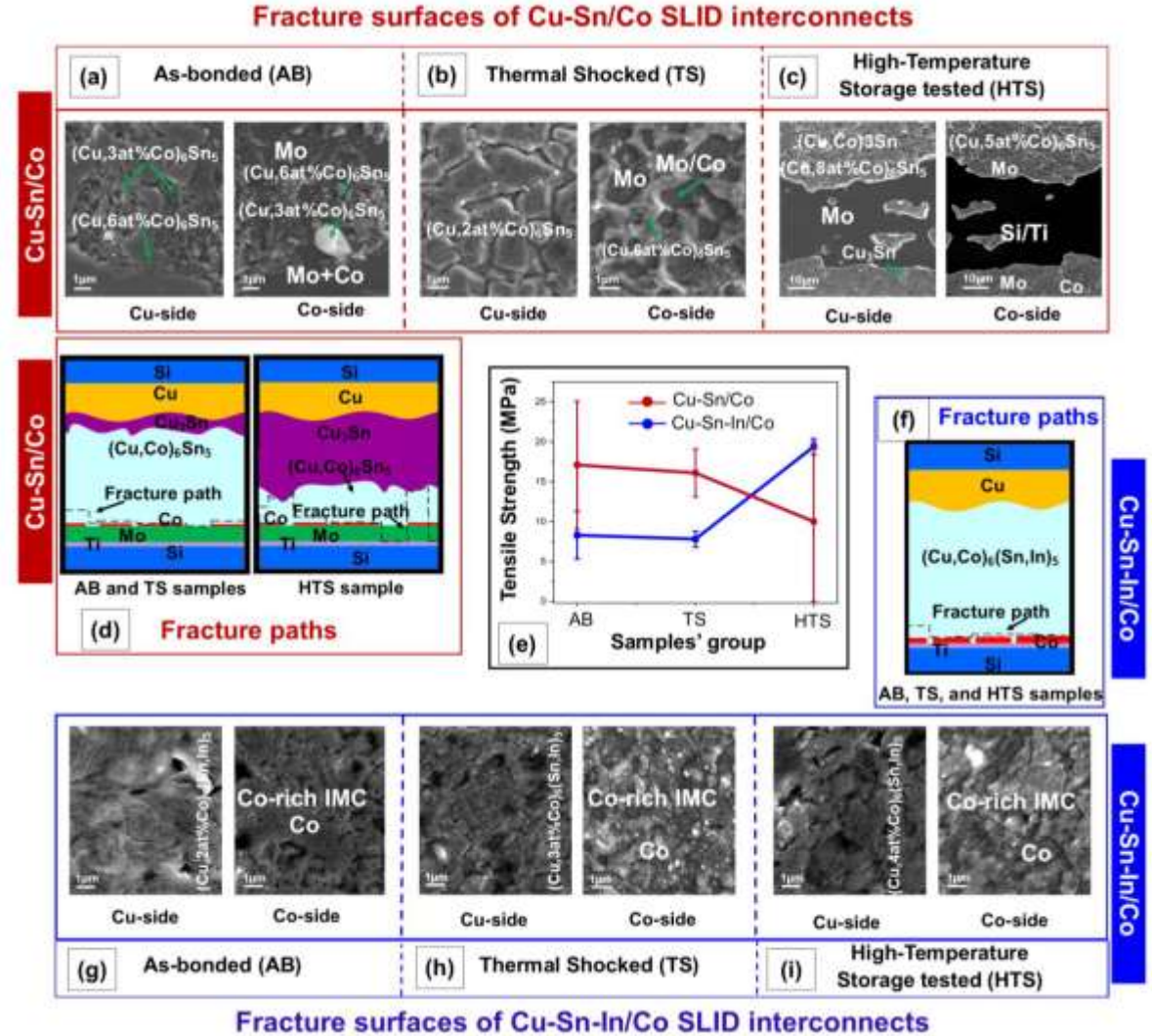
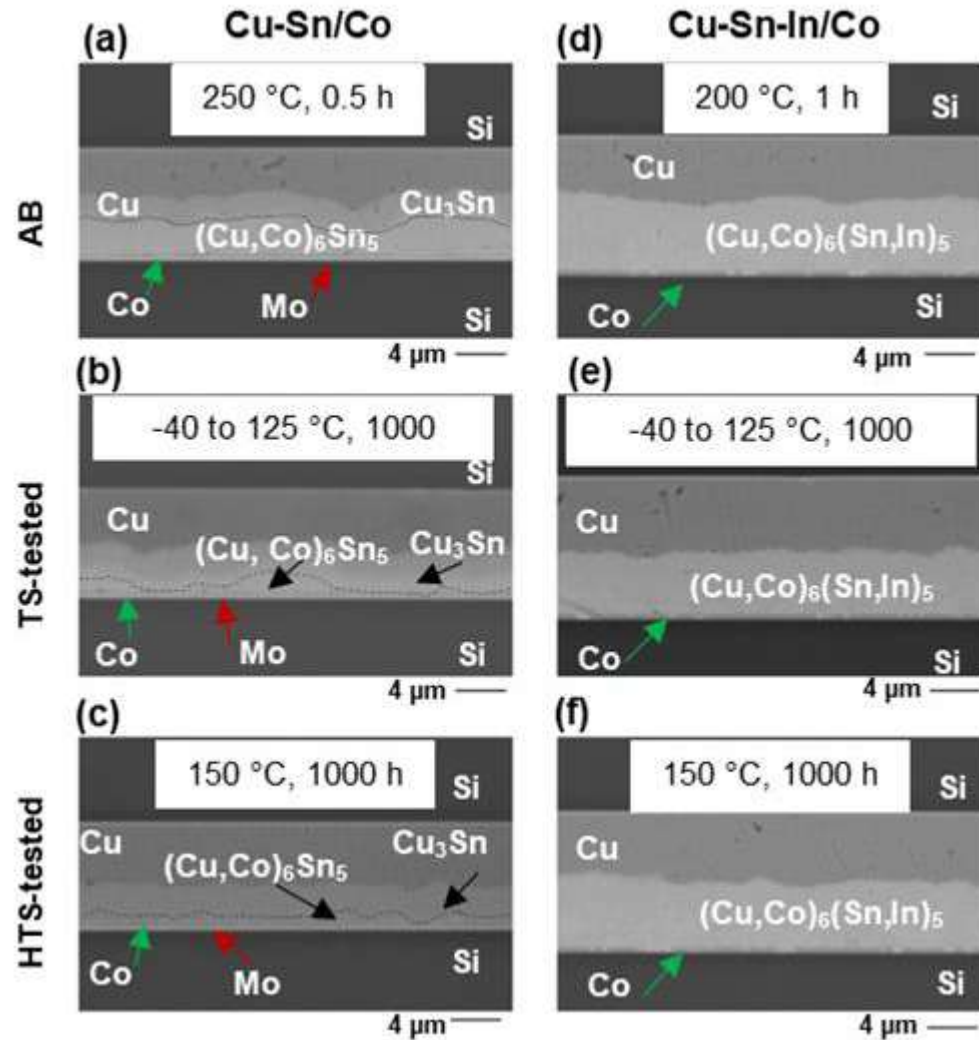
Tensile test setup



A!

Ref: F. Emadi, V. Vuorinen, S. Liu and M. Paulasto-Kröckel, "Novel low-temperature interconnects for 2.5/3D MEMS integration: demonstration and reliability," in IEEE Transactions on Components, Packaging and Manufacturing Technology, 2024.

Cu-In-Sn LTS/LID reliability

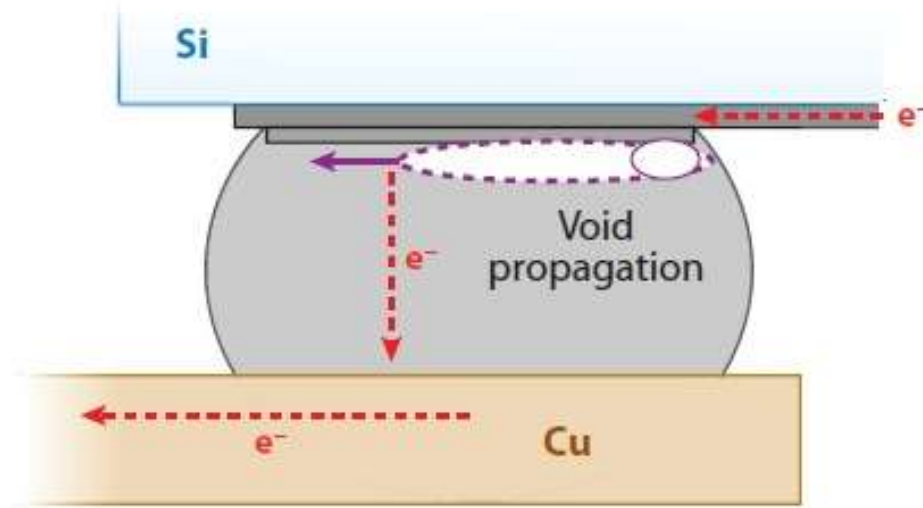


A!

Ref: F. Emadi, V. Vuorinen, S. Liu and M. Paulasto-Kröckel, "Novel low-temperature interconnects for 2.5/3D MEMS integration: demonstration and reliability," in IEEE Transactions on Components, Packaging and Manufacturing Technology, 2024.

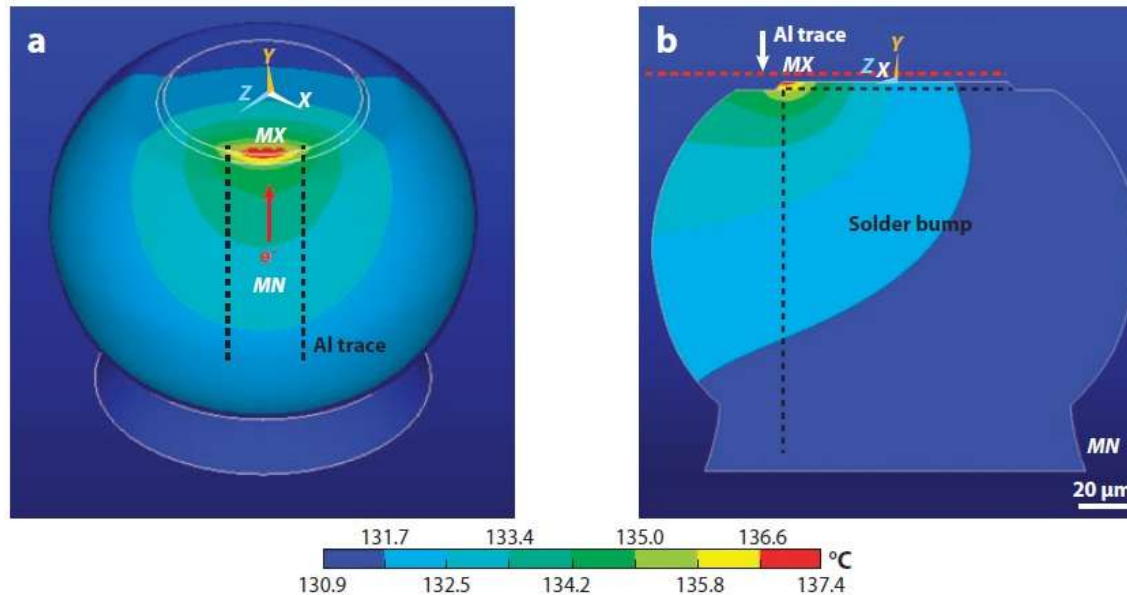
SLID electrical performance – Electromigration

Electromigration



Reasons:

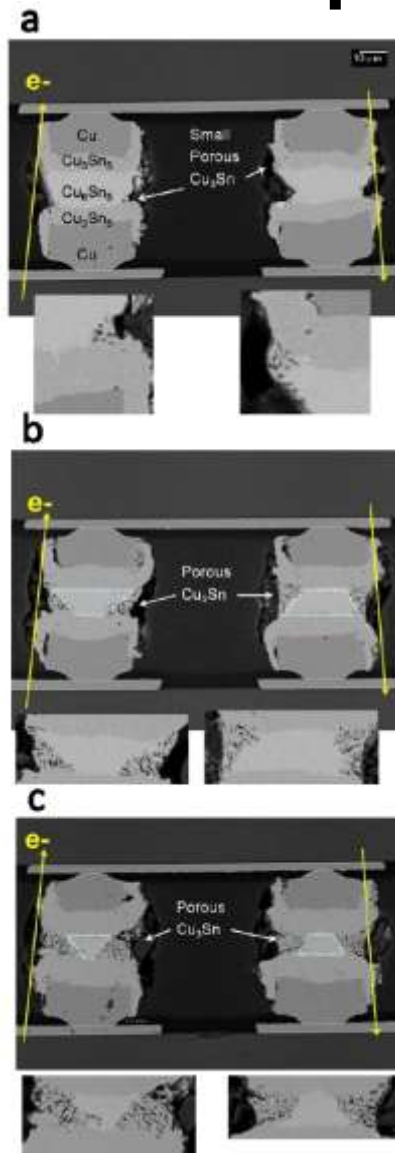
- High current density
- Thermal and thermodynamic stresses
- Geometrical discontinuities (vias and contacts)
- Microstructural flux divergence paths
- Material and chemical properties



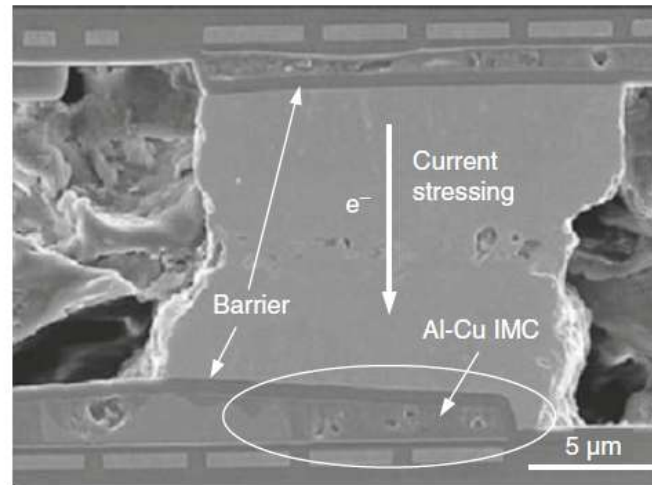
A!

Ref: C. Chen *et al.*, Annu. Rev. Mater. Res., vol. 40, pp. 531-555, 2010.

Literature reports – Cu-Sn IMCs EM tests

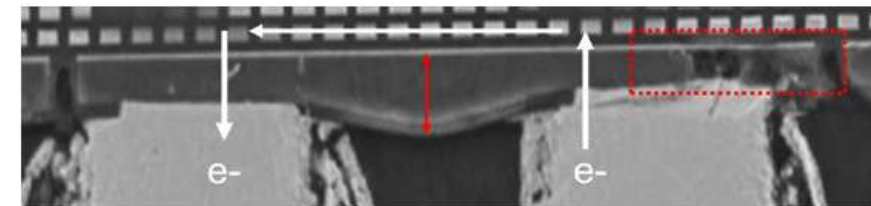
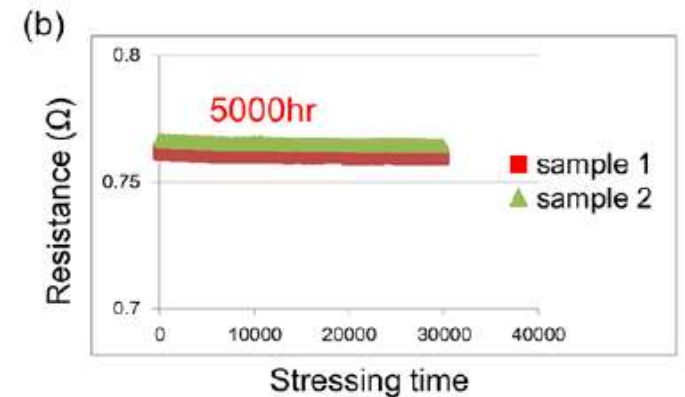
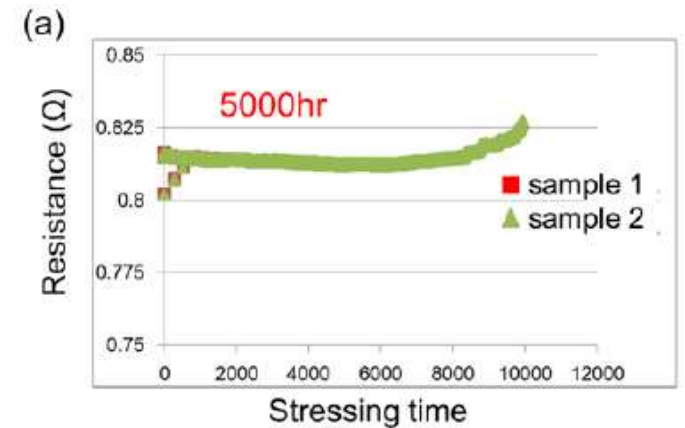


Resistance increase – 10%, 25%, 50%



Test conditions: $4 \times 10^5 \text{ A/cm}^2$ @ 200°C
for 1000 hours

Ref: A. Munding et al., in Wafer Level 3-D ICs Process Technology, C. S. Tan, R. J. Gutmann, and L. R. Reif, Eds. New York, NY, USA: Springer-Verlag, 2008, pp. 131–169



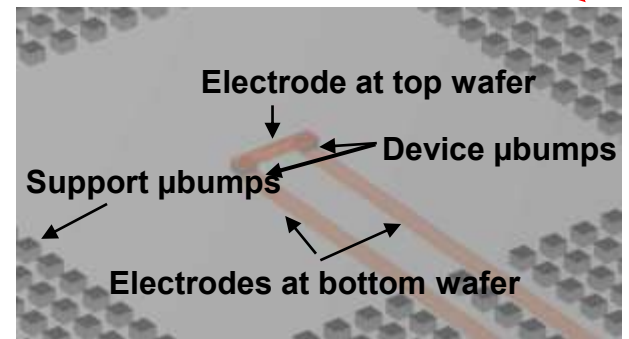
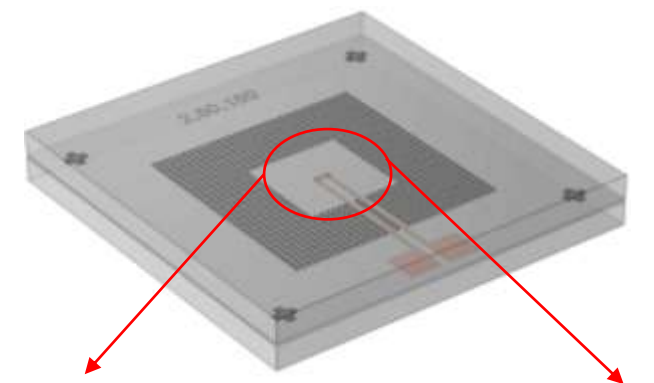
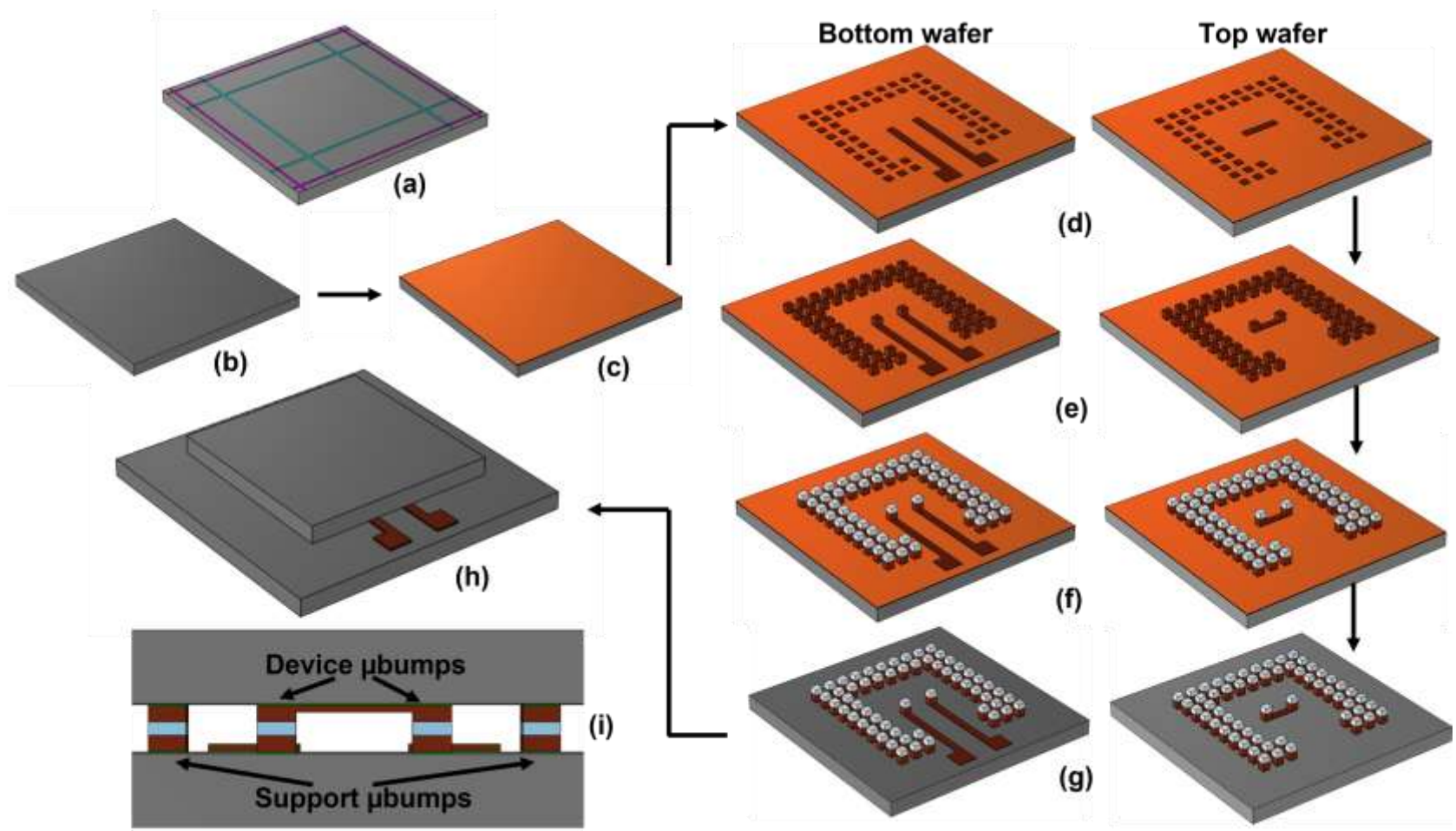
Test conditions: $2.1 \times 10^5 \text{ A/cm}^2$ @ 180°C

Ref: H.-Y. Chen et al., Proc. IEEE 65th Electron. Compon. Technol. Conf. (ECTC), San Diego, CA, USA, May 2015

A! Ref: Y-C. Chu et al., Proc. 2010 Intern. Conf. Electron. Packagin. (ICEP), Hokkaido, Japan, Jun 2016

The SLID bumps were manufactured by reflowing with SnAg bumps

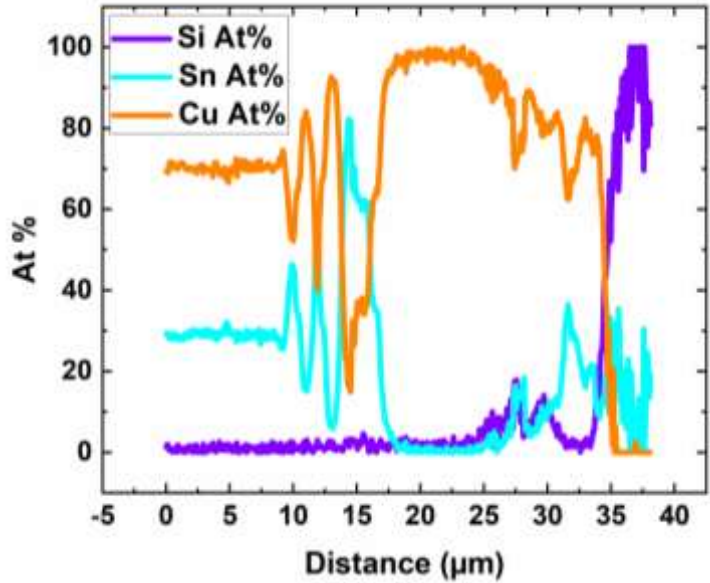
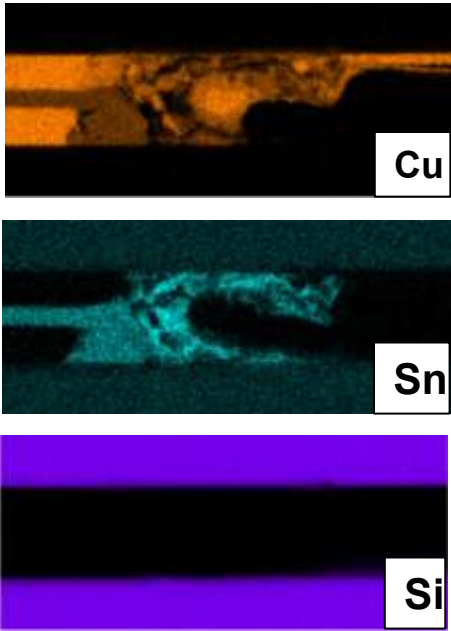
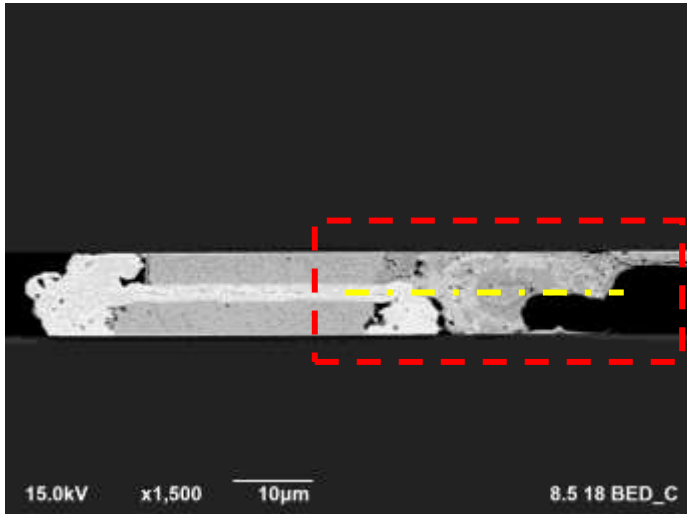
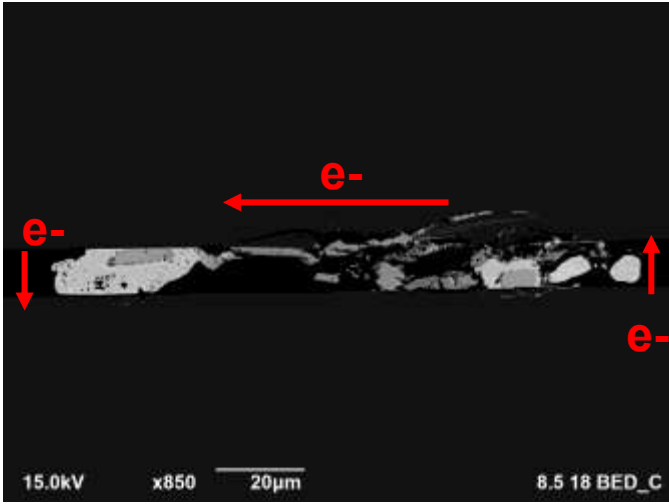
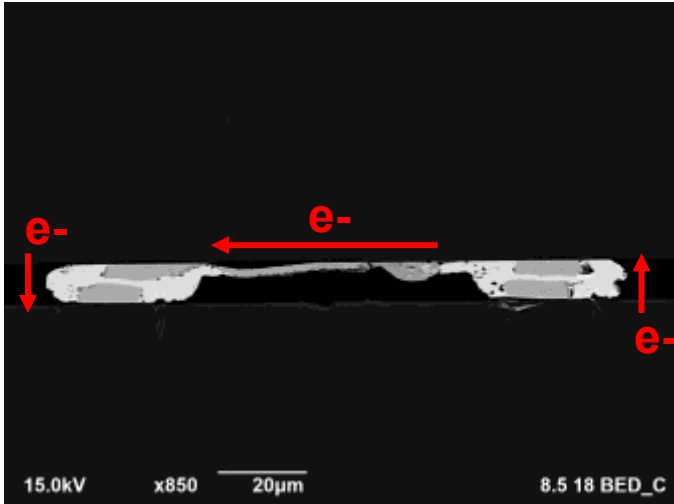
Fabrication process of Cu-Sn SLID test structures



A!

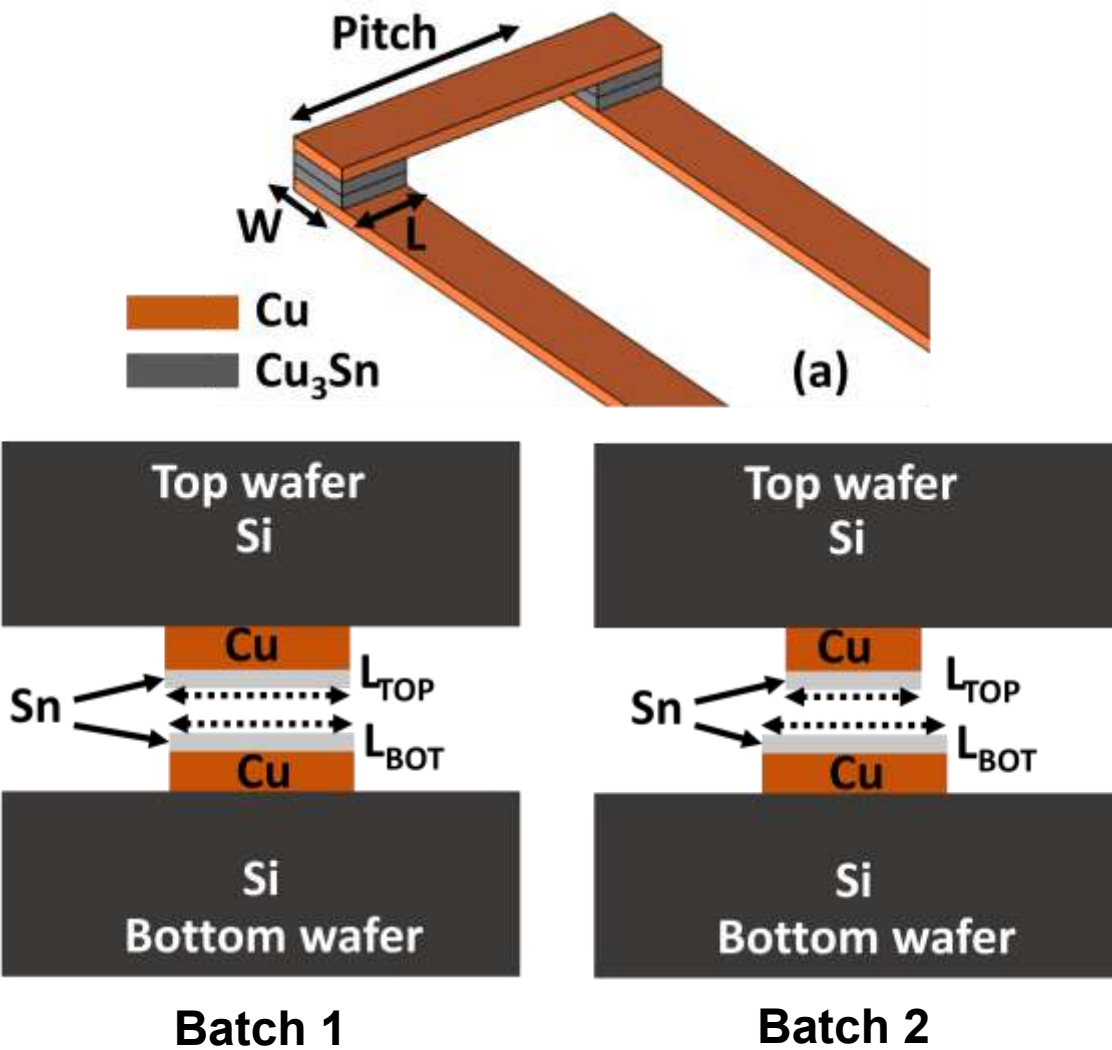
100 mm wafer level bonding was demonstrated

EM test results



A!

Design improvement to overcome Sn squeeze-out issue

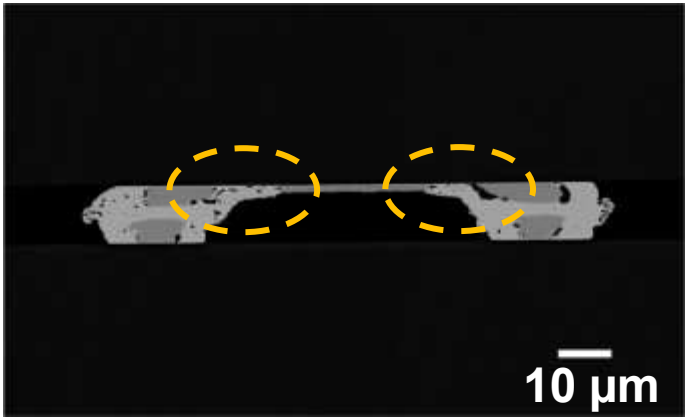


Dimensions of bottom and top μbumps in Batch-2

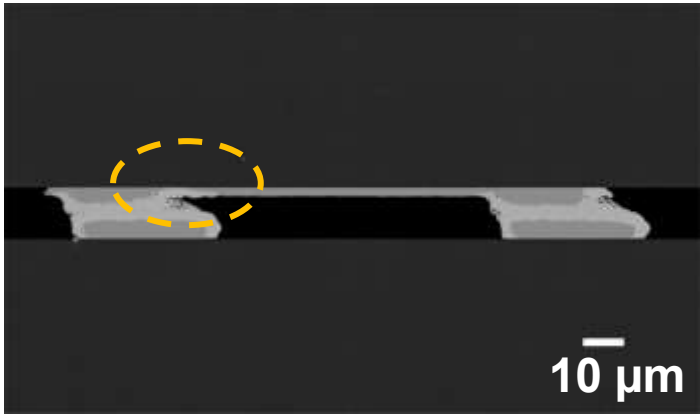
Bottom bump, $L_{BOT} = W_{BOT}$ (μm)	Top bump, $L_{TOP} = W_{TOP}$ (μm)
25	20
35	25
50	40
50	30

A!

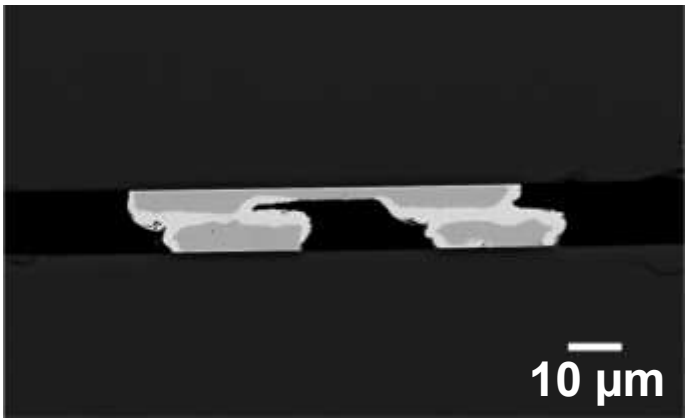
Fabrication results



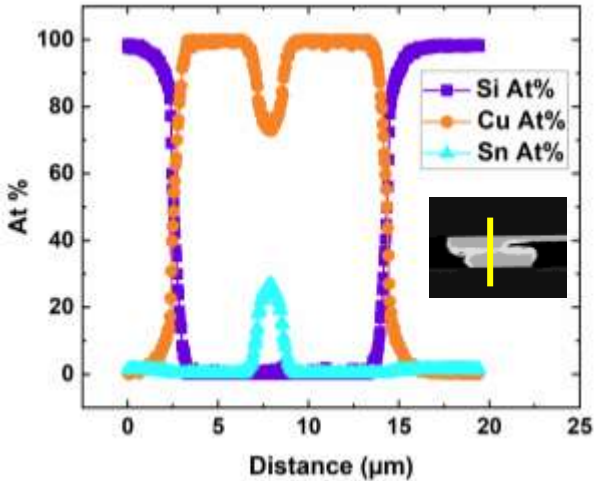
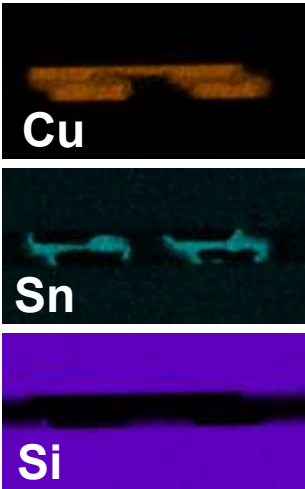
Batch 1, 25 μm



Batch 2, 35 μm

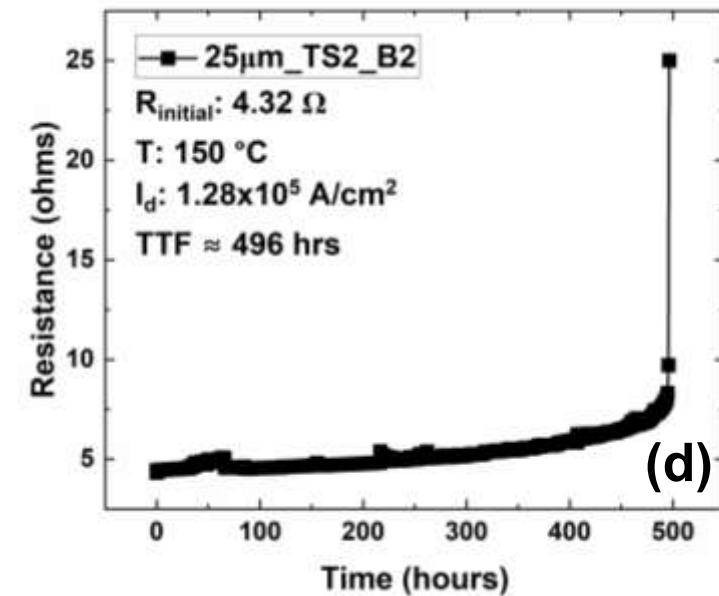
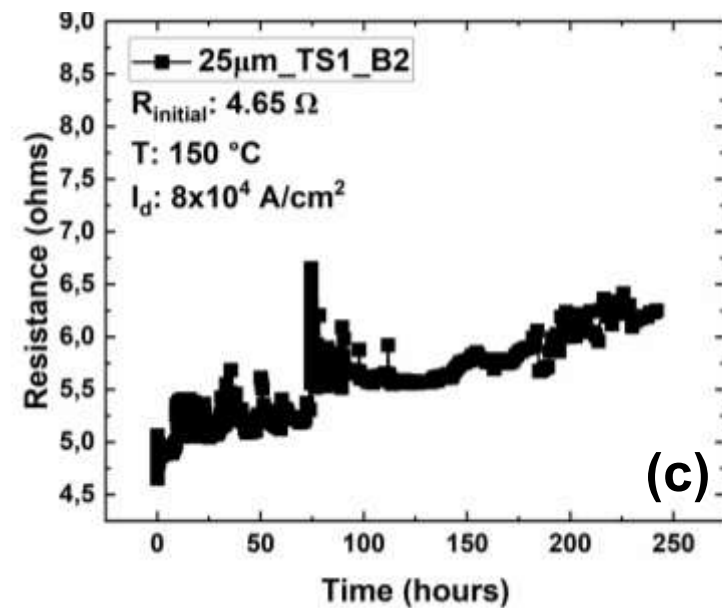
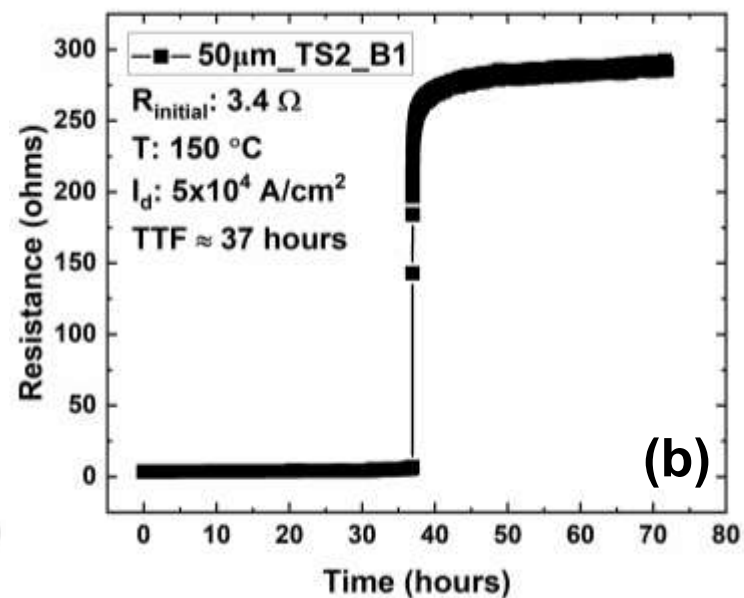
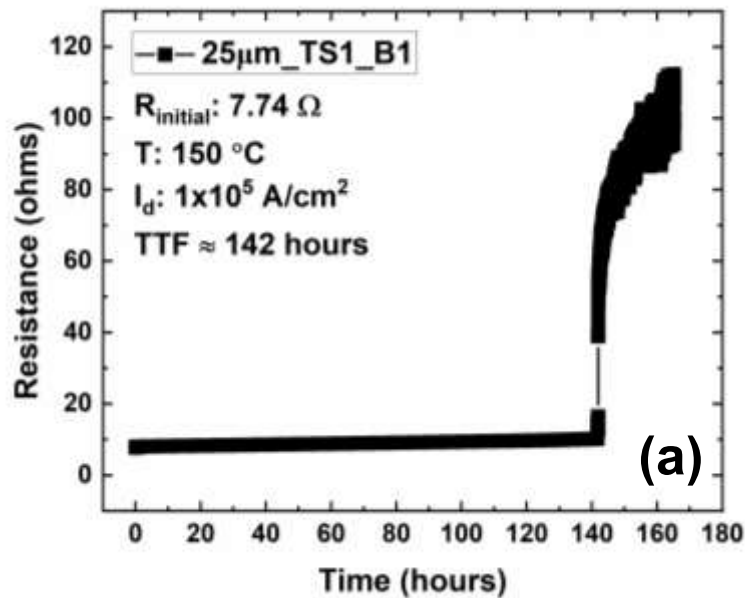


Batch 2, 25 μm



A!

EM test results

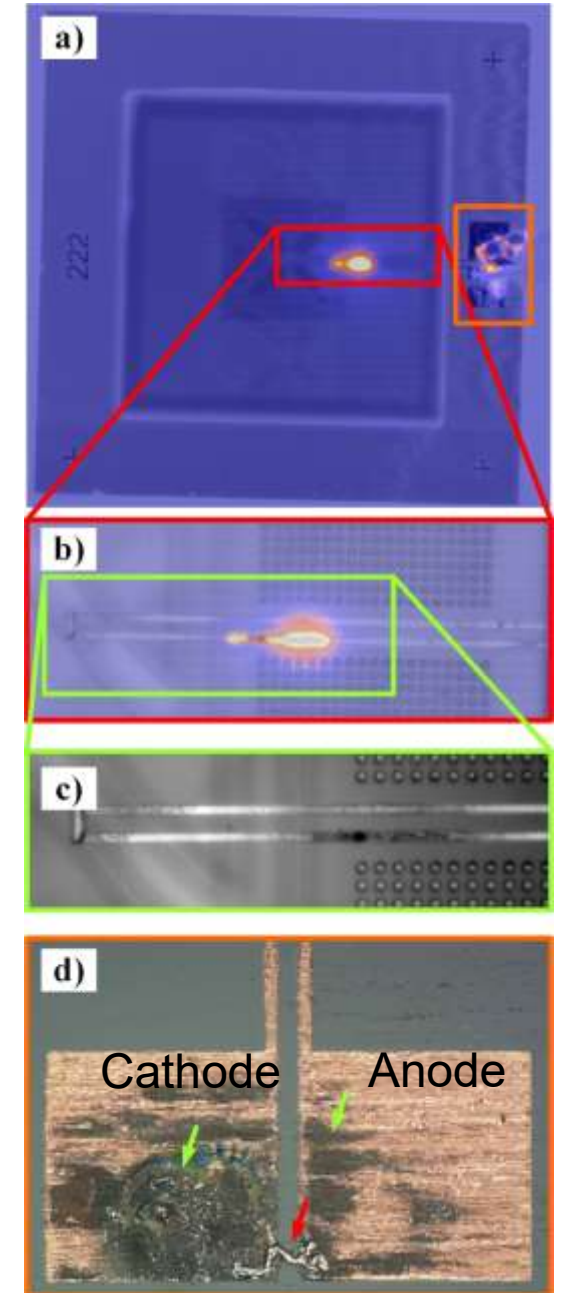
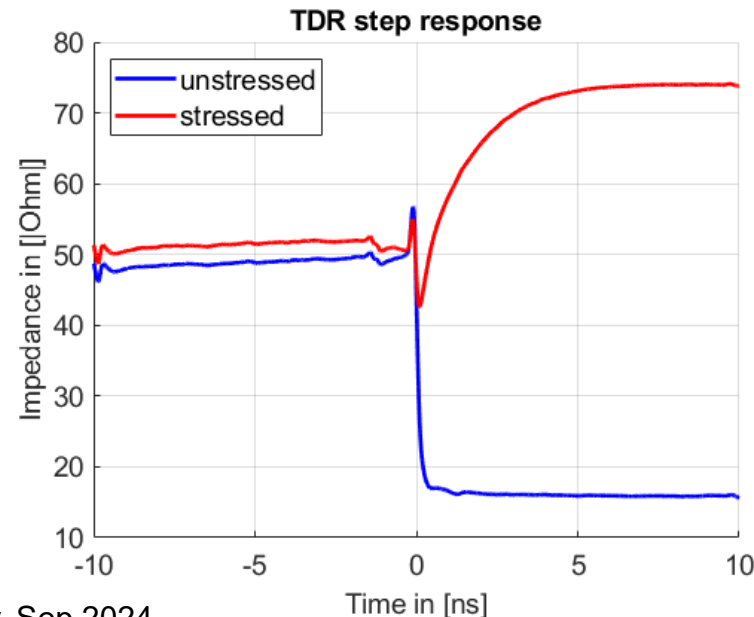
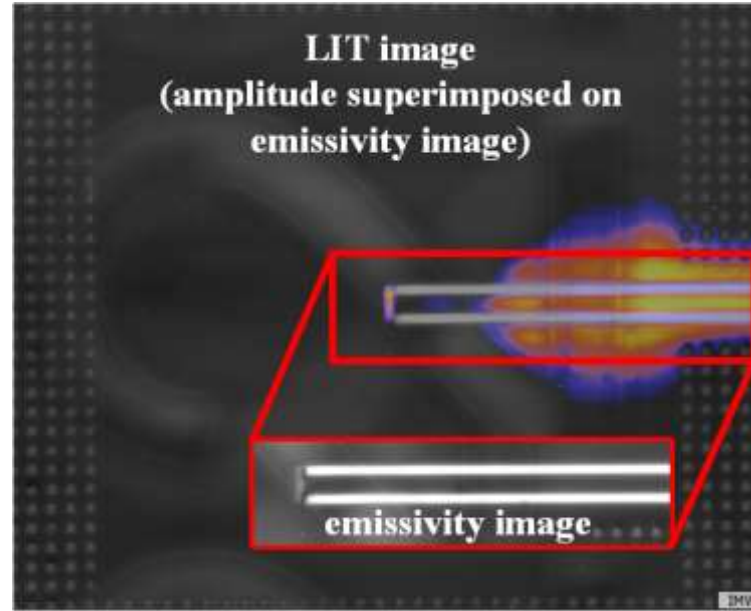


New design resulted
in $\approx 500 \text{ hrs}$ of TTF

A!

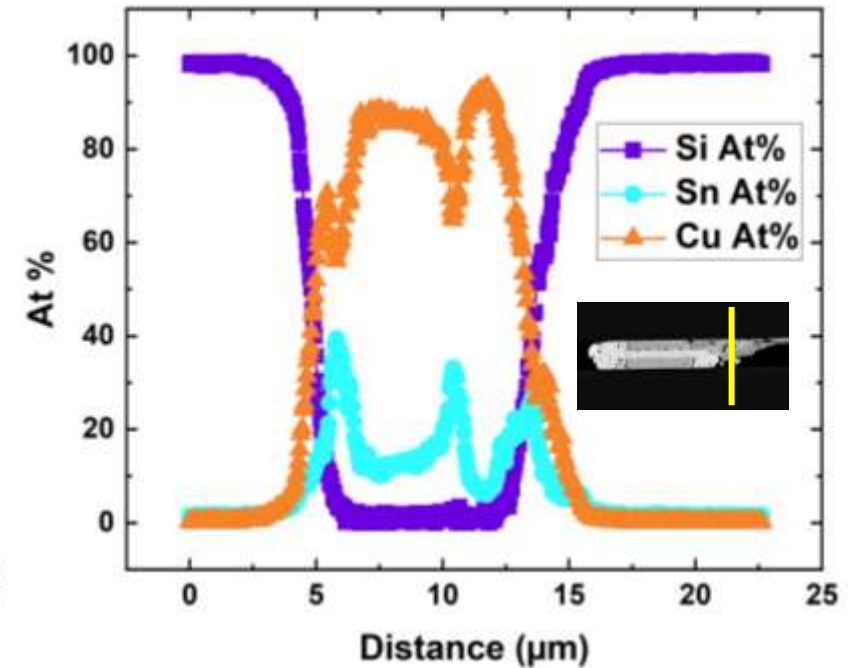
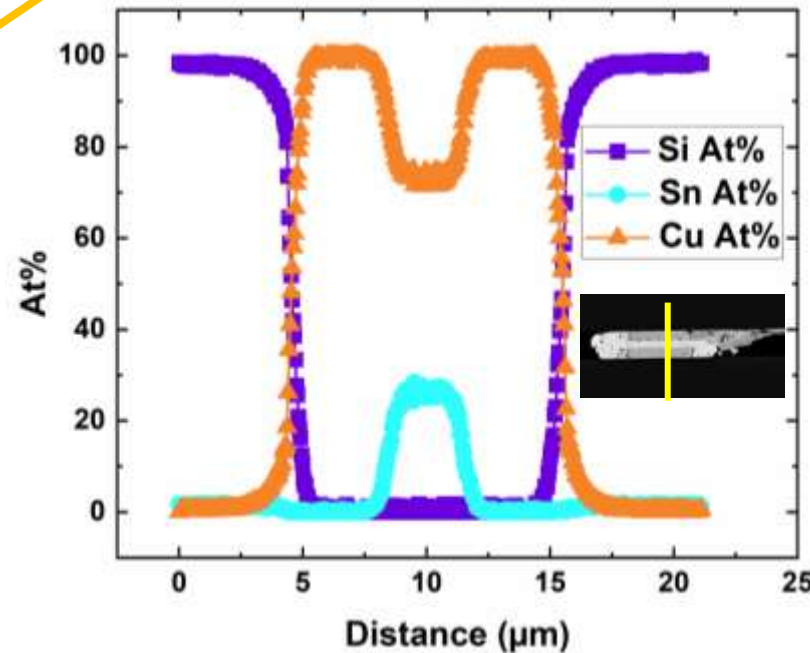
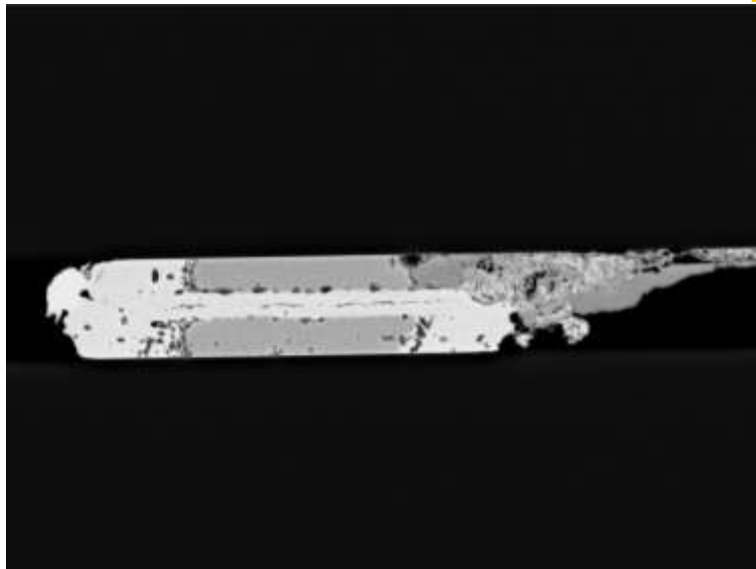
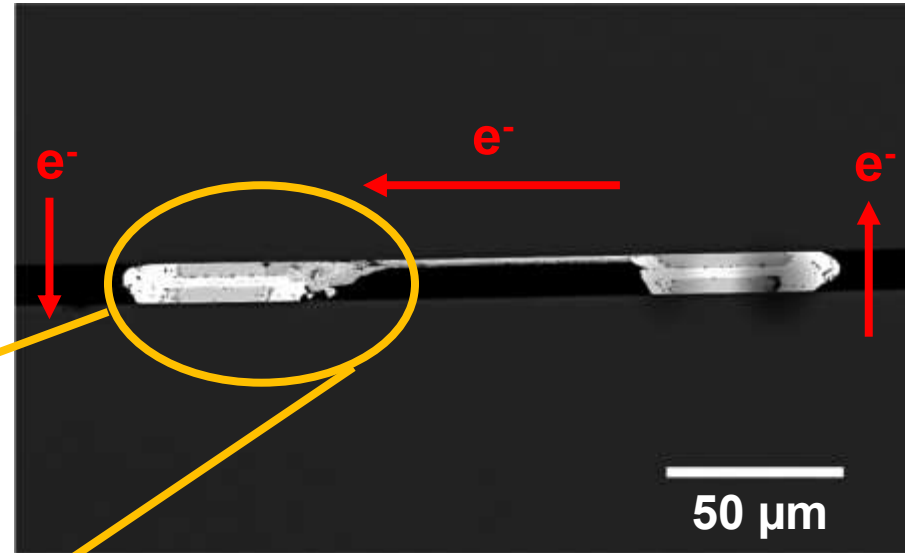
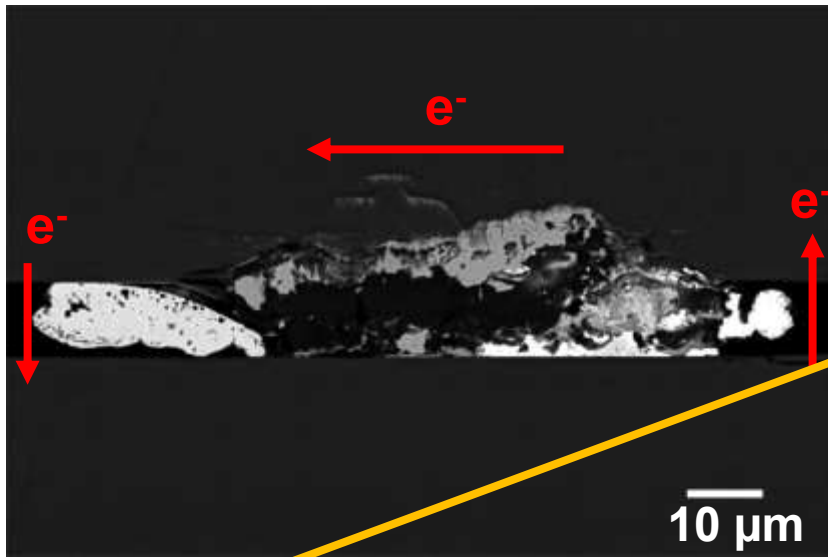
Non-Destructive failure analysis

- A combination of lock-in thermography (LiT) and time domain reflectometry (TDR) was carried out to locate failure locations non-destructively
- ND analysis indicated failures in the Cu traces and contact pads and not in Cu_3Sn μ bumps for Batch 2 samples

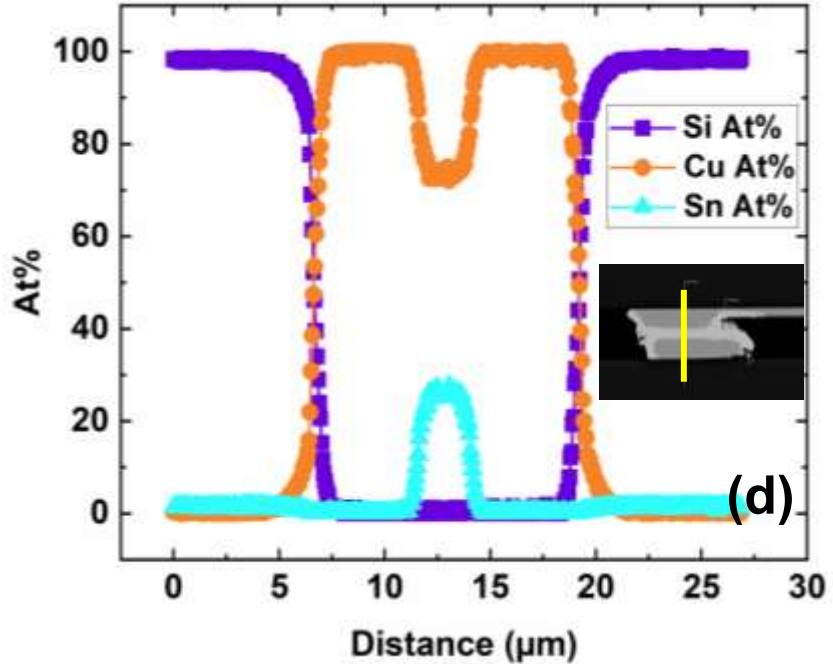
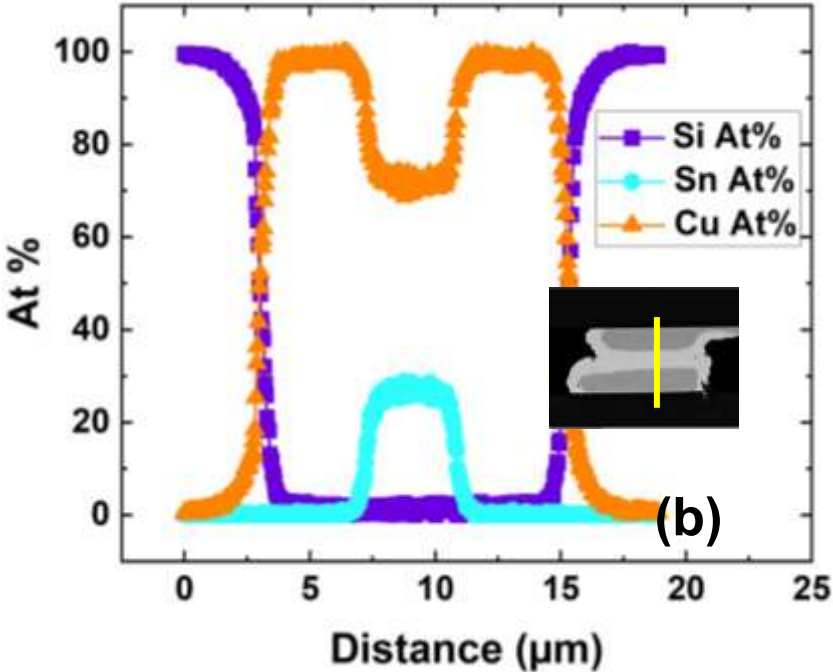
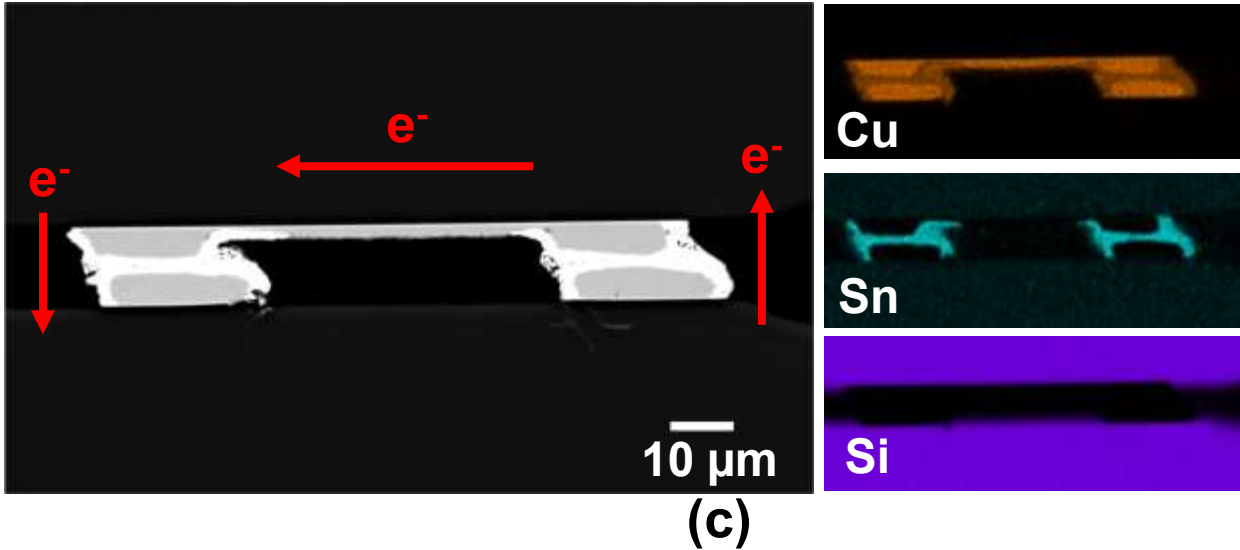
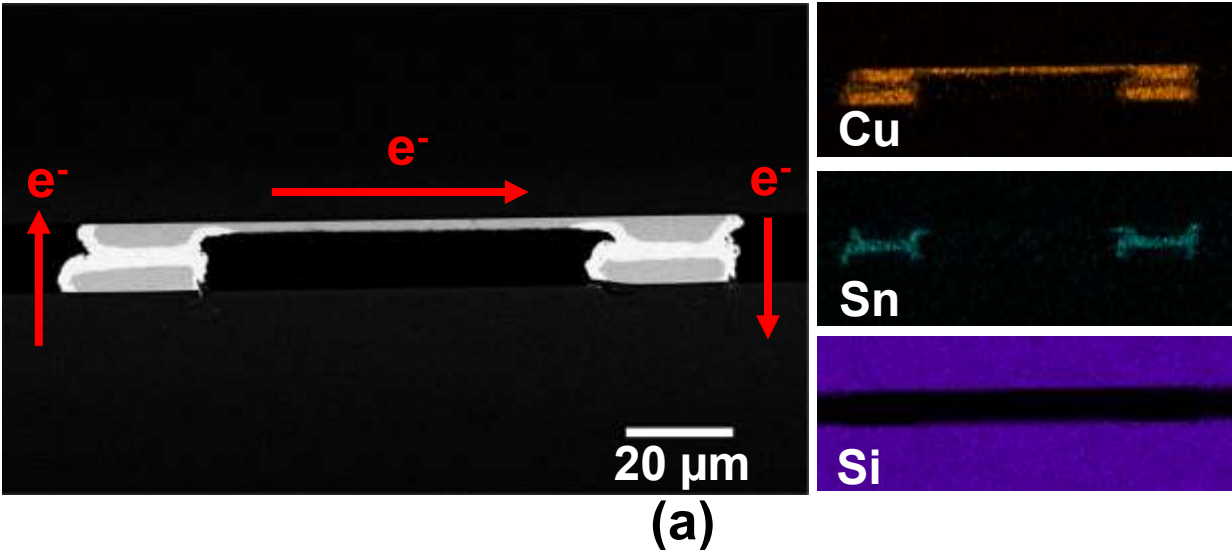


A!

Destructive failure analysis (Batch 1 samples)

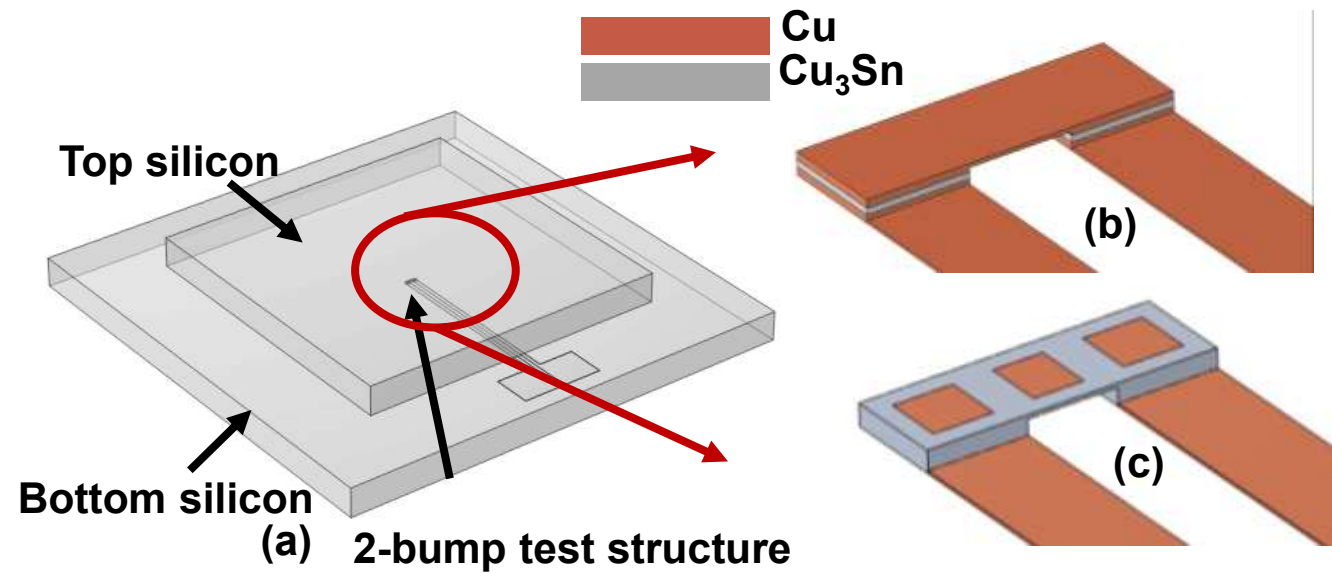


Destructive failure analysis (Batch 2 samples)

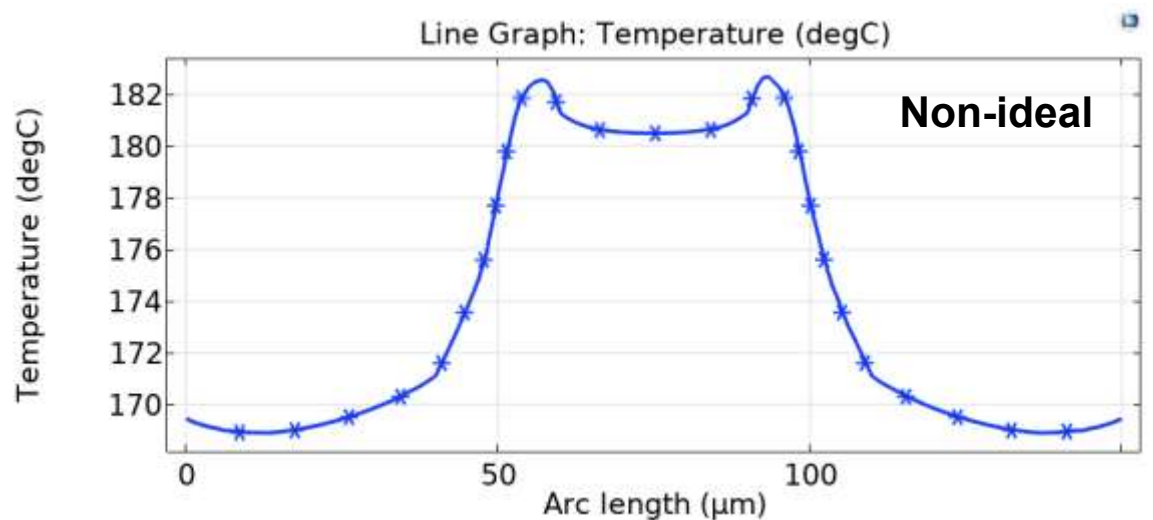
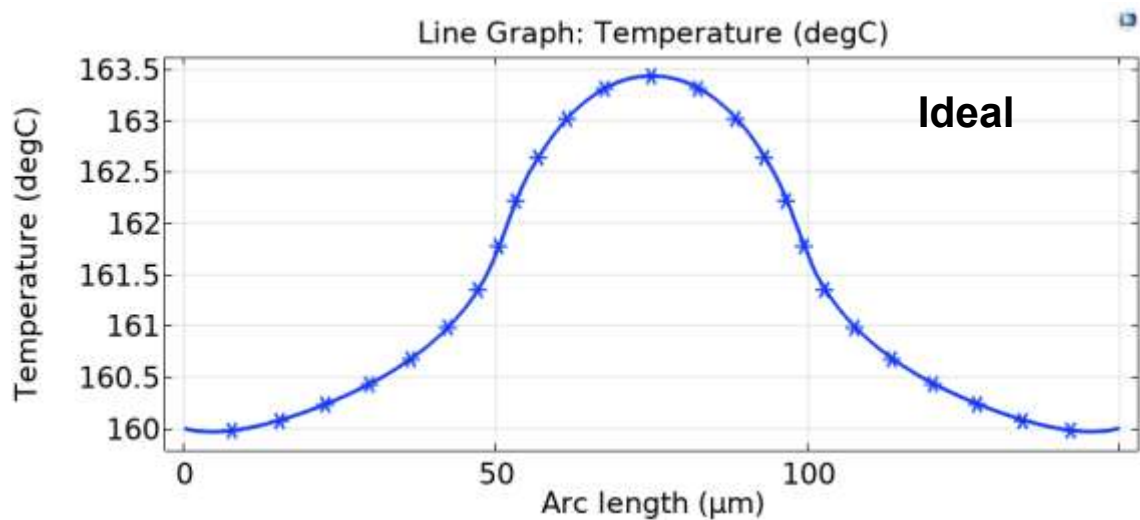
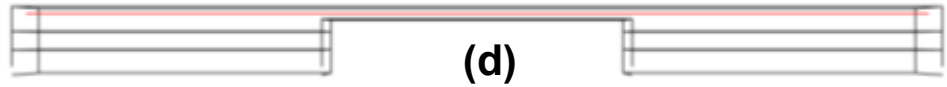


A!

FE simulations results

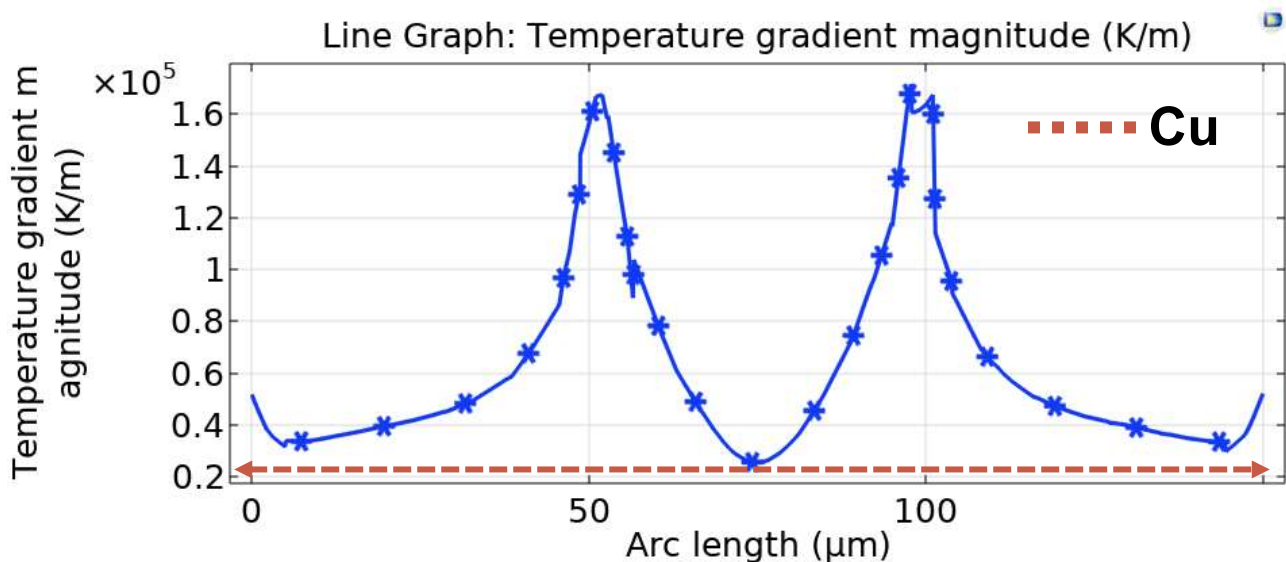
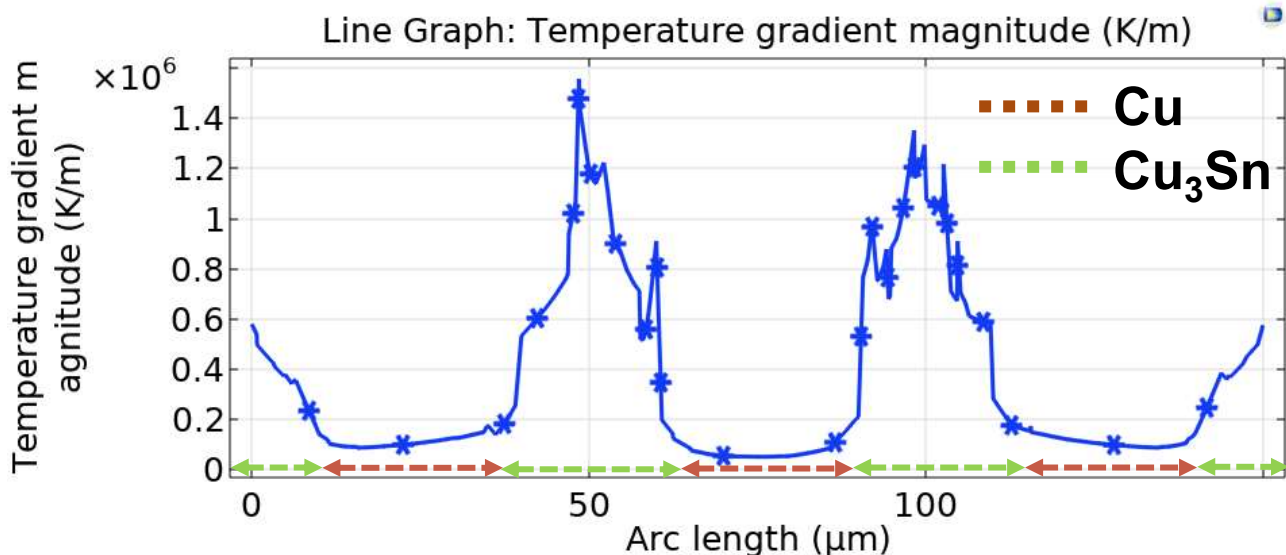
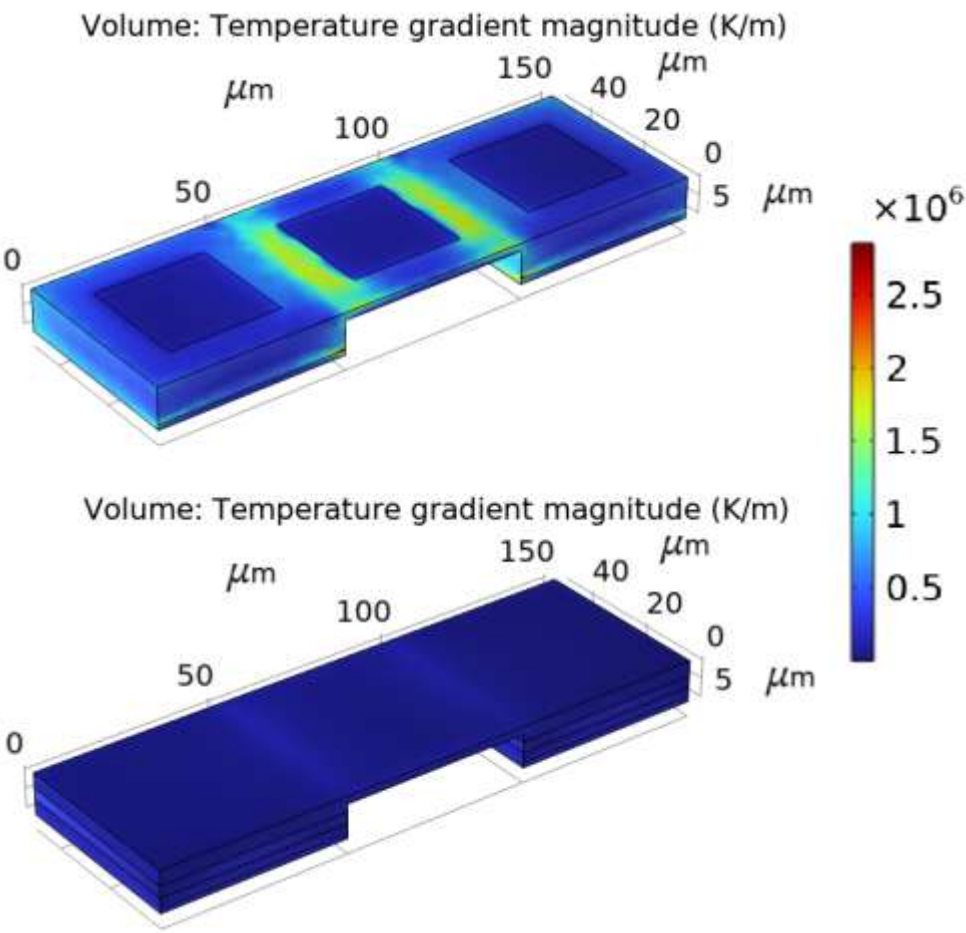


- Boundary conditions:**
- 1. Current density – $1 \times 10^5 \text{ A/cm}^2$
 - 2. Temperature at the bottom – $150 \text{ }^\circ\text{C}$
 - 3. Convective heat flux transfer at the top – $5 \text{ W/m}^2\cdot\text{K}$



A!

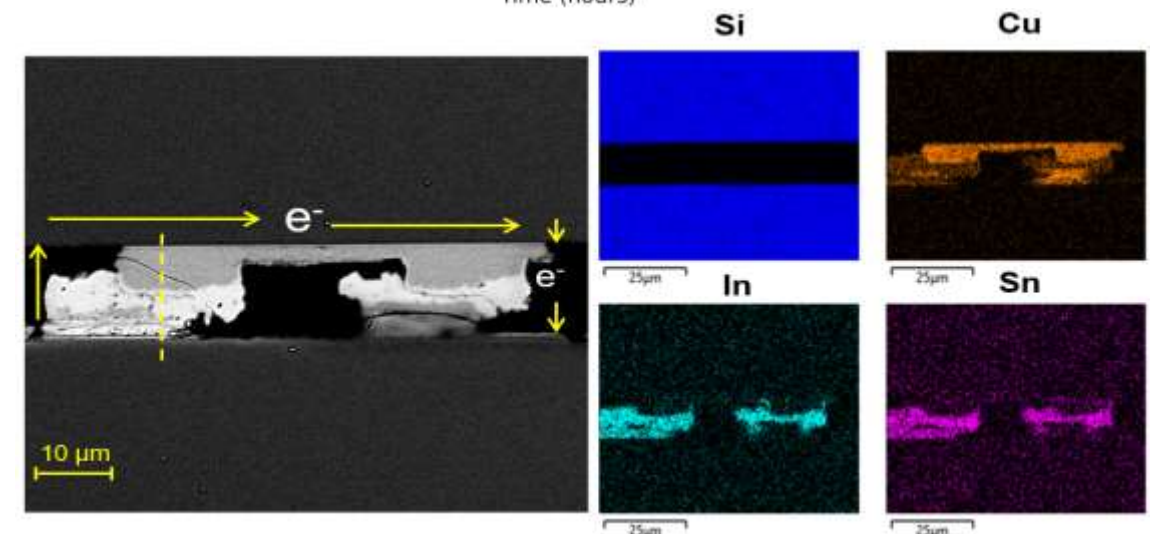
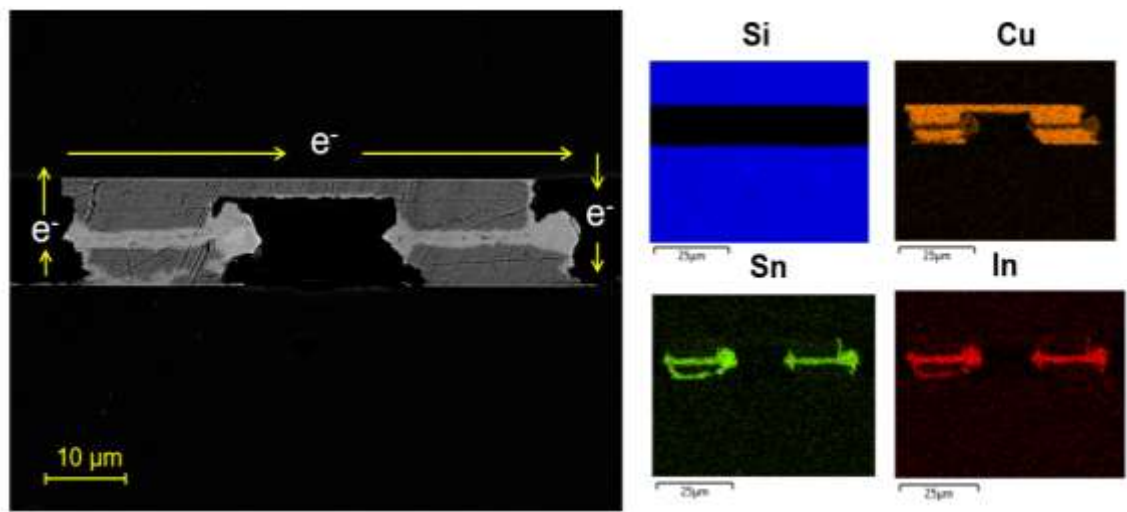
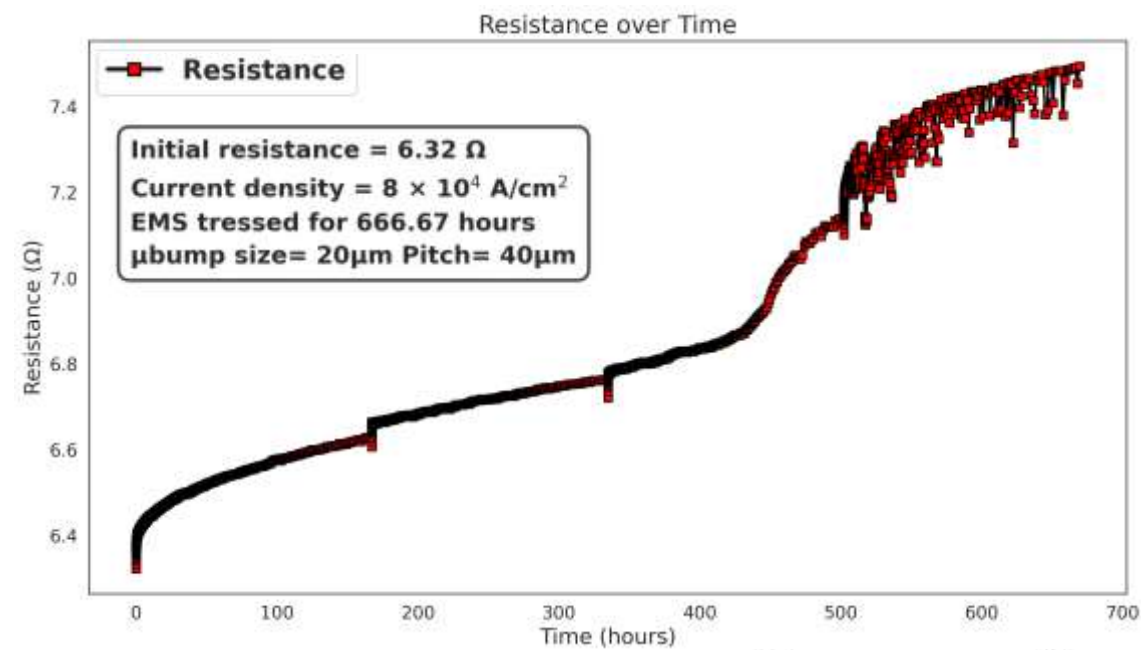
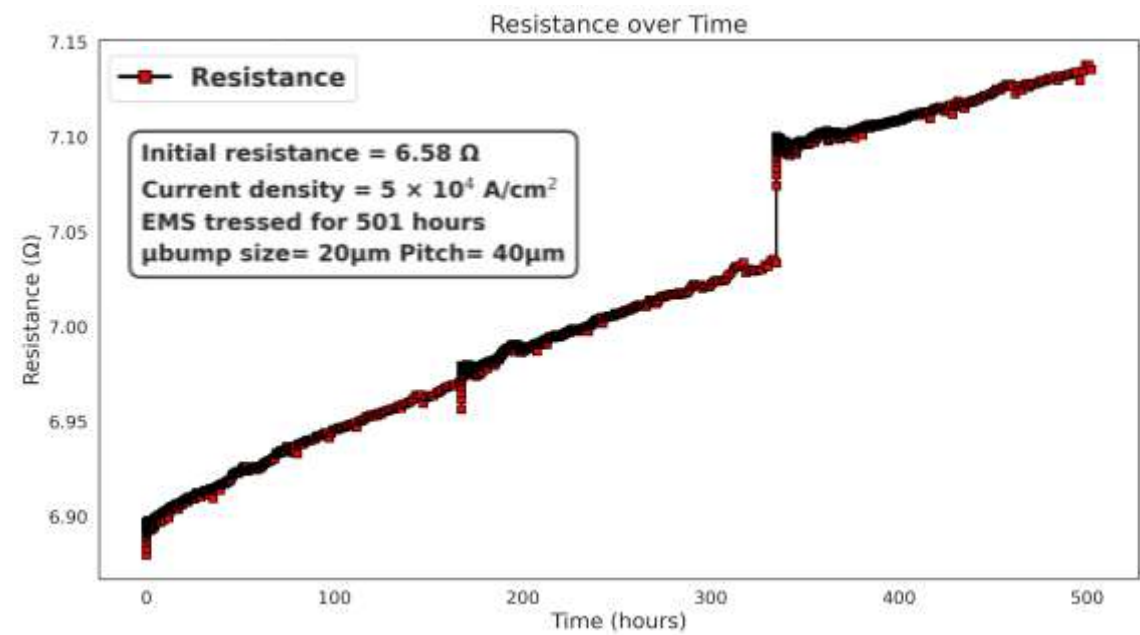
FE simulations results (contd.)



A!

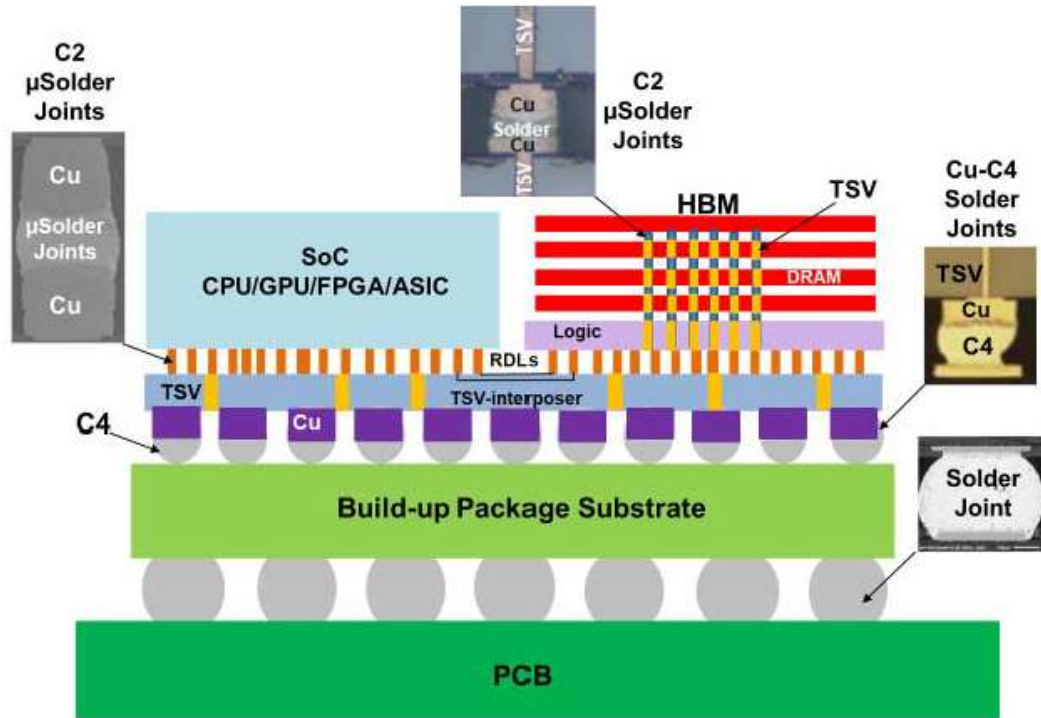
EM test results of Cu-Sn-In SLID bumps

150 mm wafer level bonding at LT of 150 °C



SLID electrical performance – RF

RF performance metrics

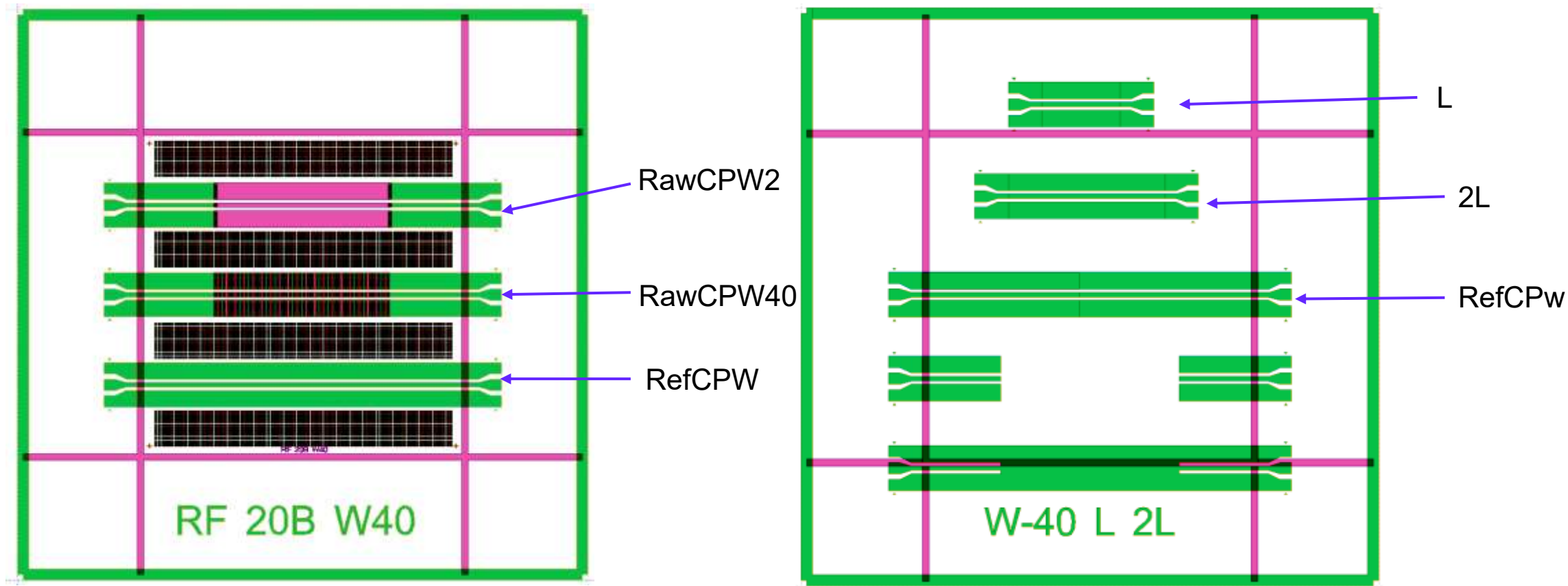


2.5D IC integration for HPC

Ref. J. H. Lau, IEEE TCPMT, vol. 12, pp. 228-252, 2022

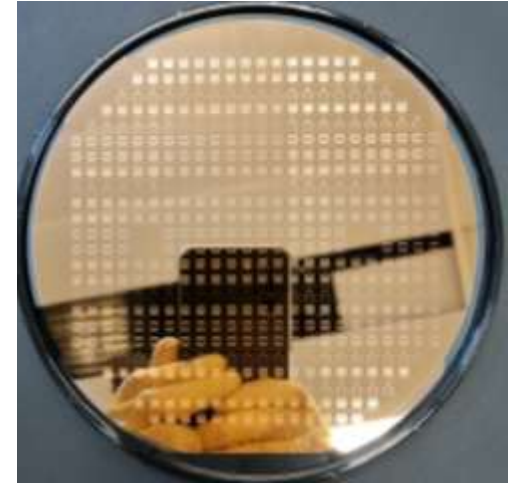
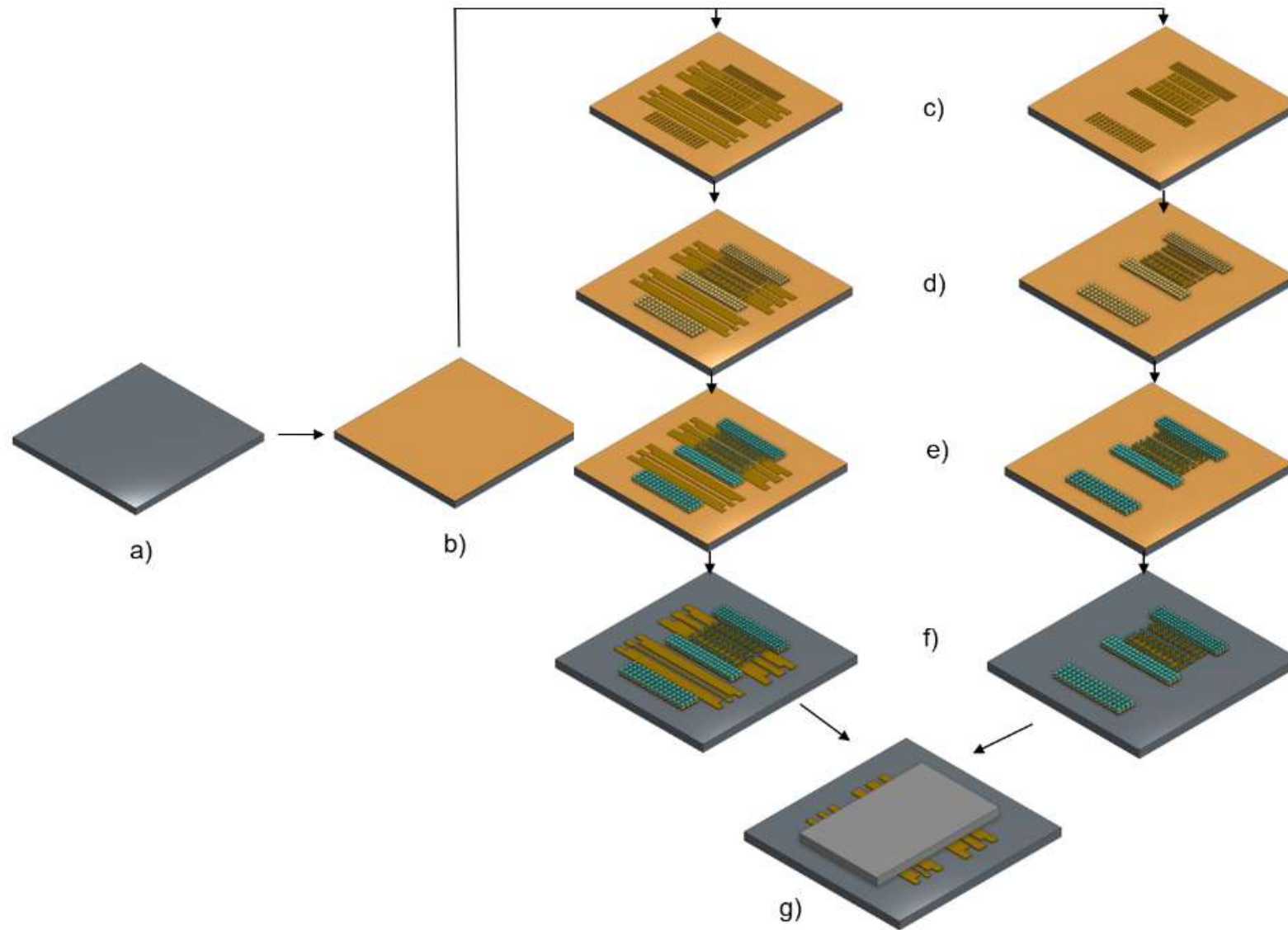
- Short-distance chip-to-chip links are critical for high-performance computing, enabling higher data rates, greater bandwidth, and lower latency.
- Small volume interconnects minimize parasitic R, L, and C, improving signal integrity and power efficiency.
- Manufacturing should be low cost, low complexity, and low thermal budget to align with More-than-Moore integration and protect sensitive backend structures.
- The RF transmission performance of SLID microbumps has been assessed and demonstrated.

Mask layout



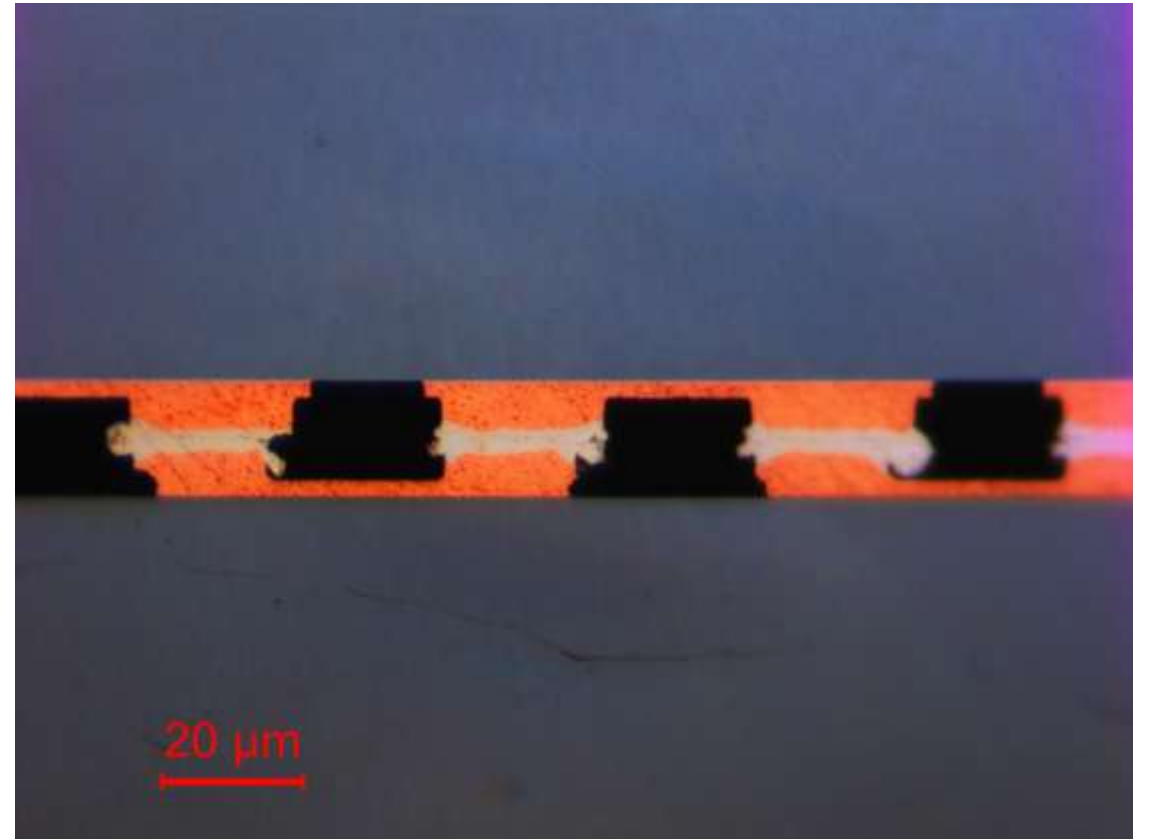
A!

Fabrication process flow



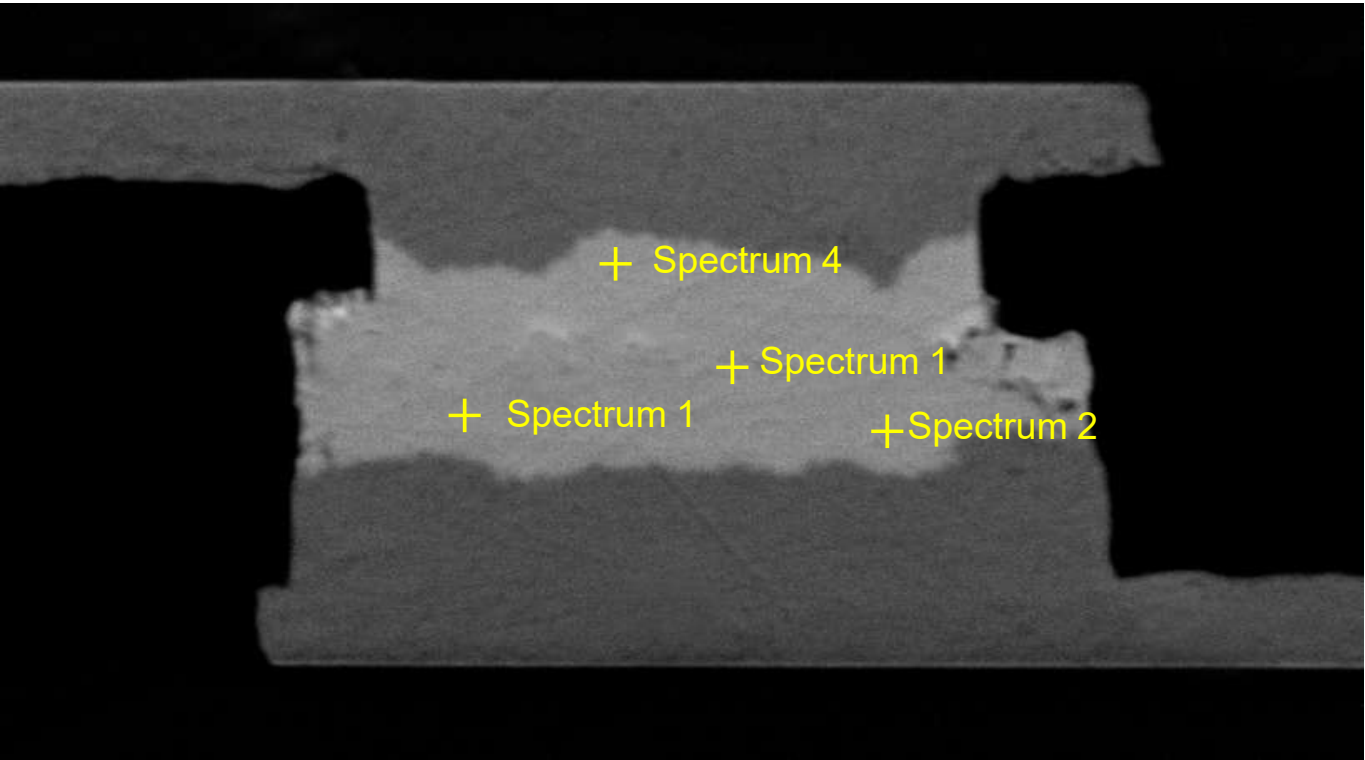
A!

RF device cross-section



A!

Point analysis

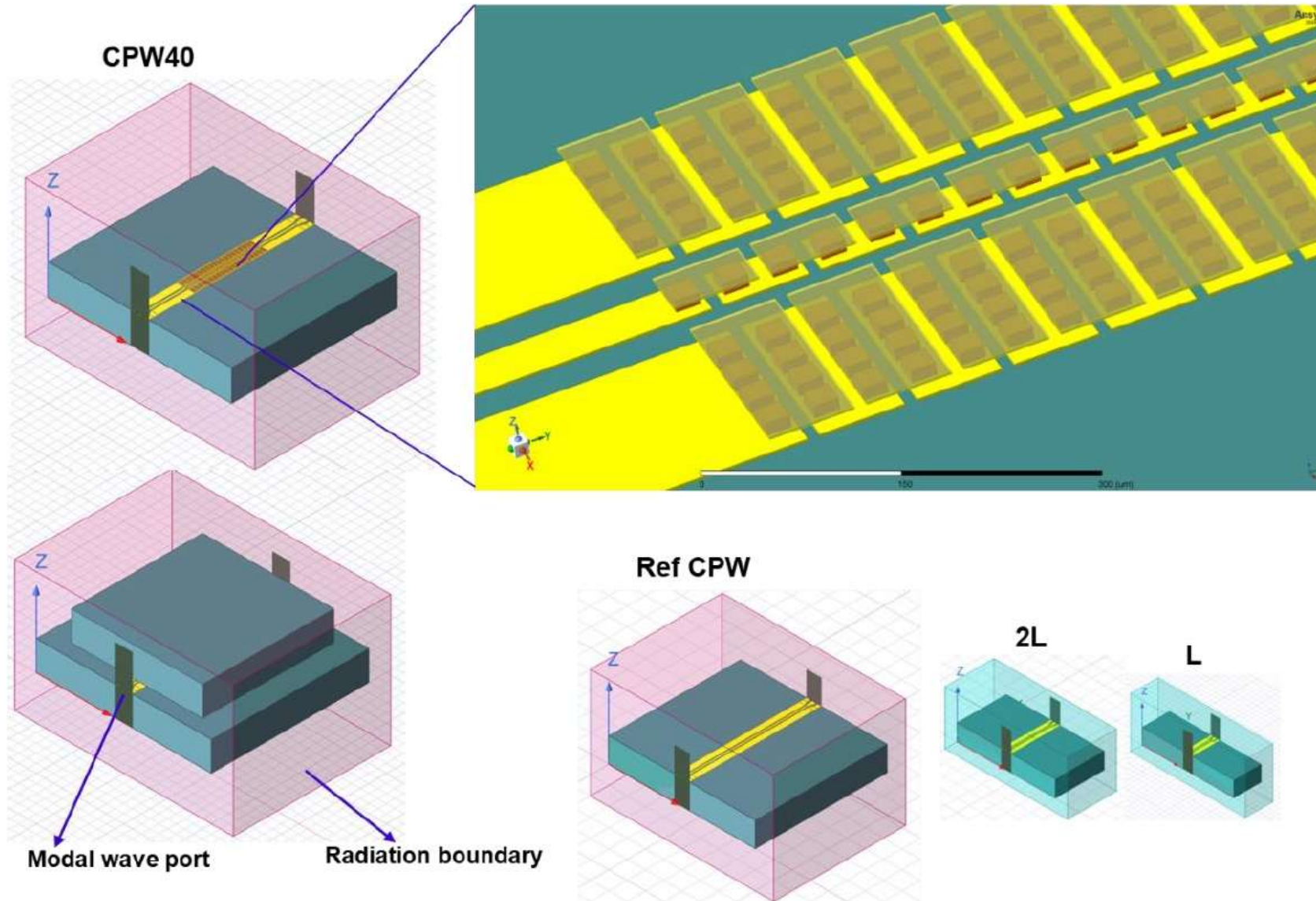


	At %		
	Cu	Sn	In
Spectrum 1	54.2	24.5	21.3
Spectrum 2	54.6	25.1	20.3
Spectrum 3	55.1	24.4	20.5
Spectrum 4	52.8	25.0	22.3

A!

Indicates $\text{Cu}_6(\text{SnIn})_5$ was formed

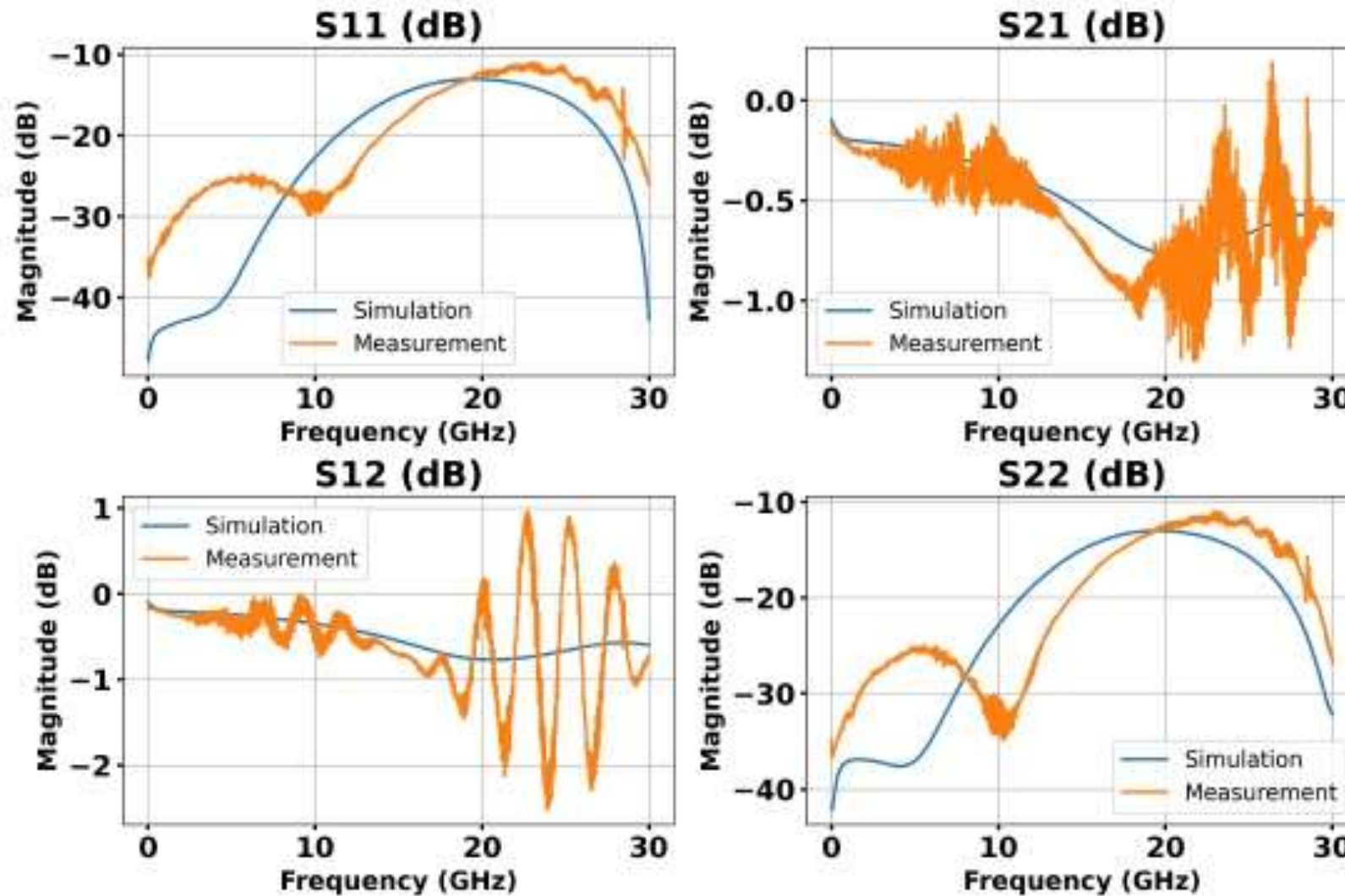
HFSS Model with CPW40



A!

Ref: T. Ukubay, M. Paulasto-Kröckel, N. Tiwary, *IEEE 11th ESTC*, Helsinki, Finland, Sep 2026,

Measurement vs HFSS simulation results



A!

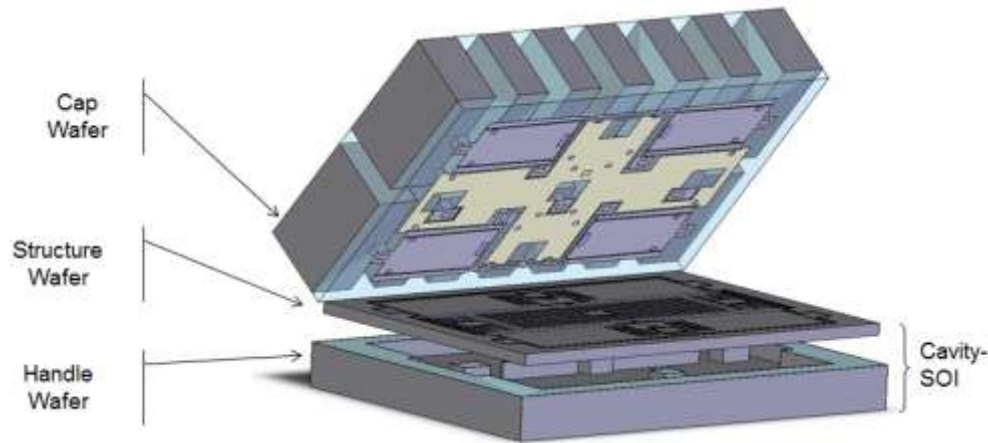
Measured and simulated S-parameters of the RF test structure containing 40 Cu-Sn-In microbumps

SLID for MEMS

Different wafer bonding methods

WB method	Typical proc. temp.	Typical bond frame width	Pros	Cons
Fusion	400-1000°C	300µm	Strong bonds High stability of the bond	High bonding temperature Poor surface contamination tolerance
Anodic bonding	Strong bonds, Small footprint Tolerance for topographies and surface contaminations Low to medium bonding temperature available Excellent hermeticity for MEMS applications Possibility to combine hermetic sealing and electrical interconnections with in the same process			Lack of data Process integration Intrinsic stresses Control of liquid metal squeeze-out
Glass bonding				
Adhesive bonding				
Metallization				
			and electrical interconnections with in the same process	

Metal wafer bonding for hermetic packaging



Devices	Structure	Hermetic Packaging
Accelerometer	bulk	yes
Gyroscope	bulk	yes
Resonator	bulk	yes
RF relay switch	bulk	yes
Micro pump	bulk	no
Mirror	bulk	no
Pressure sensor	membrane	no
Microphone	membrane	no
Valve	membrane	no

A!

TABLE 26.1 Types of metal seal bonding and related typical peak process temperatures.

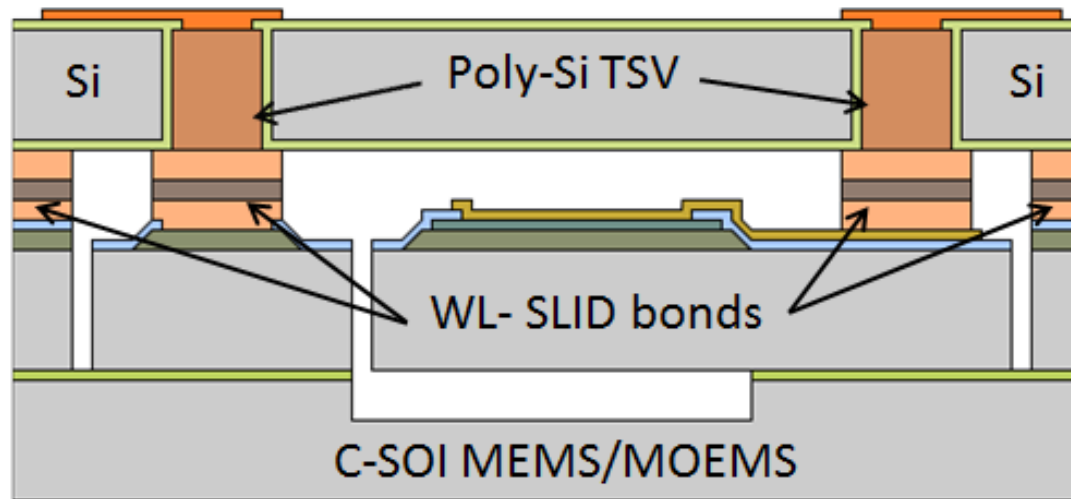
Bonding technique	Types of metal seal bonding	
	Metal system	Bond temperature (°C)
Soft soldering bonding	SnAg to Cu/Ni/Au	240
	SnPb to Cu/Ni/Au	210
	SnBi to Cu/Ni/Au	160
Eutectic bonding	Au to Si	400
	Au to SiGe	400
	Au to Ge	400
	Al to Ge	425
	AuSn to Au	300
	AuIn to Au	160
Transient liquid-phase bonding	CuSn to Cu	280
	AgSn to Ag	250
	AgIn to Ag	250
	AuSn to Au	260
	NiSn to Ni	300
	AuIn to In	175
Thermocompression bonding	Au to Au	380
	Cu to Cu	350
	Al-Al	450
	Al-Al	100–150 ^a
Ultrathin metal film	SiO ₂ Ti to Si	400
Reaction bonding	Ni/Al RMS + Sn to Au	RT
	AlPd RMS to Al	RT

The temperatures mentioned here are for guidelines only. The exact process temperature needs to be determined based on the package design, yield, and throughput required. RMS, Reactive metal layer stack.

^aAl to Al using dedicated surface preparation process [8,9].

Process Integration and Reliability of Wafer Level SLID Bonding for Poly-Si TSV capped MEMS

A summary from the Finnish cluster activities on *Design for manufacturability and reliability of metal bonding for wafer-level MEMS/MOEMS packaging* in ENIAC project Lab4MEMS II “Micro-Optical MEMS, micro-mirrors and pico-projectors”



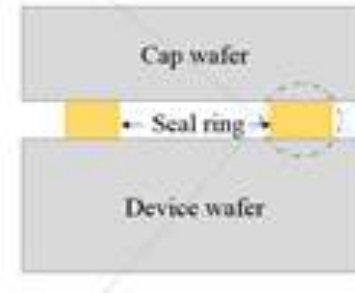
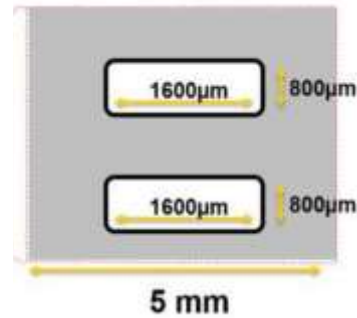
A!



Development process

■ Round 1

- Bond metallurgy
- Mechanical reliability

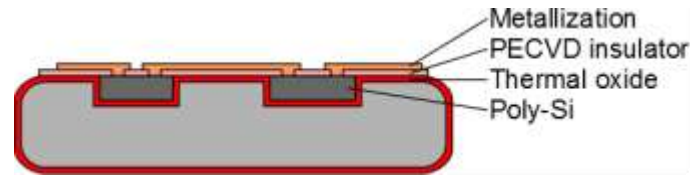


Group	Cap metallization	Device metallization
#6	TiW/Au/Sn	Ti/Mo/Ti/Pt(100nm)
#7	TiW/Ni(200nm)/Au/Sn	Ti/Mo/Ti/Pt(100nm)
#8	TiW/Ni(200nm)/Au/Sn	Ti/Mo/Ti/Pt(200nm)
#9	TiW/Ni(200nm)/Au/Sn	Ti/Pt(200nm)

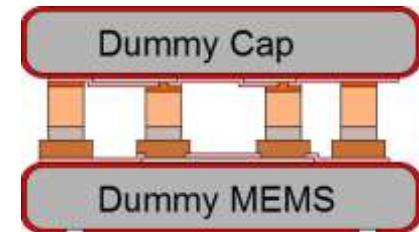
■ Round 2

- Fabrication Redistribution Layer (RDL) metallization & contacts to p-Si with the RDL.
- Bonding process

Round 2, TSV contact



Round 2, Bonding process

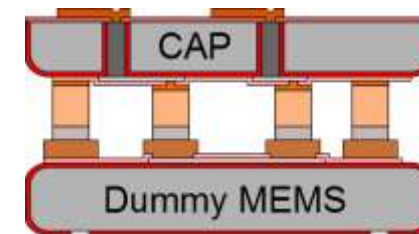


■ Round 3

- Process integration
- Electrical testing
- Reliability assessment

■ Round 4 Inertial MEMS demo

- Murata design
- VTTprocess
- Okmetic cap



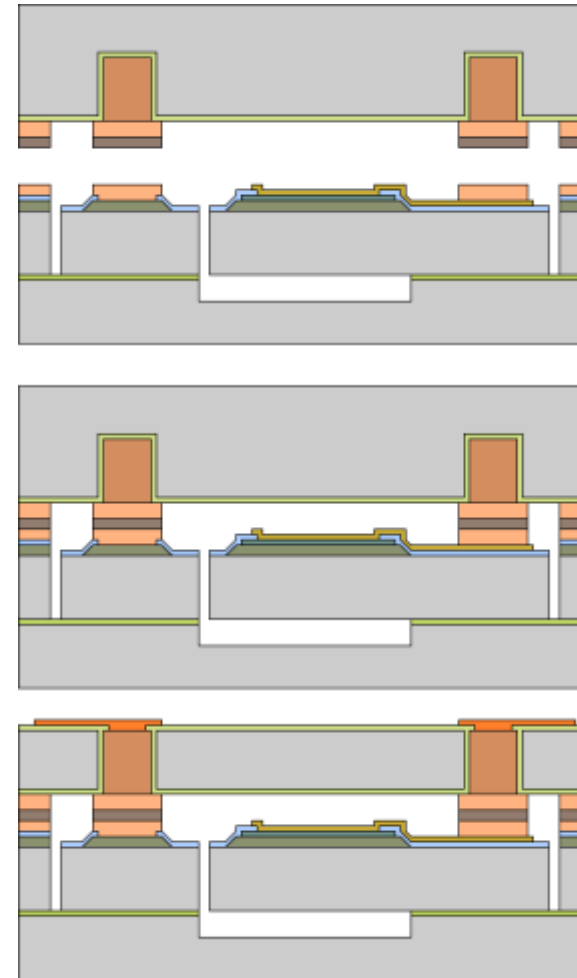
Round 3, process integration, Electrical and reliability performance

A!



Process integration – “vias before bonding”

- Process
 1. Fabrication of MEMS and Cap wafers separately
 2. Bonding
 3. Connection to the TSV back side



A!

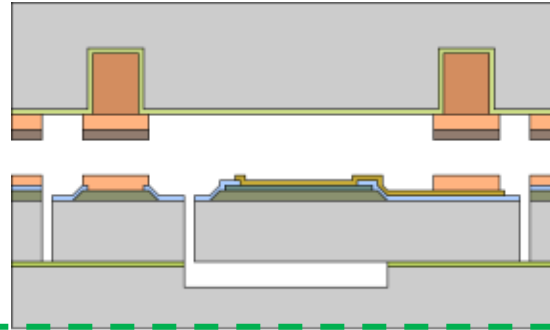
Additional info:



Round 4- Summary

1. Fabrication of MEMS and Cap wafers separately

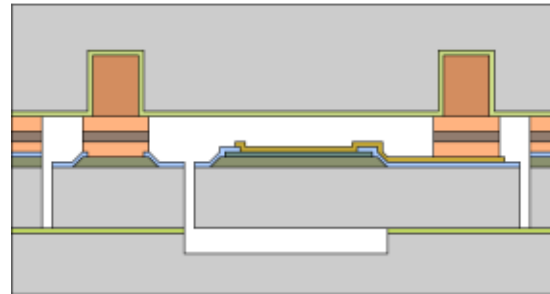
- + Process integration developed
- > 100 process steps



OK

2. Bonding

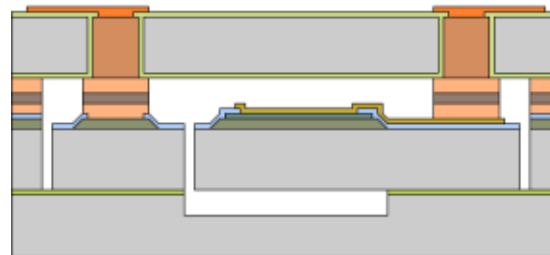
- + Process parameters OK
- Design topography challenges
- Some voids and fractures



OK?

3. Cap-side processing

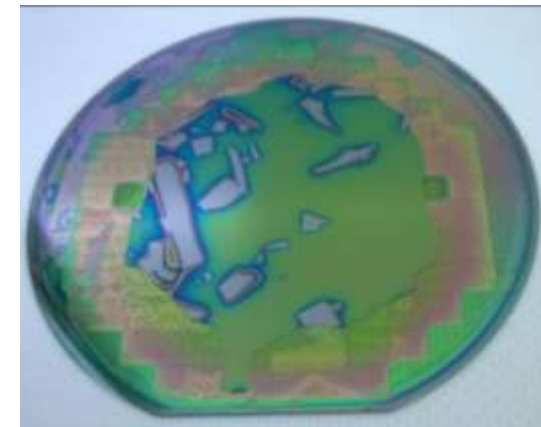
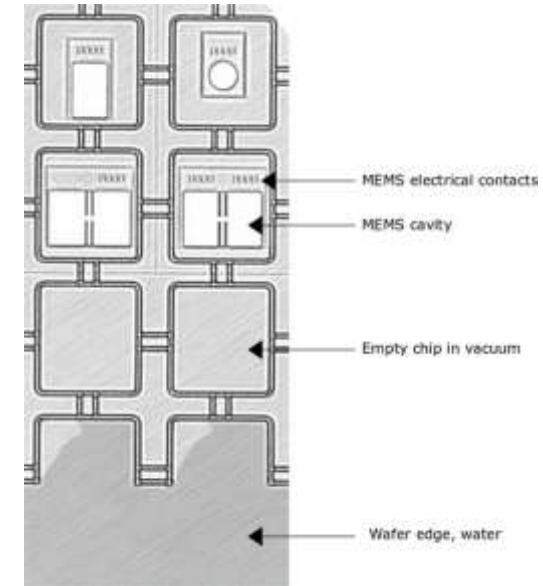
- Wafer cracking
- No functional characterization & hermeticity verification



NOK

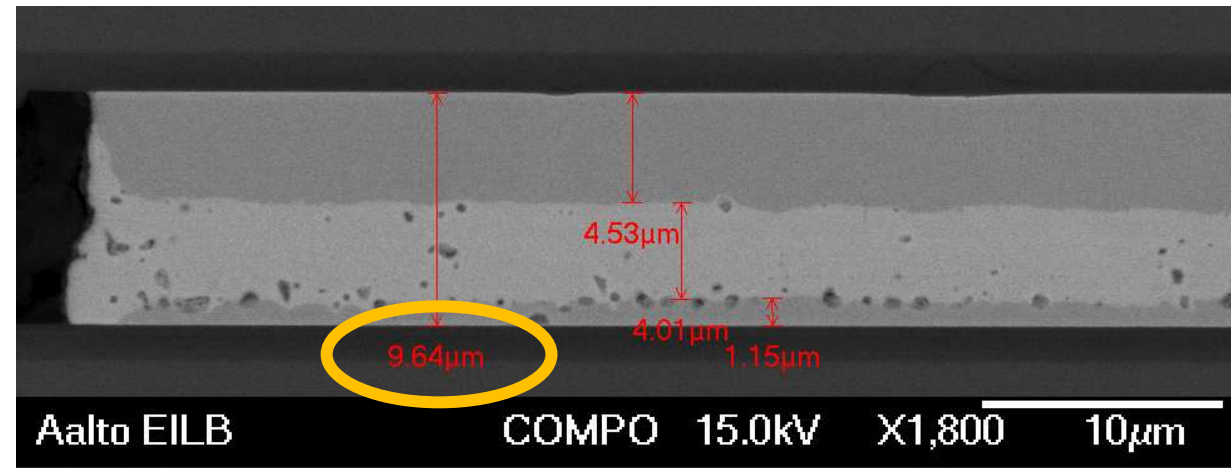
A!

Additional info:

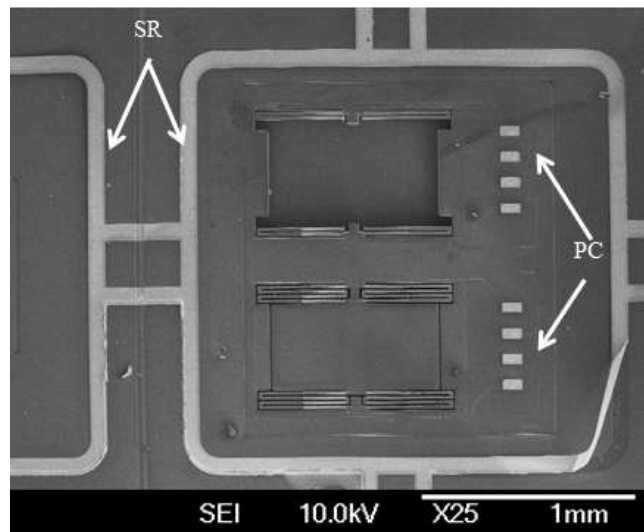


Design Challenges

Sealing ring

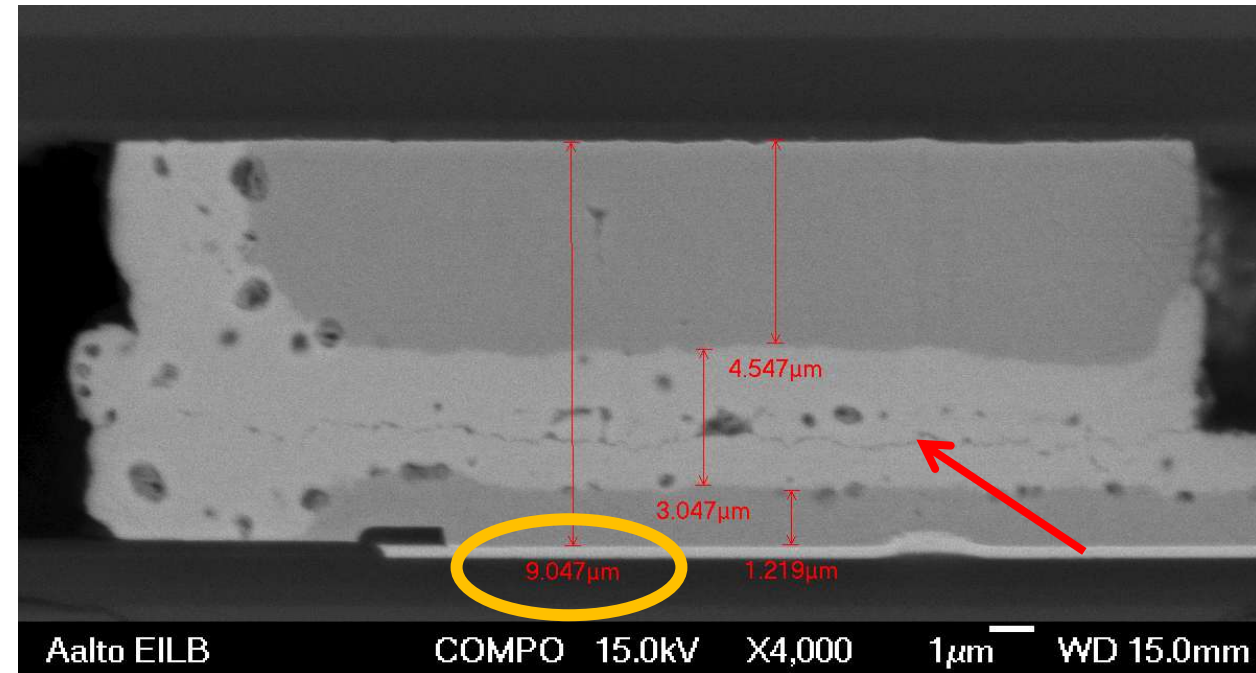


Bond height = ~9.6μm



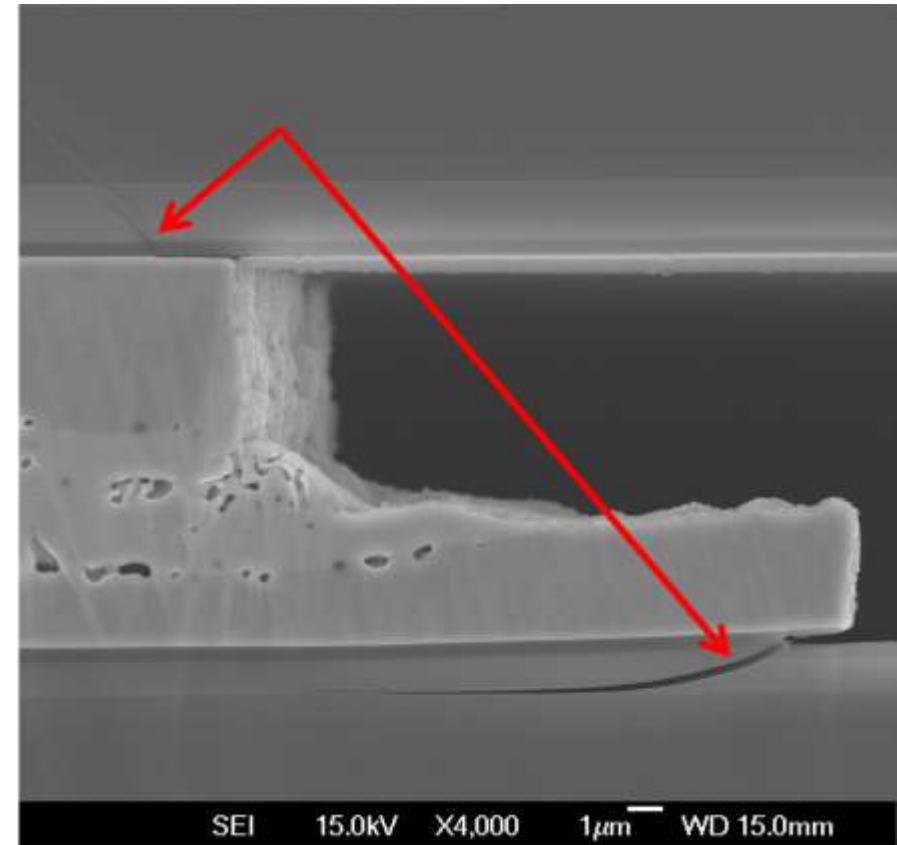
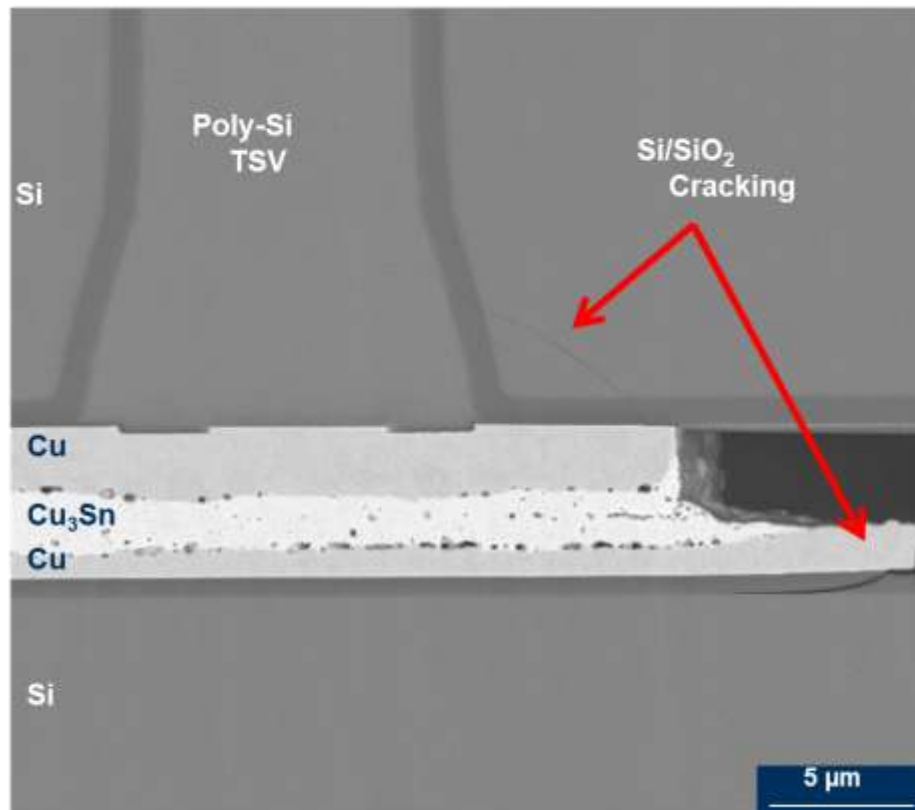
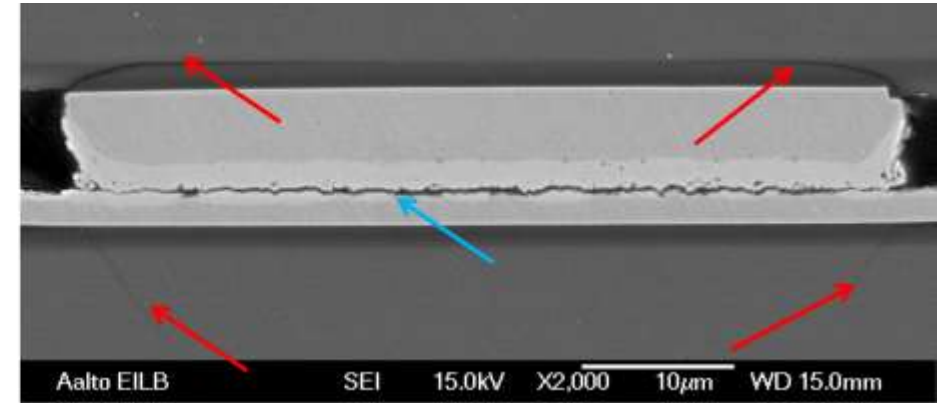
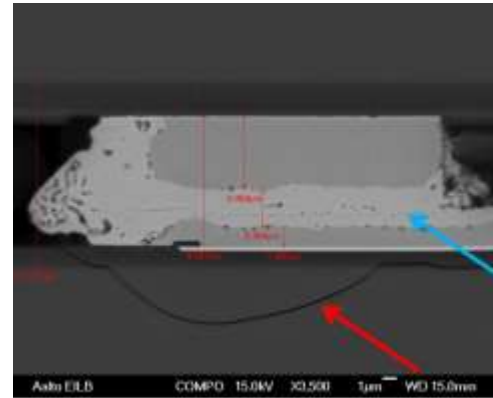
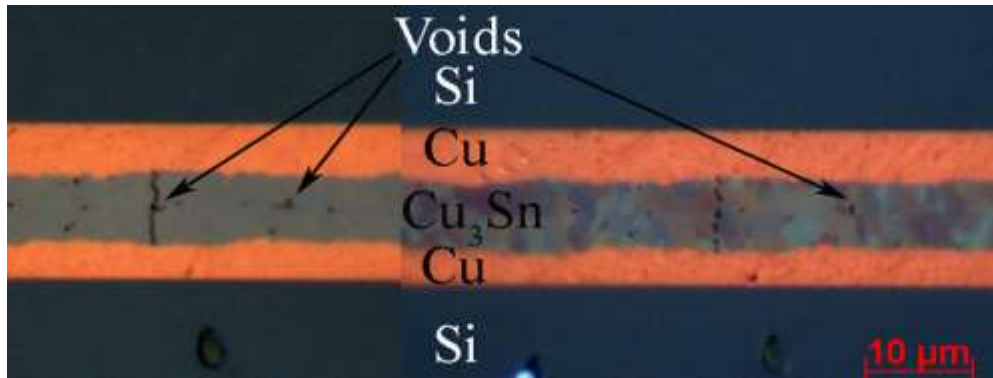
A!

Point contact



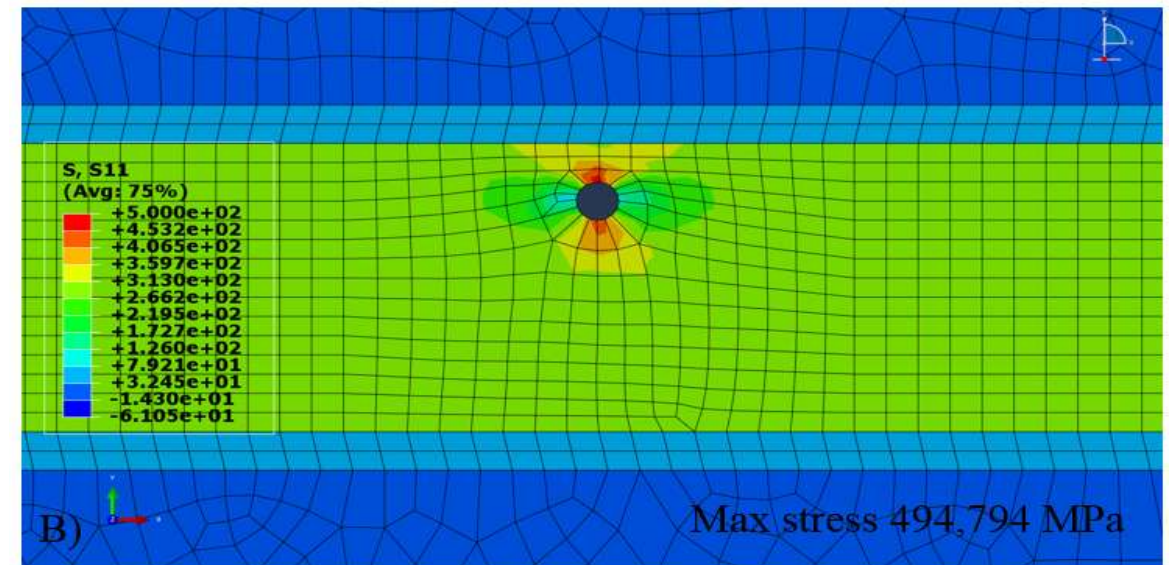
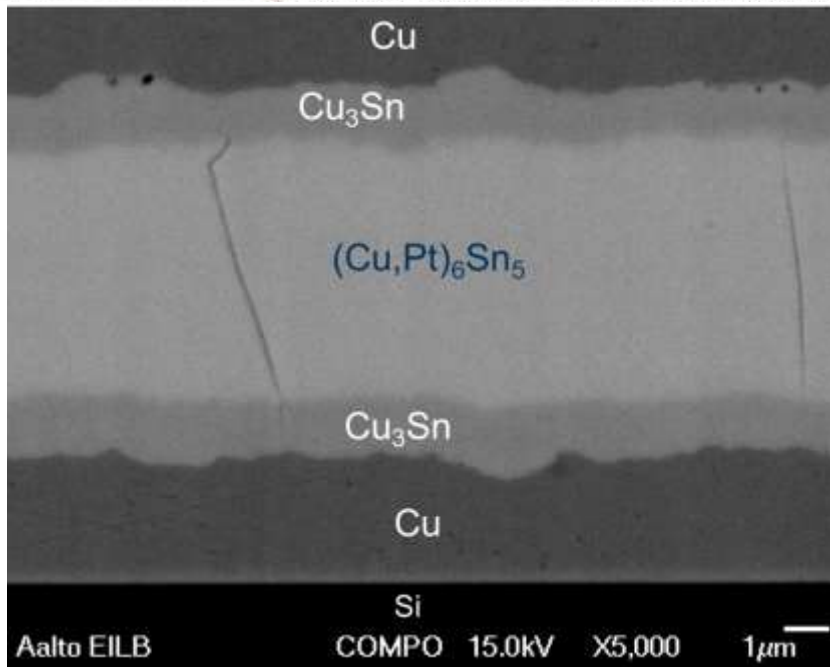
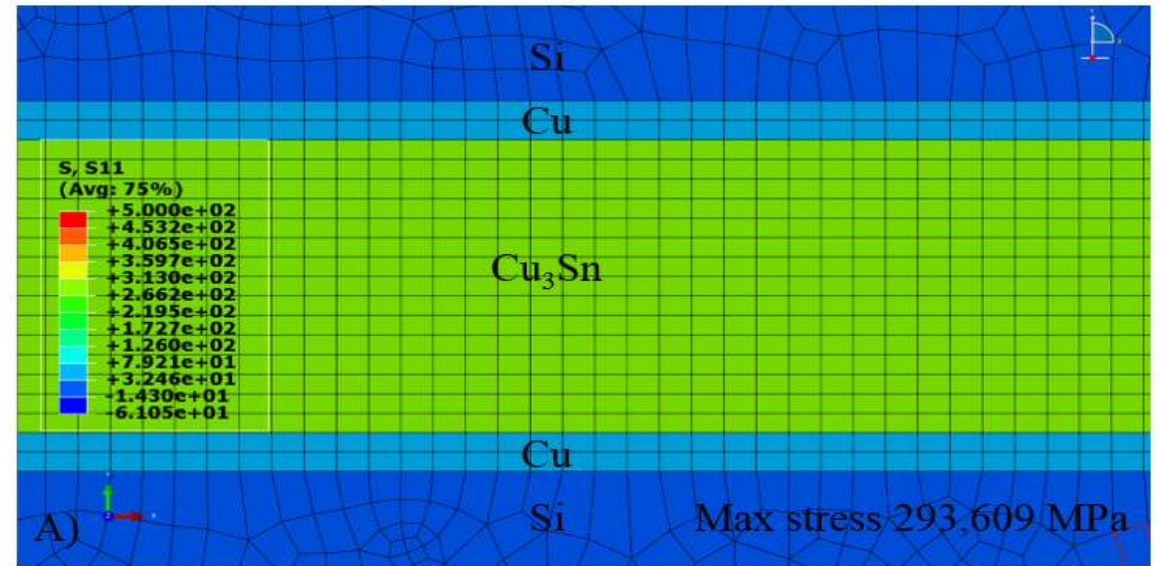
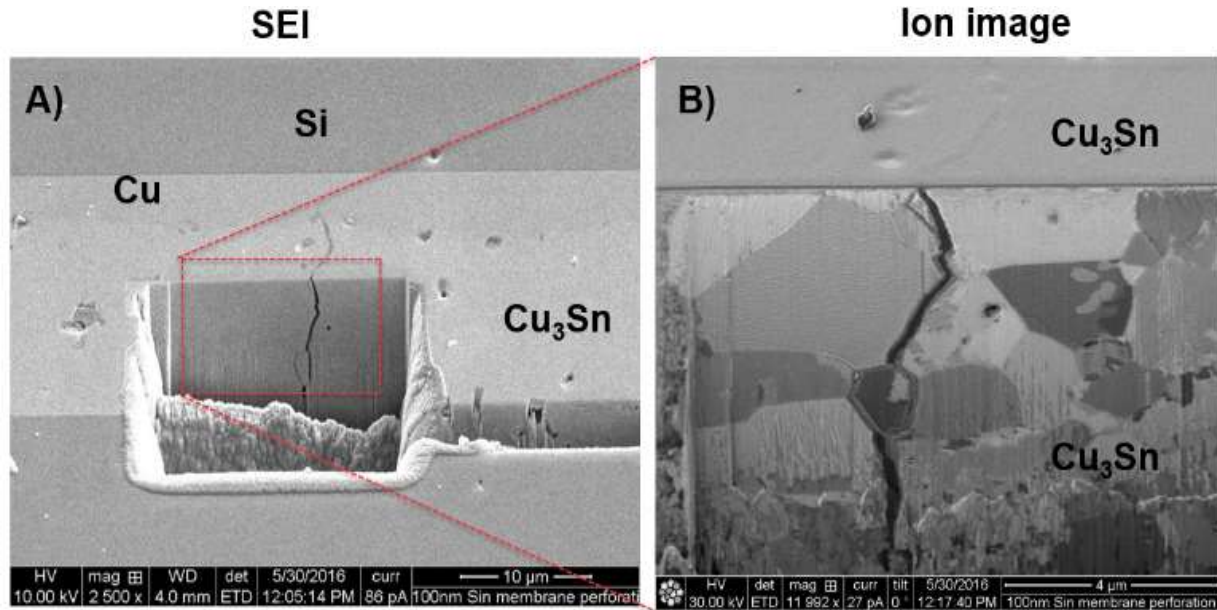
Bond height = ~9.0μm

Challenges – Stresses, Cracking & Voids



A!

Challenges - Vertical Cracking & Voids

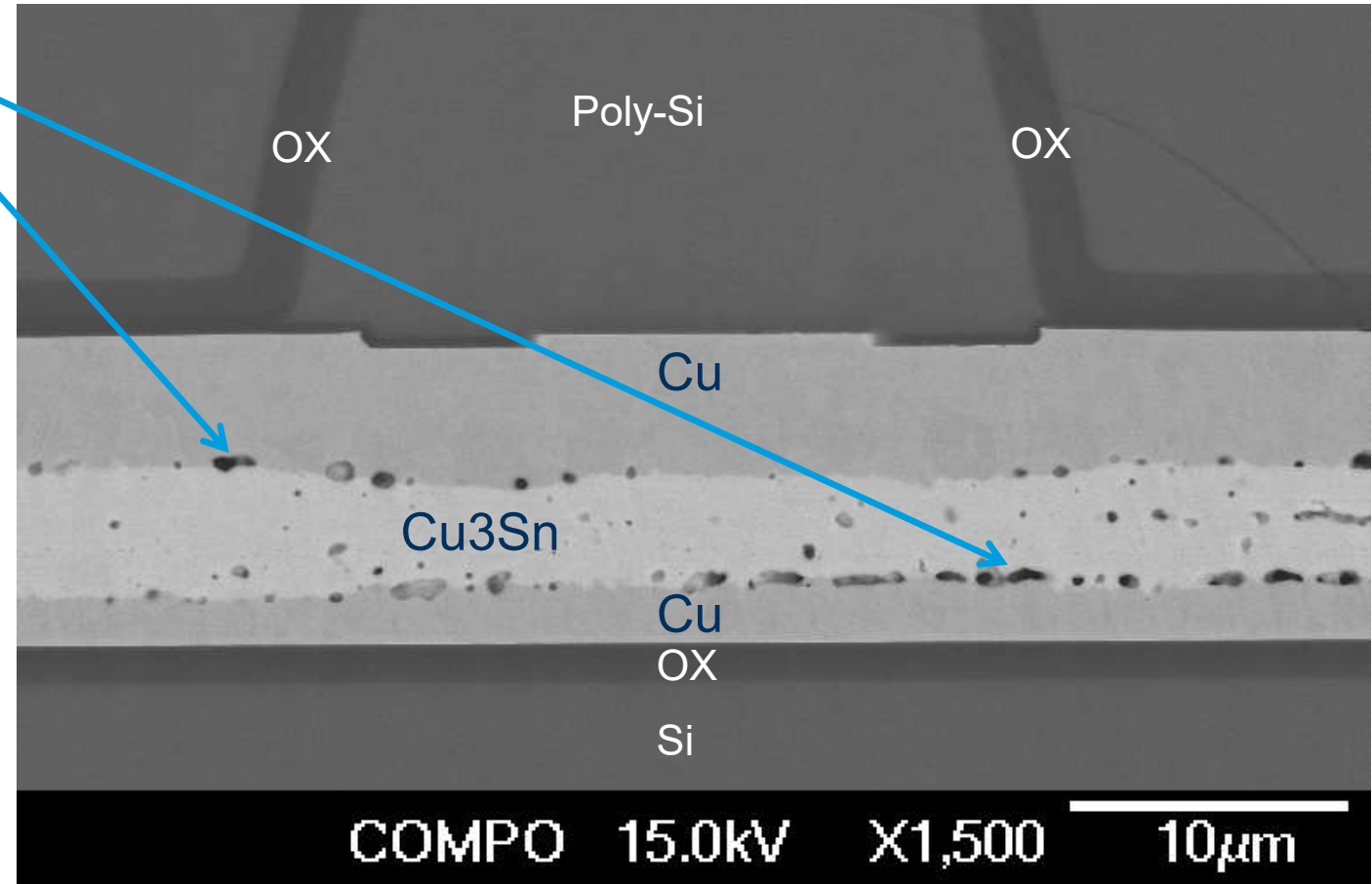
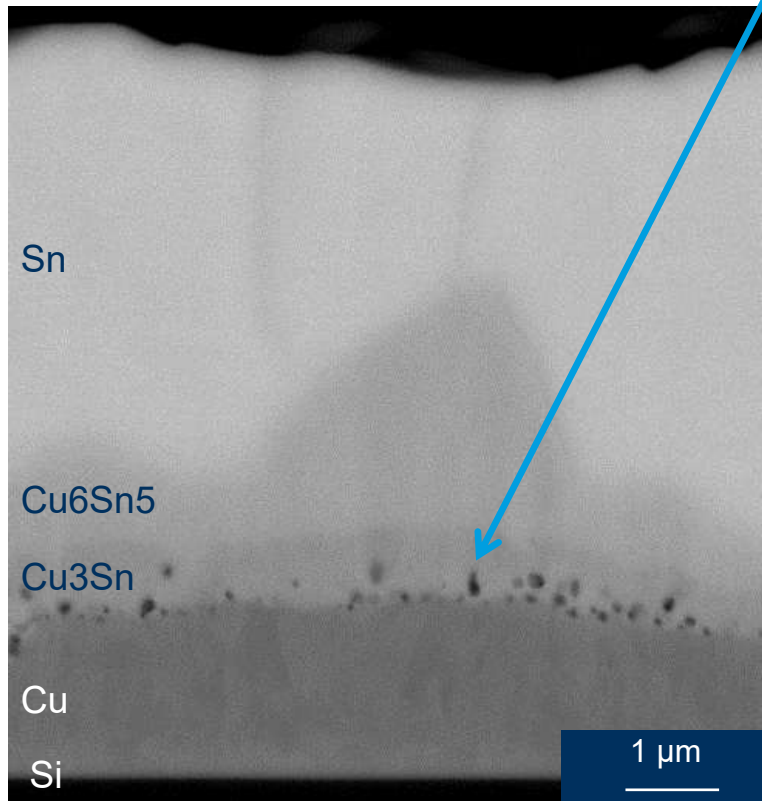


A!

Challenges - Intermetallic (IMC) void formation

Often referred to as “Kirkendall voids”

IMC voids



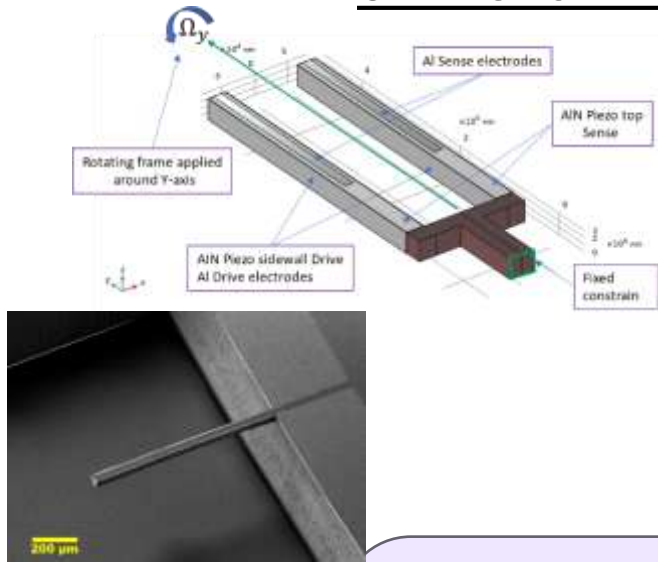
A!

Additional info:
Glenn.Ross@aalto.fi

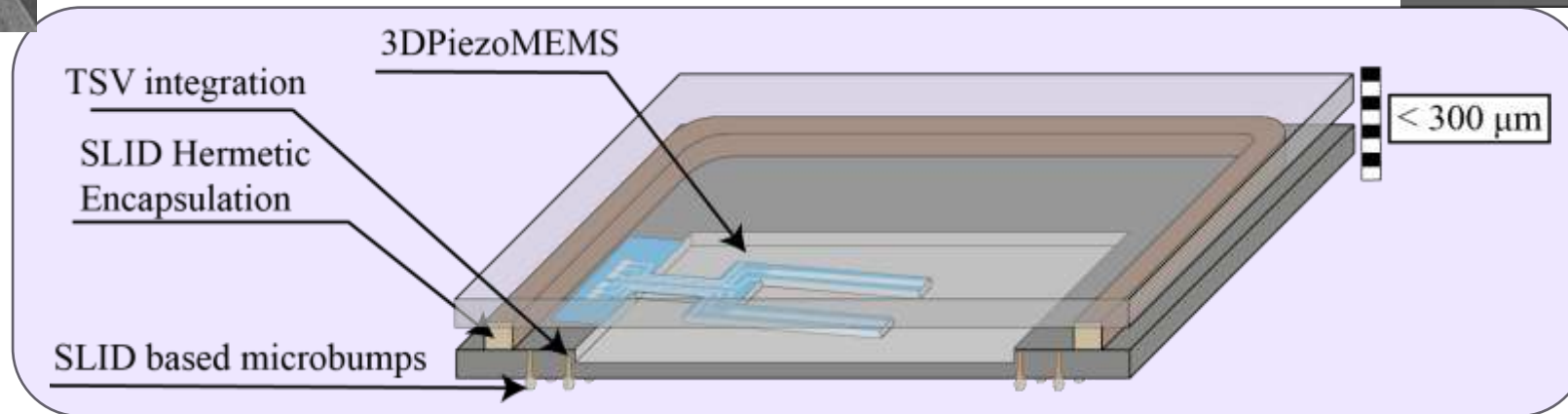
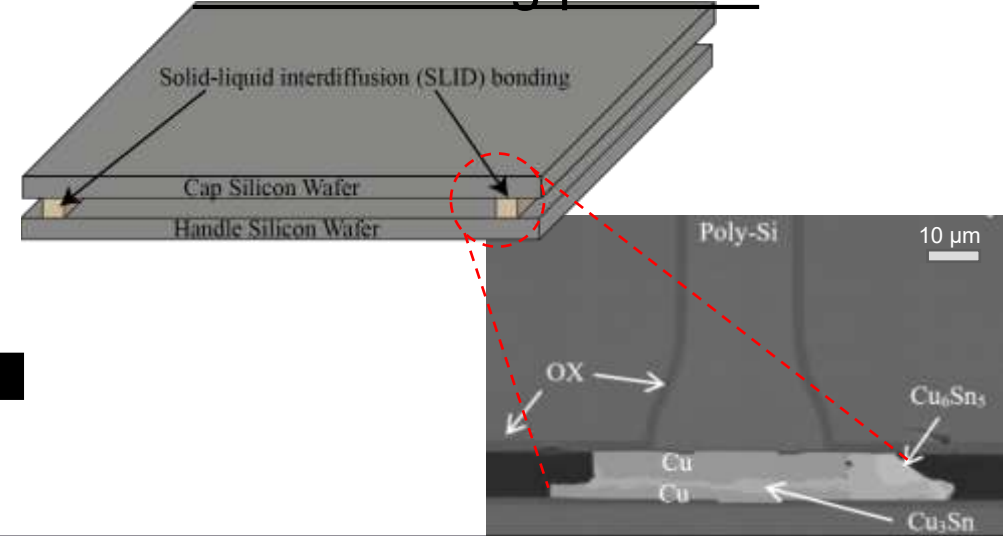
Current status

Objectives

3DPiezoMEMS platform



SLID bonding process

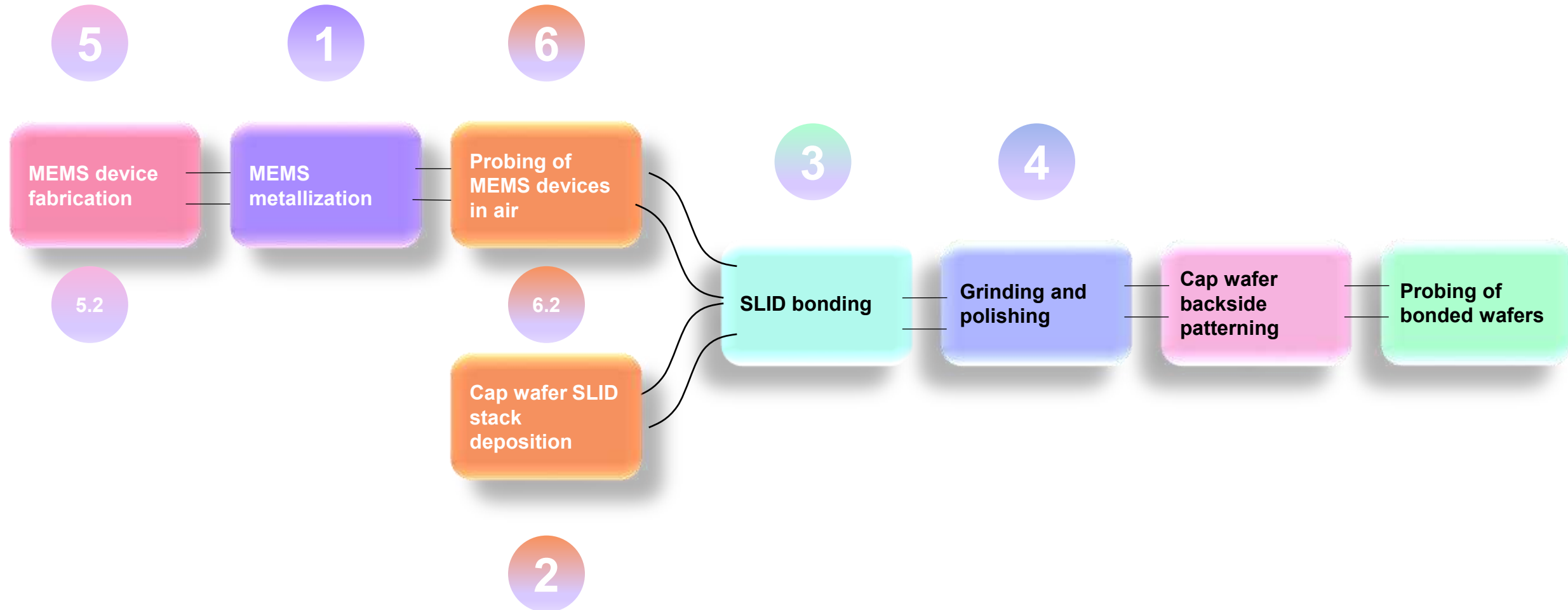


A!

To deploy AI-driven real-time edge sensor technology, we propose combining two separately, but meticulously researched technology platforms developed within the Electronics Integration and Reliability group at Aalto University.

Workflow

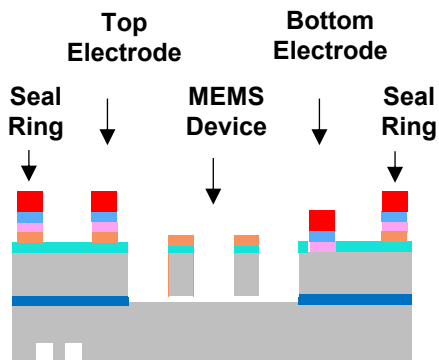
Process modules



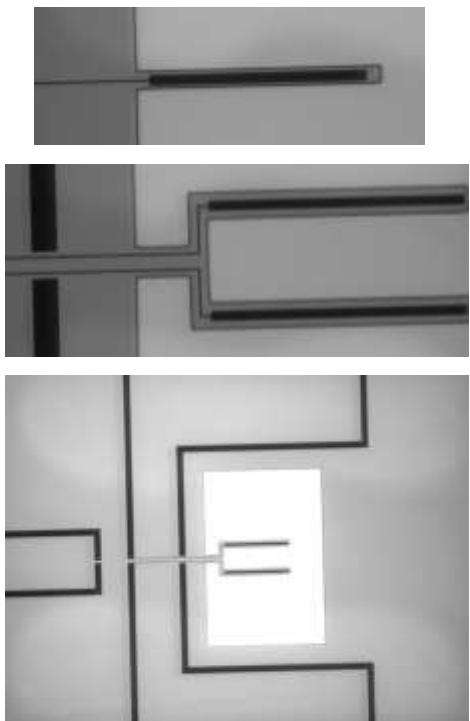
MEMS Fabrication

Design

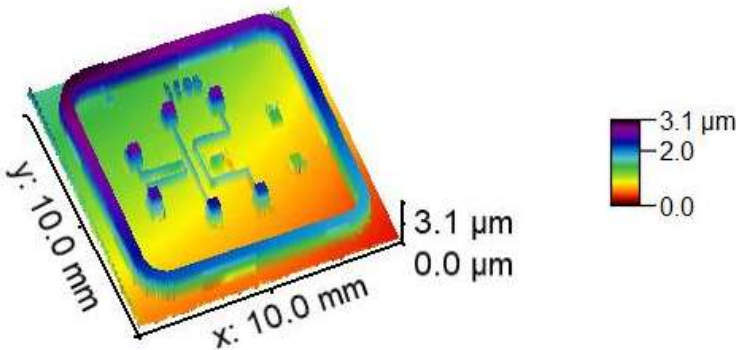
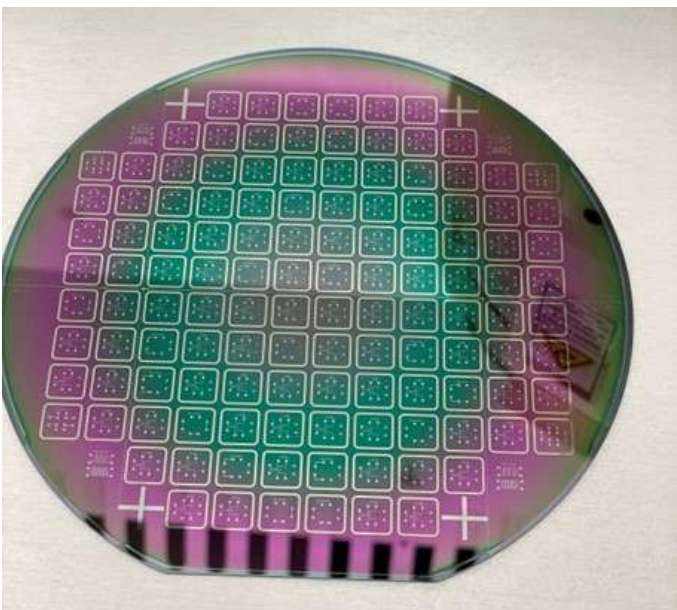
Sideview



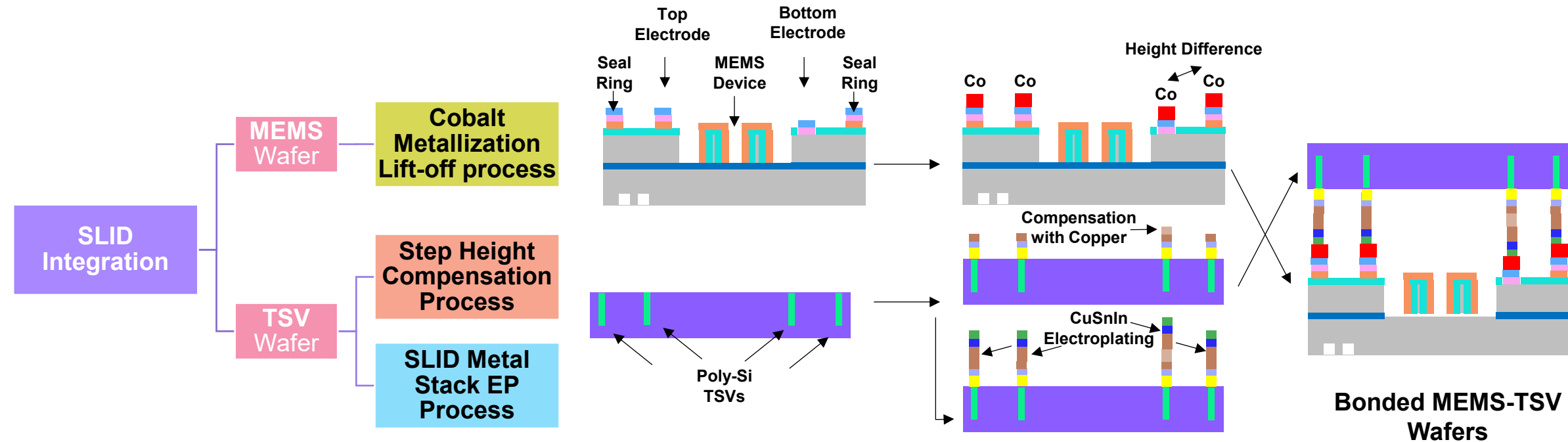
Released Device



Wafer



Process Development



A!

Aluminum

Aluminium Nitride

Titanium Tungsten

Molybdenum

Copper Seed

Aluminium

1um Copper Compensation

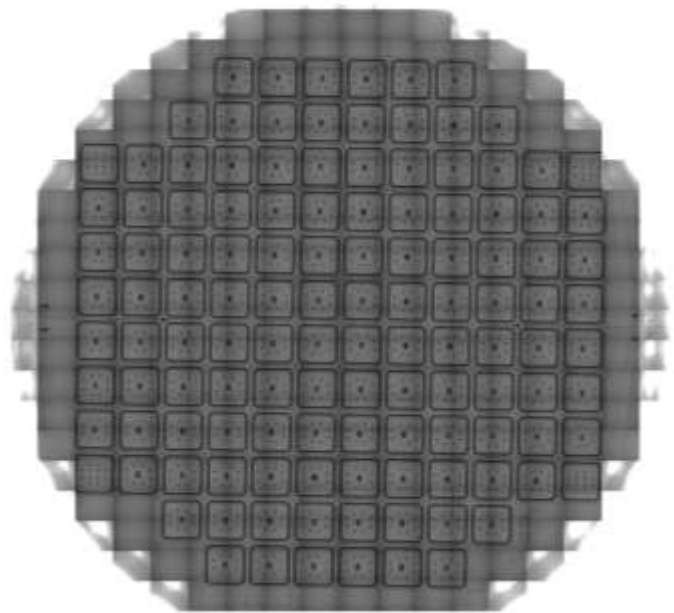
Titanium

Tin

Cobalt

Indium

IR Imaging Results



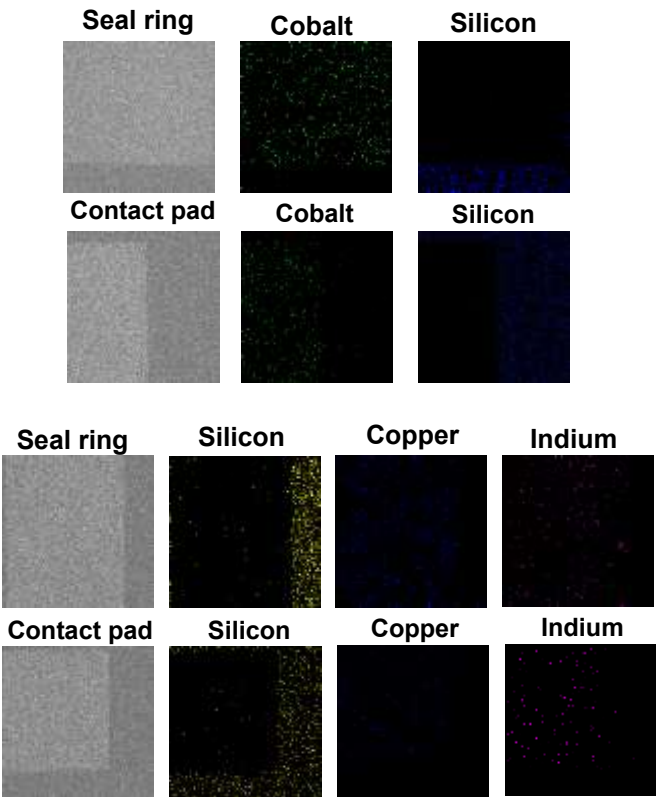
Bonded Sample#1: Had Indium over-etching Issue
(Detached during Dicing)

A!

Post EP, Indium over-etching during Aluminium layer etching

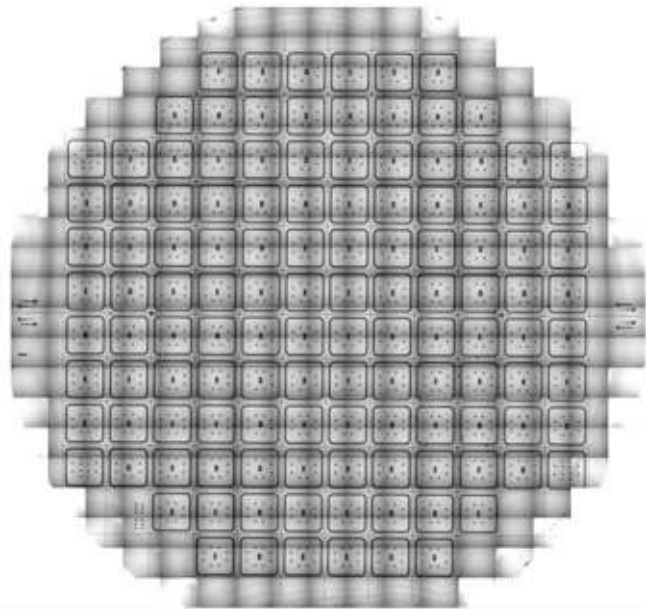
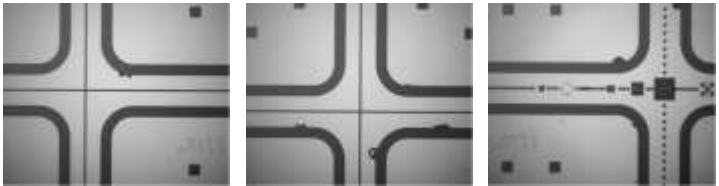


Bonding at 200C for 1 hr. at 20MPa



Possibly Cu-Sn IMC formed on the cap-side but no traces of Cobalt were found on the cap side. On the MEMS side, no traces of copper or tin, indium were observed

Squeeze out observed



Bonded Sample#2: Non-uniform Indium EP

Grinding and polishing

IR inspection

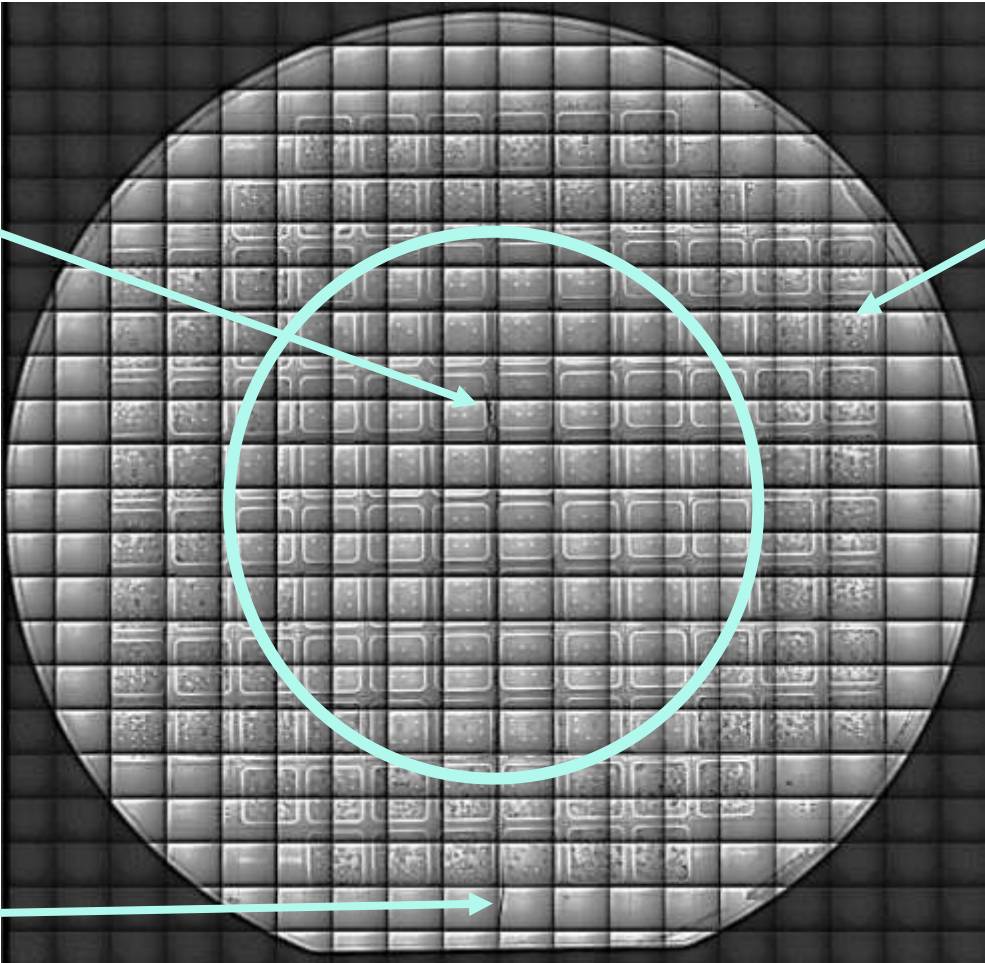
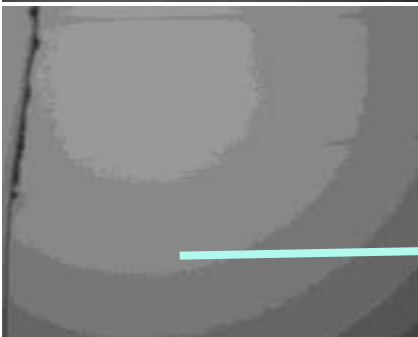
Major crack



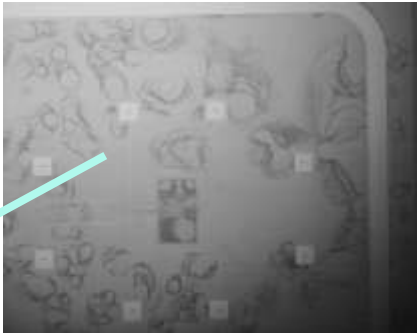
Small cracks



Major crack



Dies with stains



Clean dies



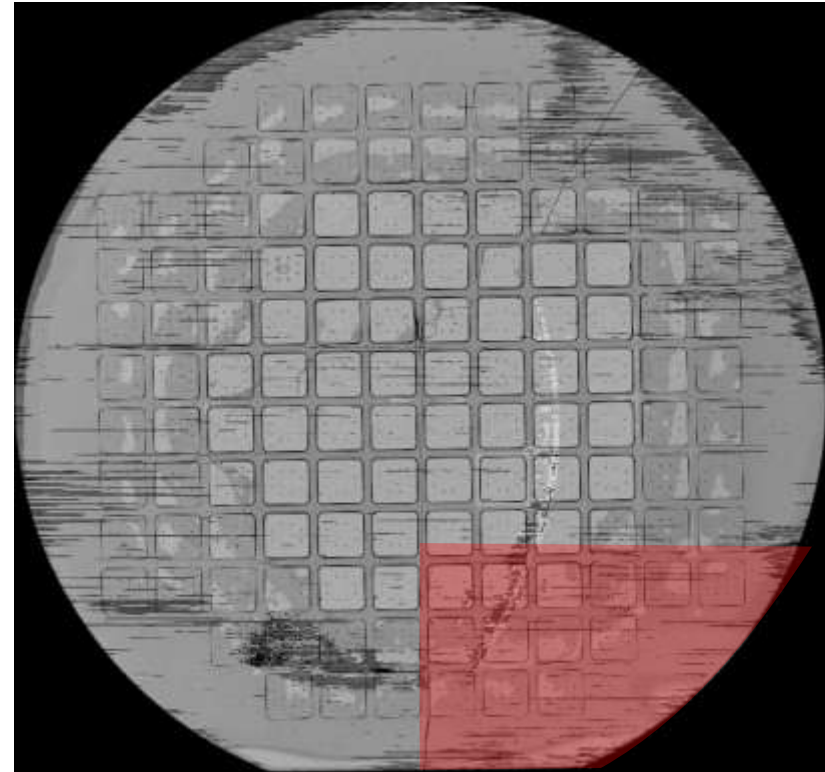
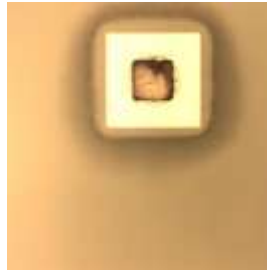
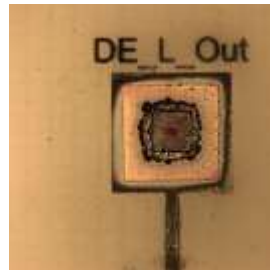
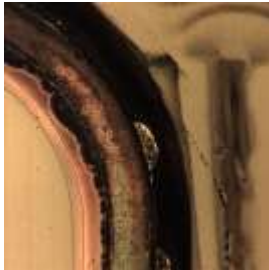
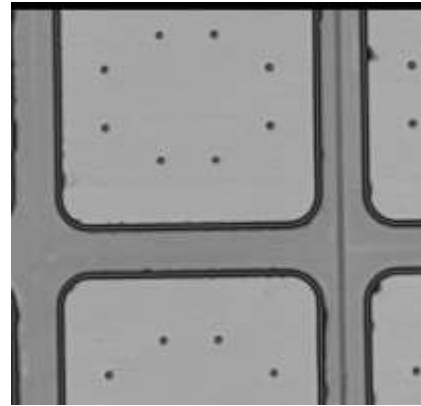
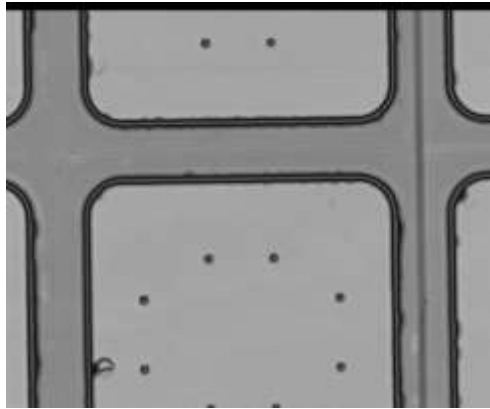
Clean dies



A!

Grinding and polishing

SAM inspection



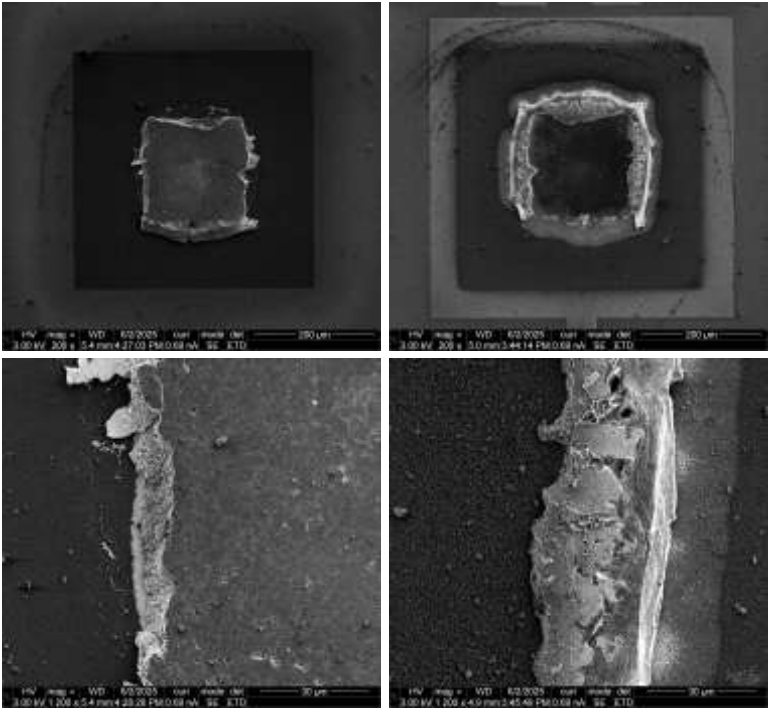
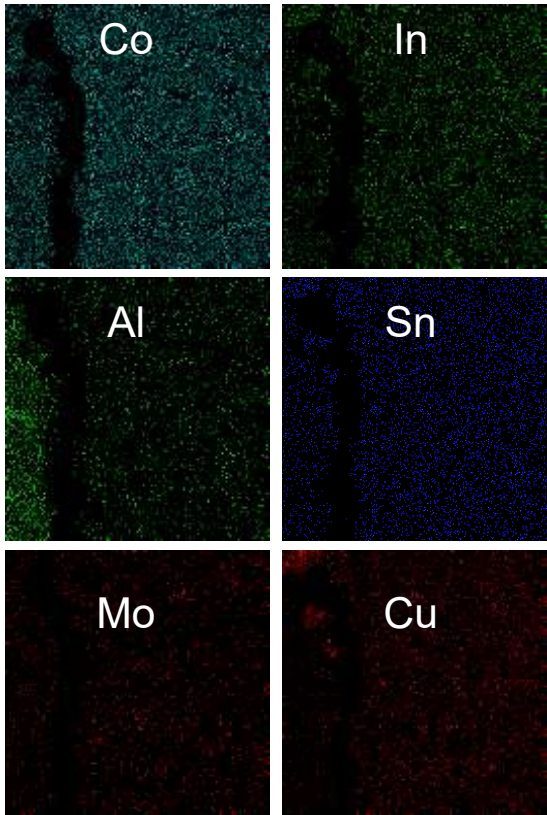
44/124 survived (35%)

A!

Grinding and polishing

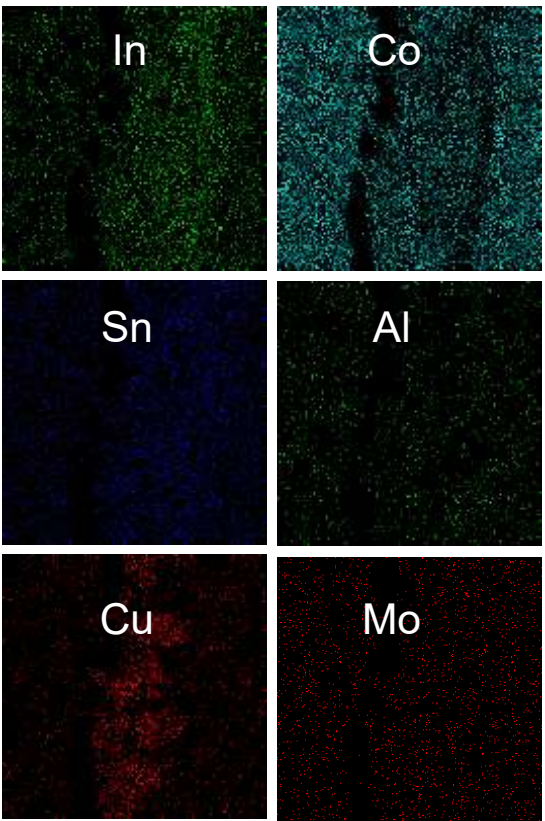
Optical inspection of detached samples

Top Electrode: EDX



CAP

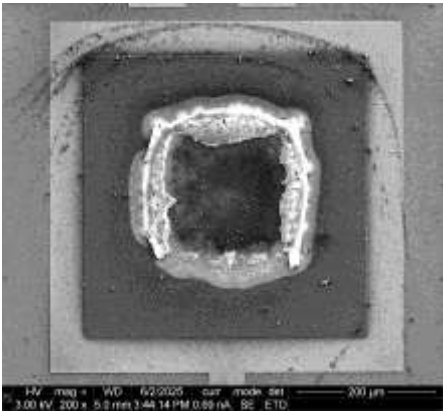
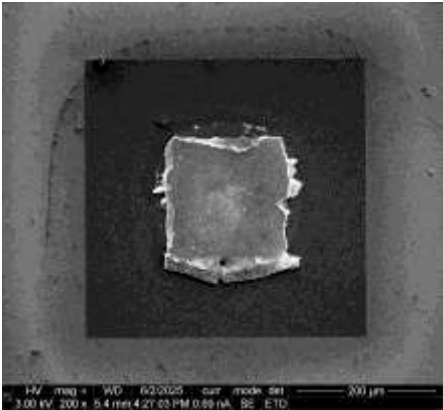
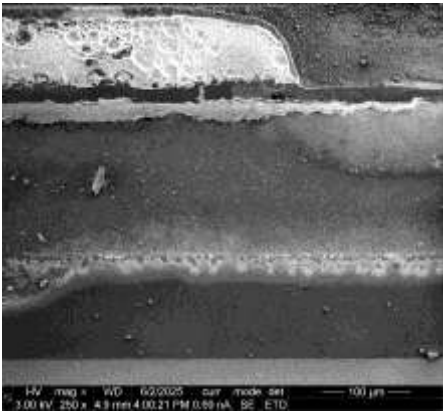
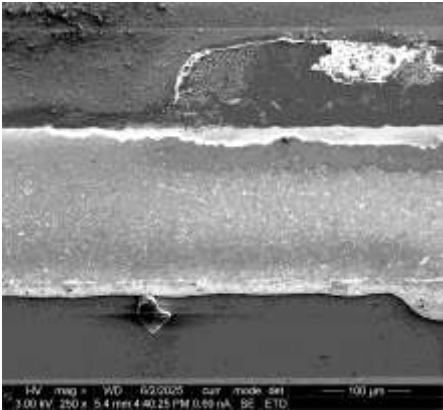
MEMS



A!

Grinding and polishing

Cross sectioning



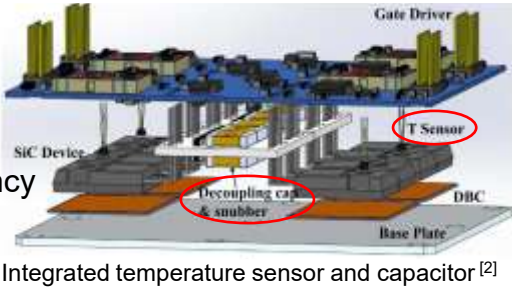
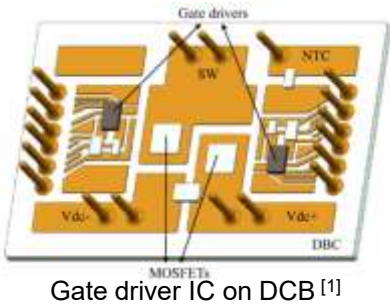
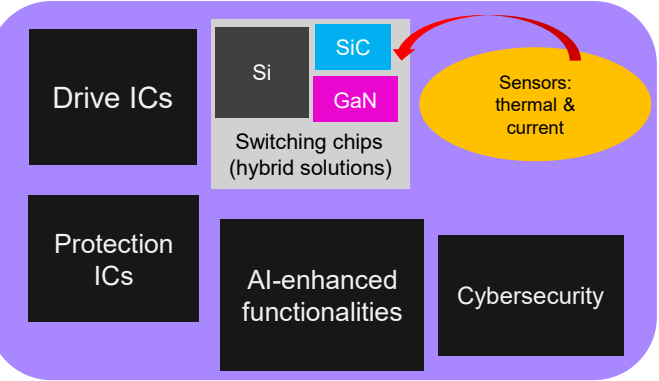
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SLID for Power Electronics

Higher integration and higher performance interconnection technologies in power electronics

Integrated Power Module (Power Chiplet)



Main motivations

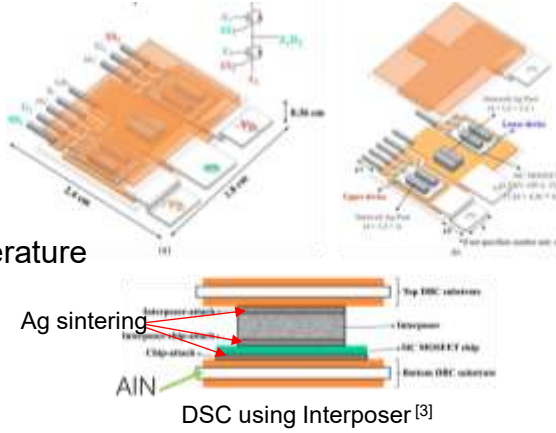
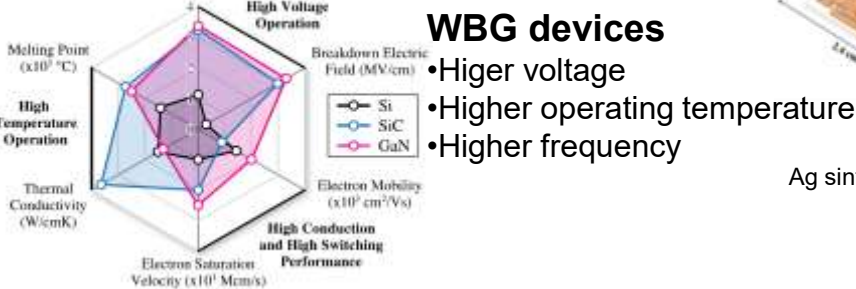
- Reduce the size of the overall system
- Reduced Parasitic Parameters
- Improve switching performance and efficiency

Higher power density
Enhanced reliability

A!

[1] L. Zhang, P. Liu, A. Q. Huang, S. Guo and R. Yu, "An improved SiC MOSFET-gate driver integrated power module with ultra low stray inductances," 2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Albuquerque, NM, USA, 2017, pp. 342-345, doi: 10.1109/WiPDA.2017.8170570
[2] Z. Chen and A. Q. Huang, "High Performance SiC Power Module Based on Repackaging of Discrete SiC Devices," in IEEE Transactions on Power Electronics, vol. 38, no. 8, pp. 9306-9310, Aug. 2023

Interconnection technologies



Wire bonding frontside interconnection

- High loop inductance
- Wirebond lift-off



Double side cooling (DSC)

- Better heat dissipation
- Lower inductance
- Compact design

Conventional solder

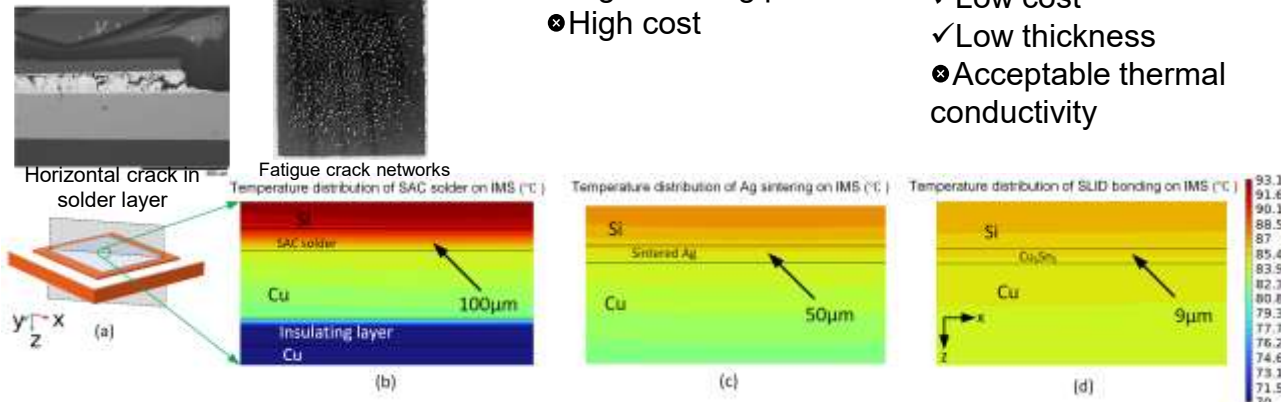
- Low melting point, 217;
- Module operating temperature <175°C
- Poor thermomechanical reliability

Ag sintering

- ✓High melting point
- ✓High thermal conductivity
- ✗High bonding pressure
- ✗High cost

SLID bonding

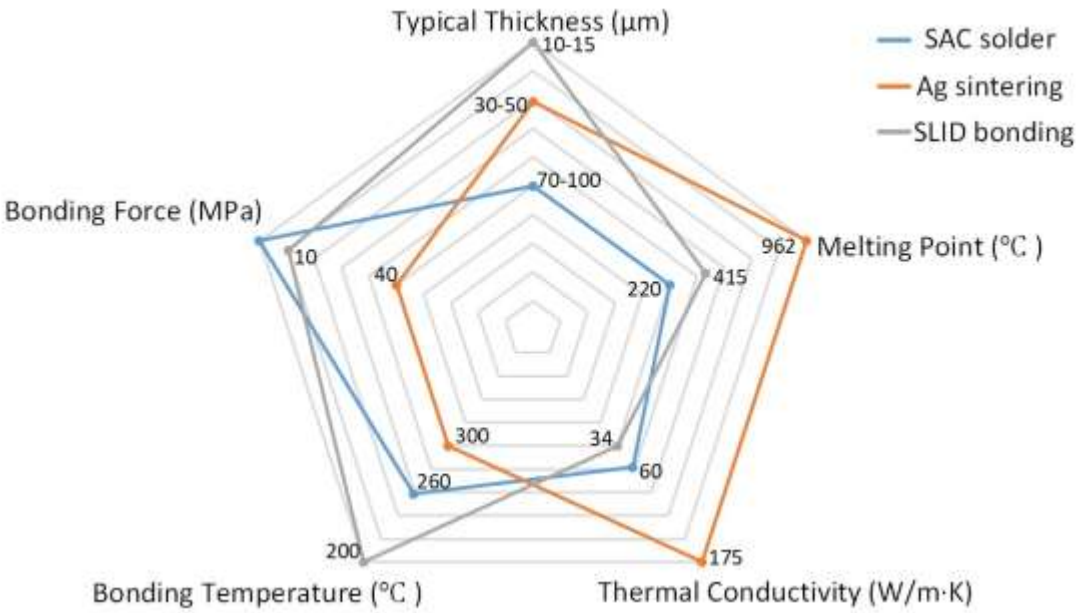
- ✓High melting point
- ✓Moderate bonding pressure
- ✓Low cost
- ✓Low thickness
- ✗Acceptable thermal conductivity



[3] C. Ding, et al., "A Double-Side Cooled SiC MOSFET Power Module With Sintered-Silver Interposers: I-Design, Simulation, Fabrication, and Performance Characterization," in IEEE Transactions on Power Electronics, vol. 36, no. 10, pp. 11672-11680, Oct. 2021

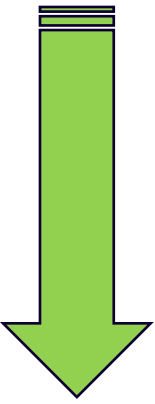
Motivation

- Different die-attach methods



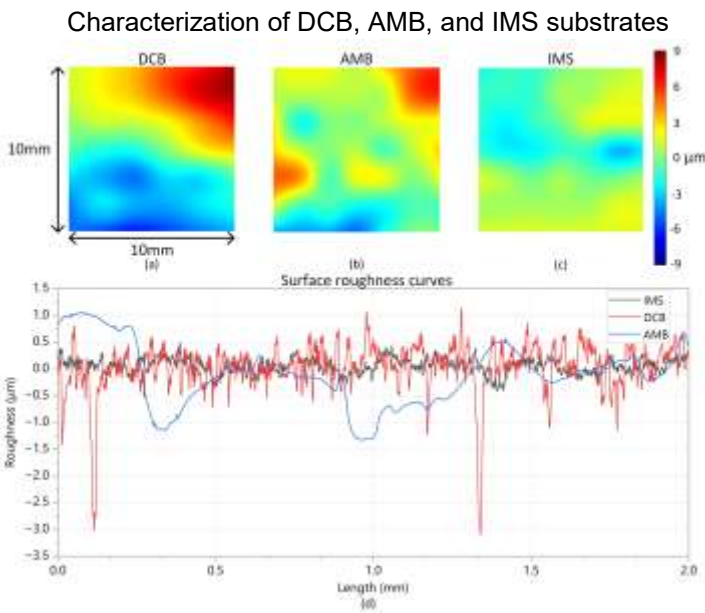
- SLID bonding

- Bonding temperature < ~200°C
- High melting point
- High mechanical strength
- Reduced thickness
- Low bonding force



Thermal performance?
Reliability?

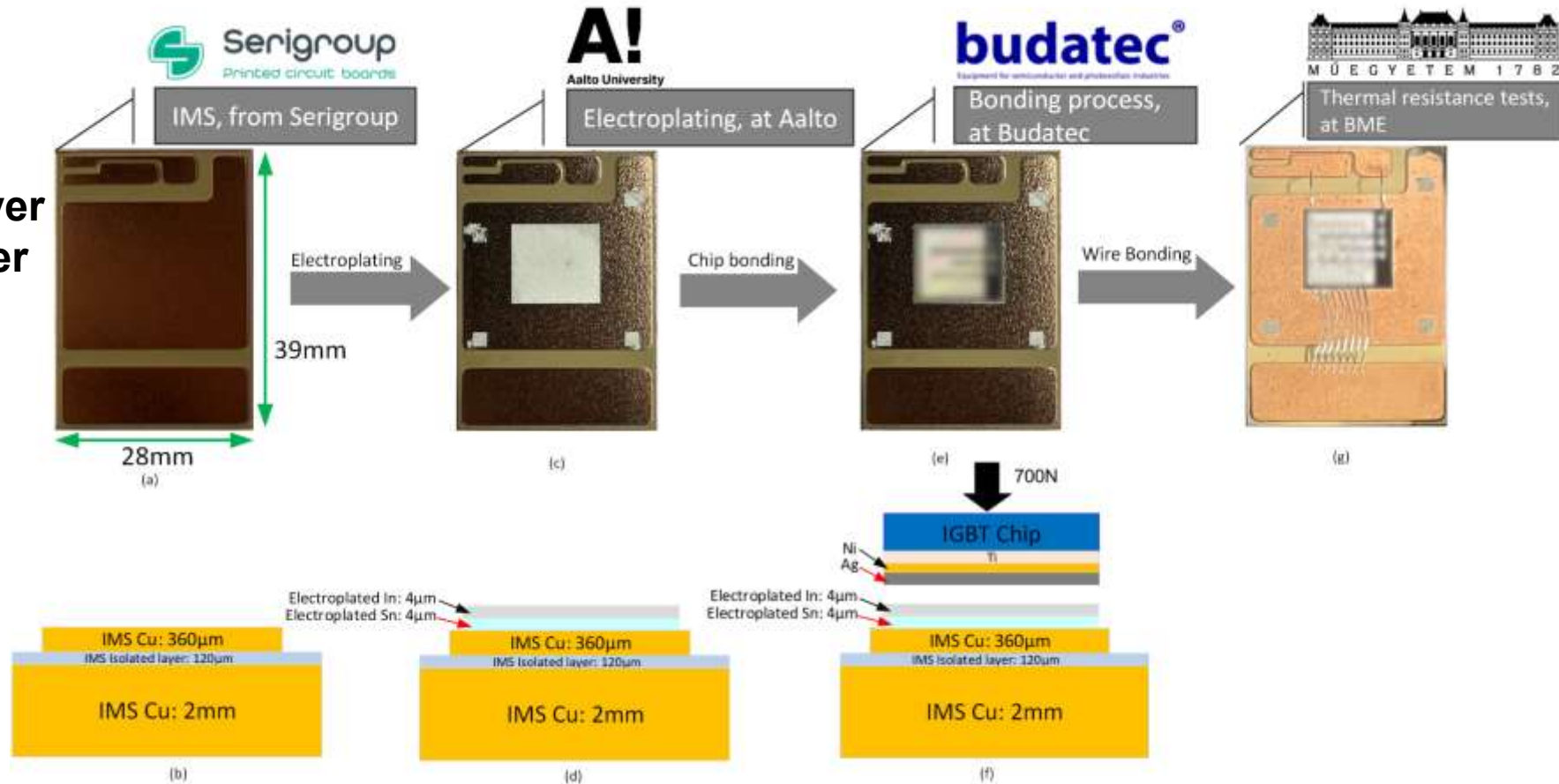
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Conventional DCB and AMB substrates typically exhibit relatively high warpage and surface roughness

Bonding process

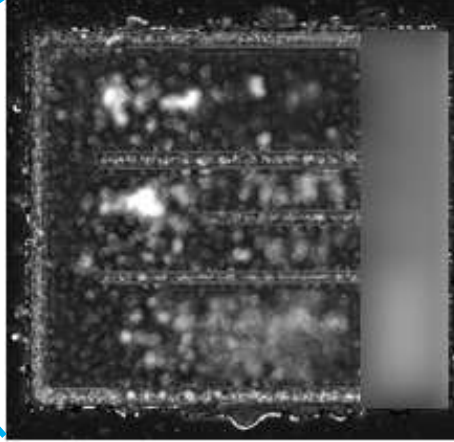
- IGBT chip:
 - Size: $11.2 \times 12.5 \text{ mm}^2$
 - Thickness: $118 \text{ }\mu\text{m}$
- IMS substrate preparation:
 - **$4\text{ }\mu\text{m}$ Sn electroplating layer**
 - **$4\text{ }\mu\text{m}$ In electroplating layer**
- Bonding temperature & time:
 - **200°C : 2h**
 - **170°C : 5h**
- Bonding pressure: **5MPa**



S. Liu et.al, Thermal Characterization of SLID Bonding Die-Attach in IGBT Module Packaging Application, PCIM Conference 2026, 9 – 11 June 2026, Nuremberg

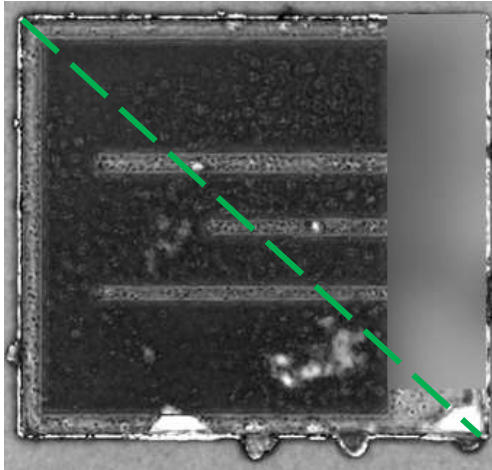
SAM results

200°C, 2h Average Bonded area percentage: ~92%



Bonded area percentage: ~91.2%
 $R_{th,jc}$: 0.180 K/W

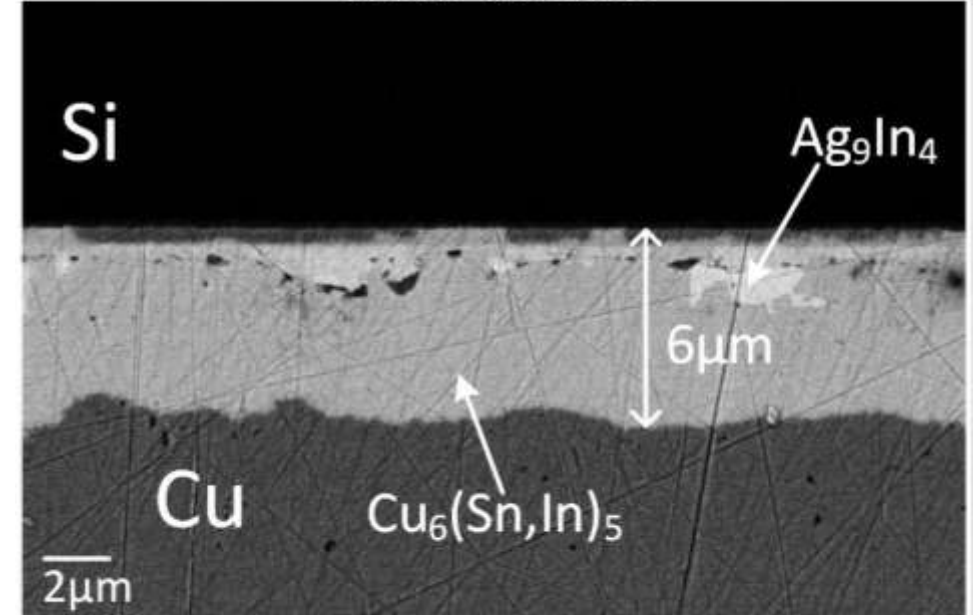
170 °C, 5h Average Bonded area percentage: ~96%



Bonded area percentage: ~97%
 $R_{th,jc}$: 0.174 K/W

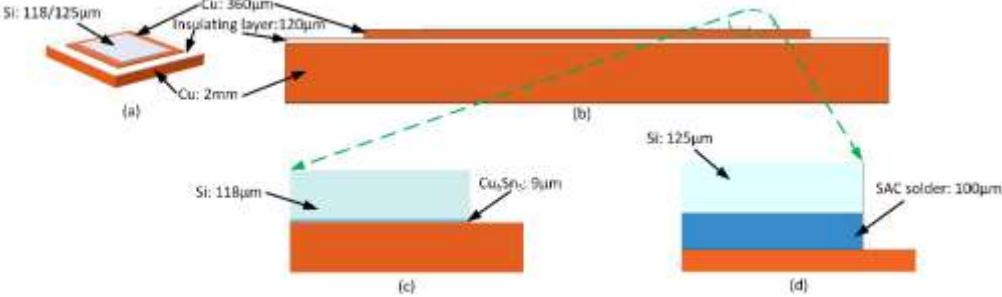
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Cross-section



- The thickness of the die-attach layer: ~6 µm
- Main IMC phase: $\text{Cu}_6(\text{Sn},\text{In})_5$

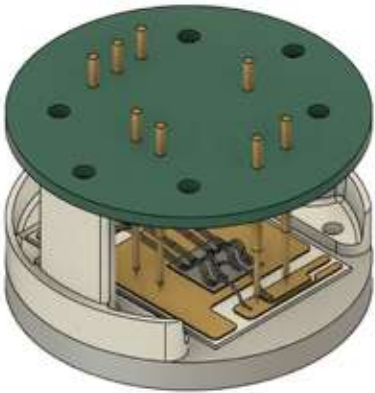
FE Simulation & thermal characterization



Schematic of FE models

Dimensions of different model layers

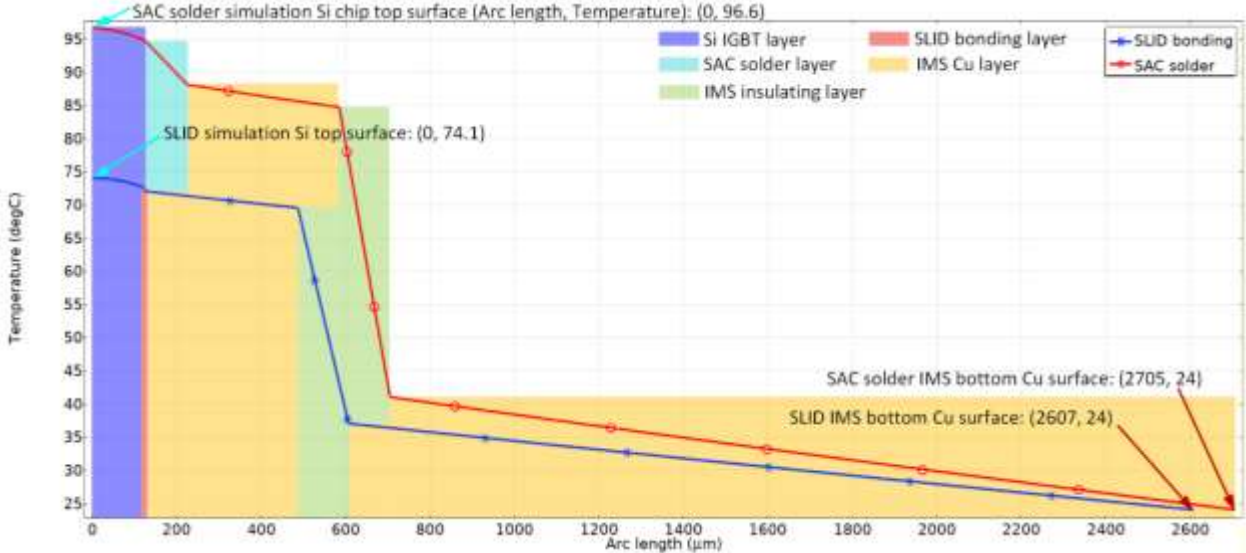
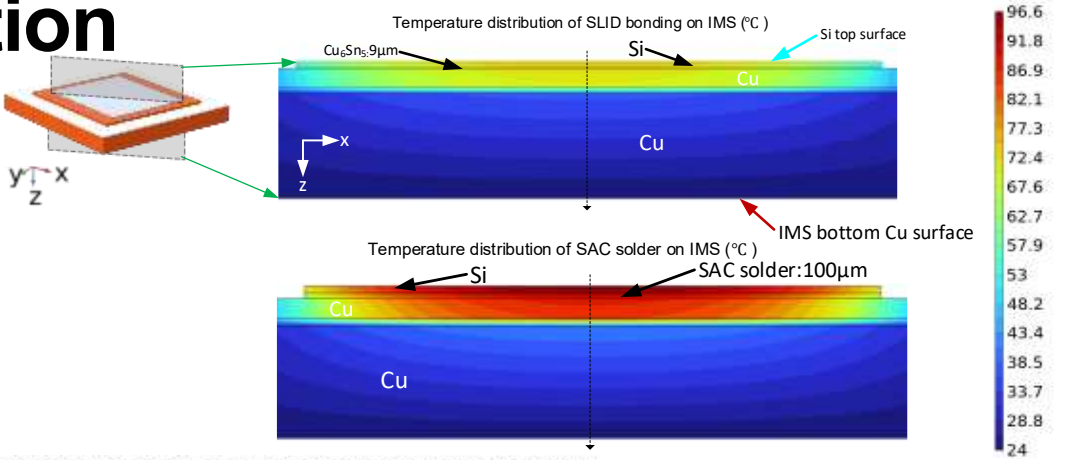
Domains	Dimension (mm ³)
Si chip in SLID-IMS	11.2 × 12.5 × 0.118
Si chip in SAC solder-IMS	9.73 × 10.23 × 0.125
Cu ₆ Sn ₅ layer	11.2 × 12.5 × 0.009
SAC solder layer	9.73 × 10.23 × 0.1
top IMS Cu layer	15 × 15 × 0.36
IMS insulating layer	20 × 20 × 0.12
bottom IMS Cu layer	20 × 20 × 2



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Experimental thermal measurements

JEDEC JESD 51-14 method



$R_{th,jc}$ values obtained from FE simulation and thermal resistance measurements

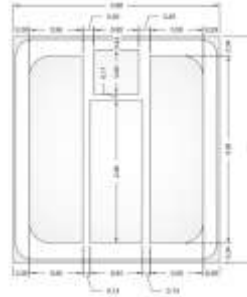
$R_{th,jc}$ value	SAC solder-IMS	SLID-IMS	$\Delta R_{th,jc}$
FE simulation (K/W)	0.182	0.125	0.057
Thermal resistance measurements (K/W)	0.232	0.179	0.053

- Compared to SAC soldering, the SLID bonding method reduces the $R_{th,jc}$ by **22.8%**

Double-sided cooled (DSC) demonstrator

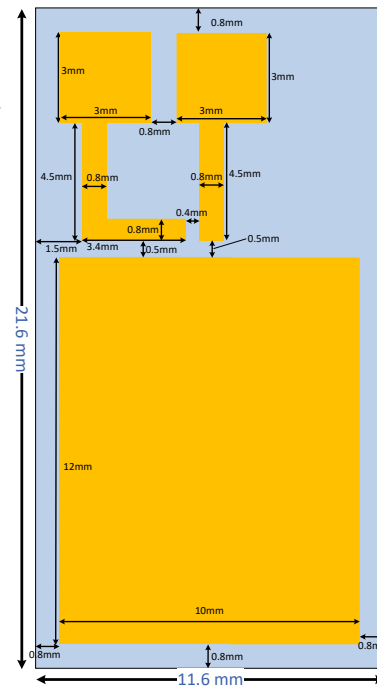
➤ SiC MOSFET bare dies bonding on IMS substrates

- Wolfspeed, CPM4-0120-0104JS0A
- Die size: 3.68*4.06mm²
- Backside metallization: Au
- Substrate: Electroplating Sn and In layer, 4+4μm



➤ Front side interconnection

- Double side cooling:
 - ◆ front side re-metallization
 - ◆ Top IMS circuit design
- Double-side bonding



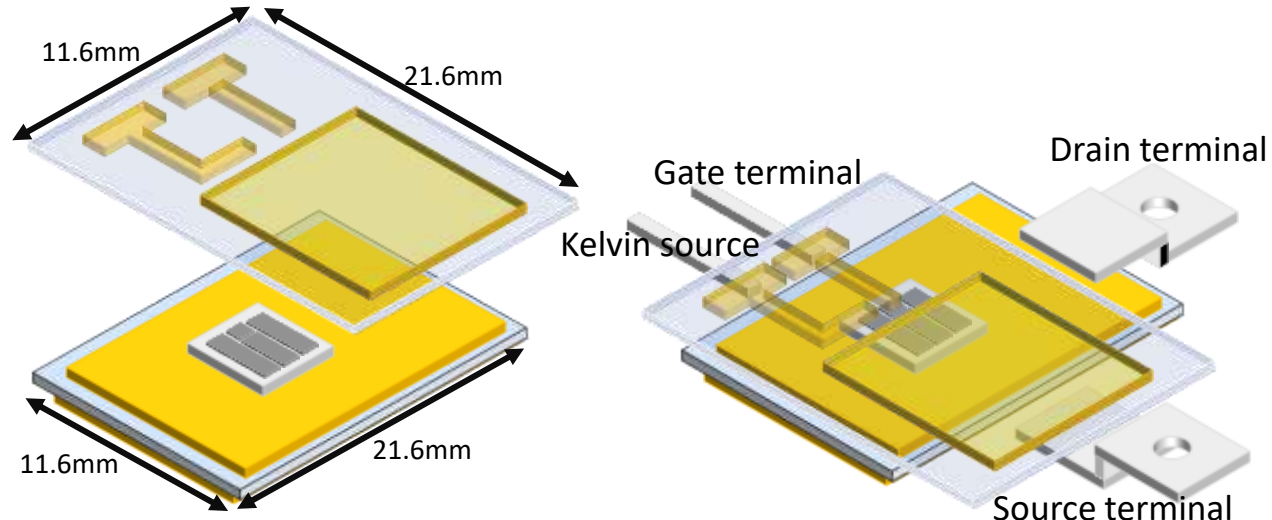
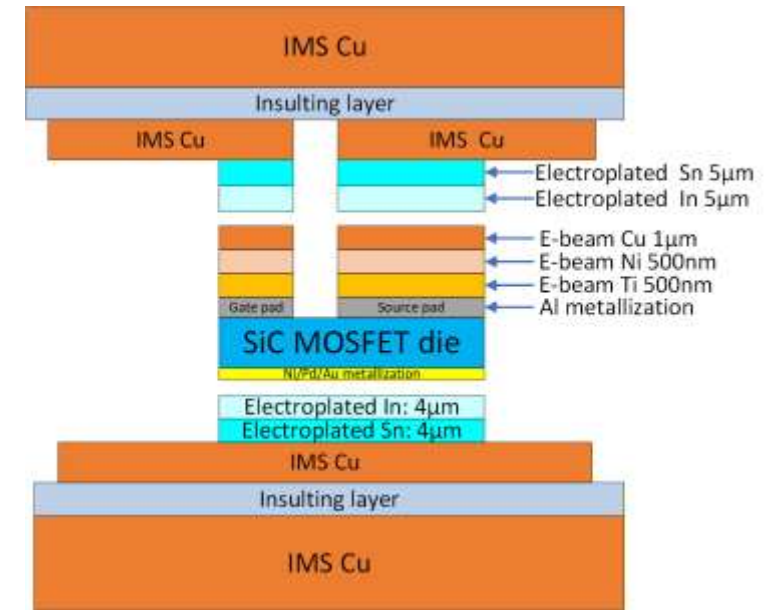
➤ Simulation:

- Thermal resistance
- PCT

➤ Electrical characterization

- ON-state resistance, leakage current, I-V output characteristics

➤ Reliability testing TBD



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Double-sided cooled (DSC) demonstrator

DSC-SiC-SLID results

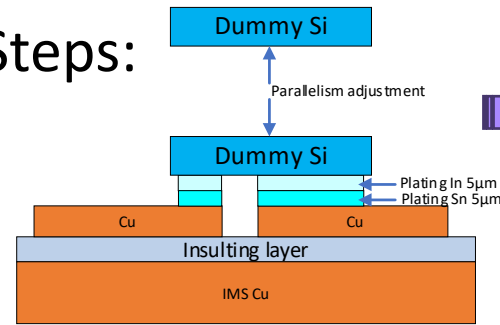
double-side boning test

two-step bonding

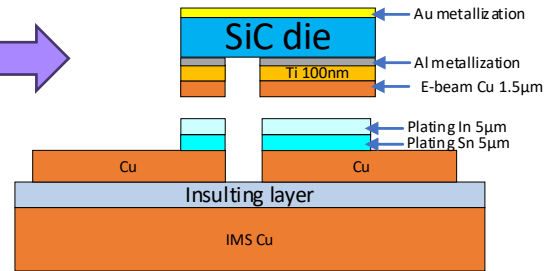
Bonding condition:

- front side: 5+5 μm
- back side: 4+4 μm
- temperature: 185°C

Steps:

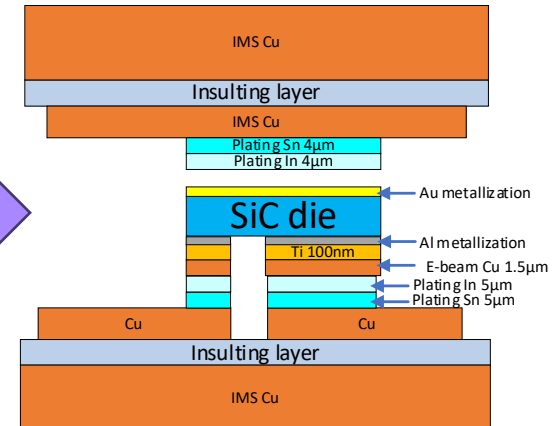


Parallelism adjustment



Chip front-side and top IMS bonding

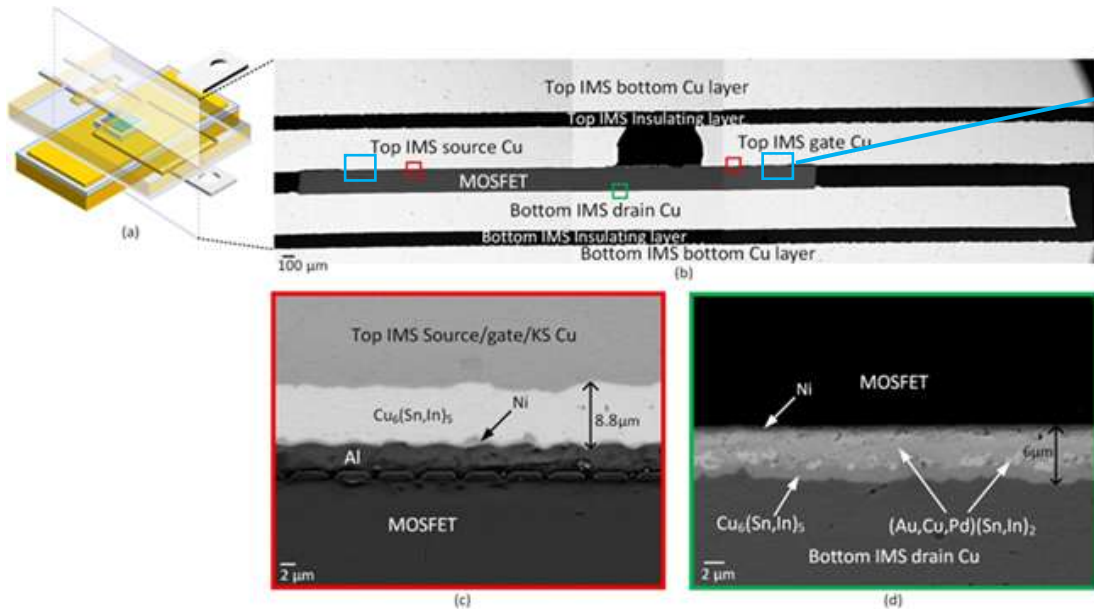
- pressure: front: 14.6MPa;
- Time: 0.5h



Chip back-side and bottom IMS bonding

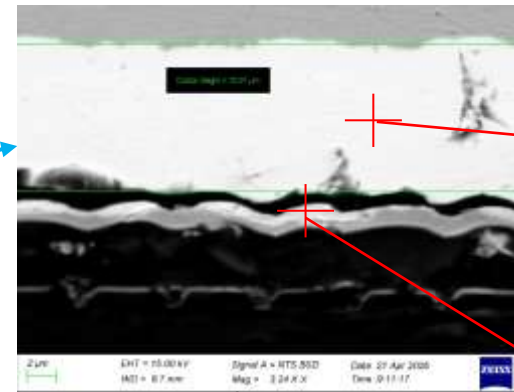
- Pressure: back: 7MPa
- Time: 2.5h

Cross-sectional results

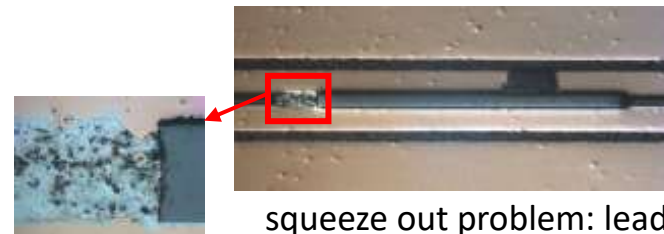
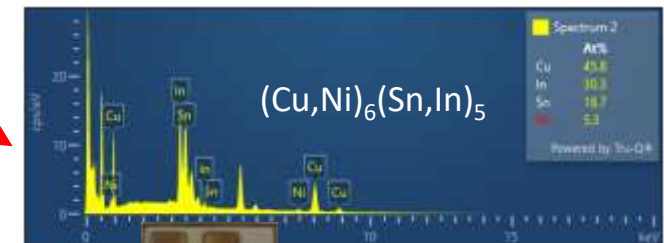
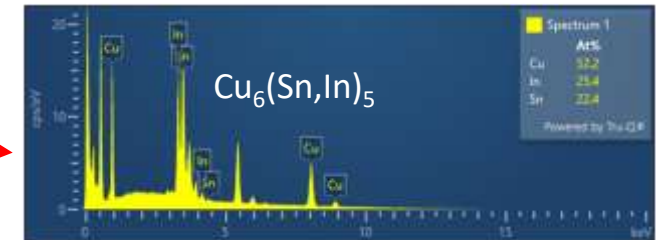


Frontside connection bonded area

backside die-attach bonded area



Cracks in the frontside connection



squeeze out problem: lead to short circuit between drain and source



Top IMS

squeeze out

2.9.2026

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Conclusions

- Wafer-level metal bonding as potential key enabling method for “more than Moore” 3D integration
- SLID μ bumps are very attractive low-cost low-temperature option for 3D HI, advanced packaging, MEMS and power packaging applications (both chip to wafer and wafer to wafer level)
- EM resistant and good high-frequency metrics was observed
- Observed challenges related to process integration, defects, residual stresses and substrates
- Novel metallizations could help in process integration & reliability performance
- Low temperature Cu-In-Sn SLID bonds were successfully demonstrated via 150 mm wafer-level bonding with bonding temperatures down to 150°C
 - ⇒ Lower residual stresses
 - ⇒ Attractive for More-than-Moore integration

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