

11th Electronics System-Integration Technology Conference (IEEE ESTC 2026)
Sept. 9-11, 2026, Helsinki, Finland



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Advanced Packages for Emerging Applications: Markets, Materials, Fabrication Processes and RF Design Considerations

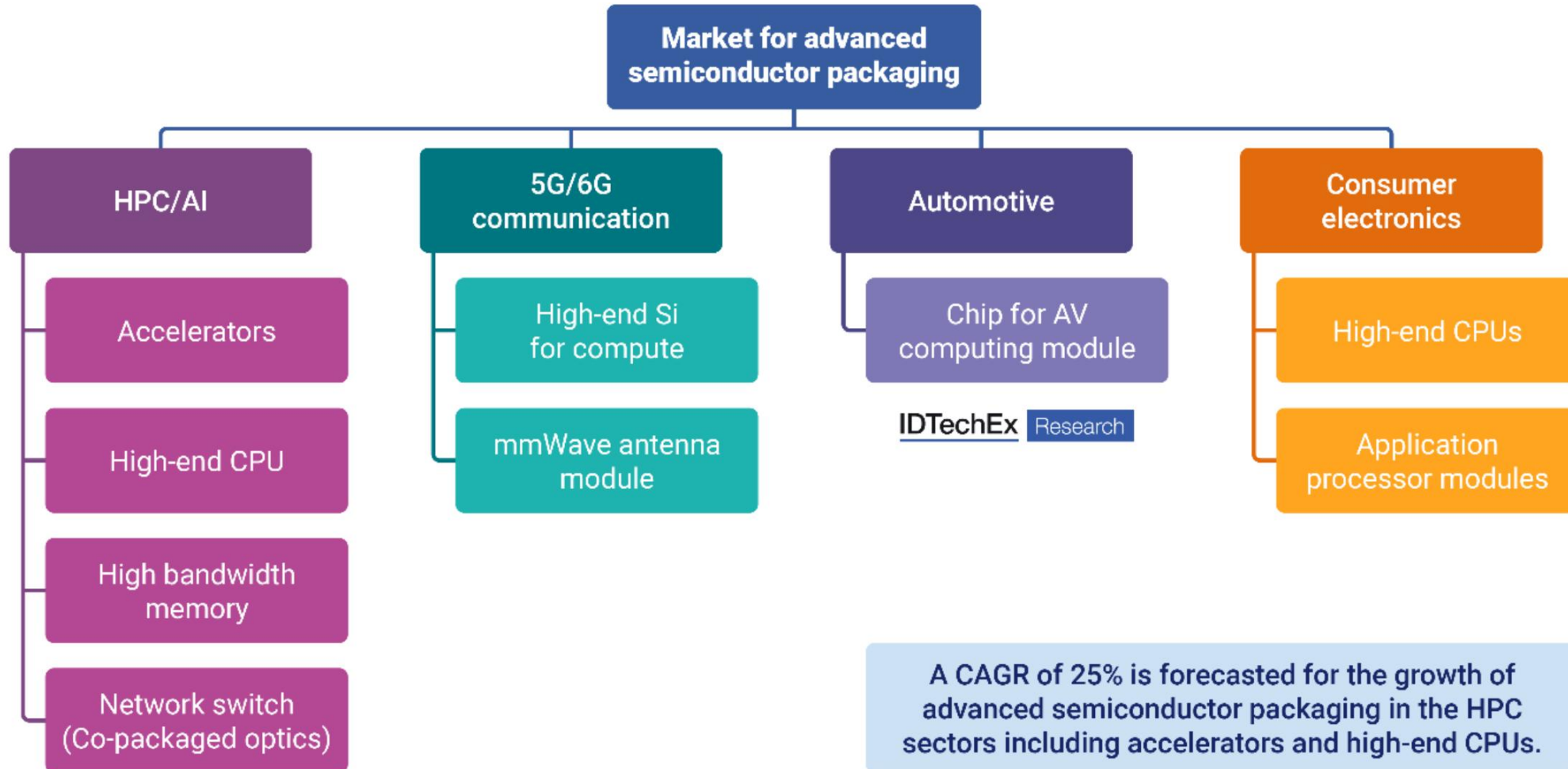
Timeline

08:00 – 08:05	Introduction and Outline of PDC	Ivan/Markus
08:05 – 08:20	Key Applications Driving Advanced Packaging	Ivan
08:20 – 09:10	Materials and Processes for Advanced Packages	Markus
09:10 – 09:20	Break	All
09:20 – 10:00	RF Design Considerations & Packaging Architectures	Ivan
10:00 – 10:15	Summary, Open Questions & Feedback	All

Key Applications Driving Advanced Packaging and Overview of Markets

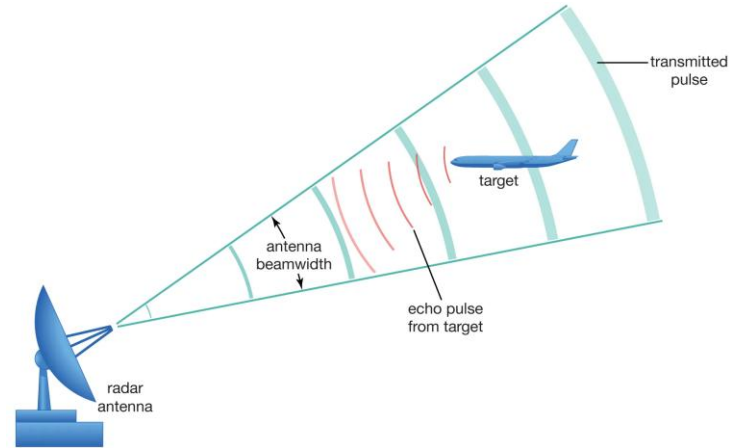
Overview of Markets and Applications driving Advanced Packaging – 1/1

Key Markets for Advanced Semiconductor Packaging



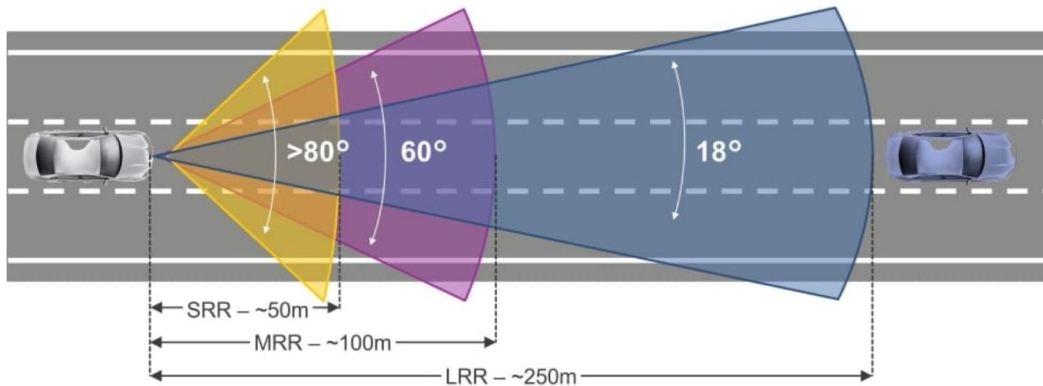
Automotive Radar – 1/2

$$\Delta R = \frac{c}{2 BW}$$



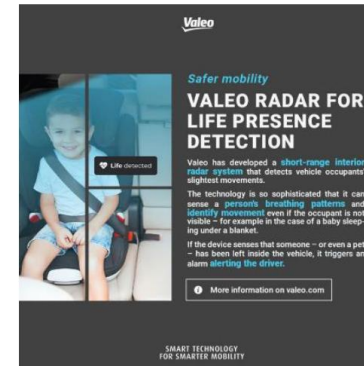
<https://www.britannica.com/technology/radar>

External radar

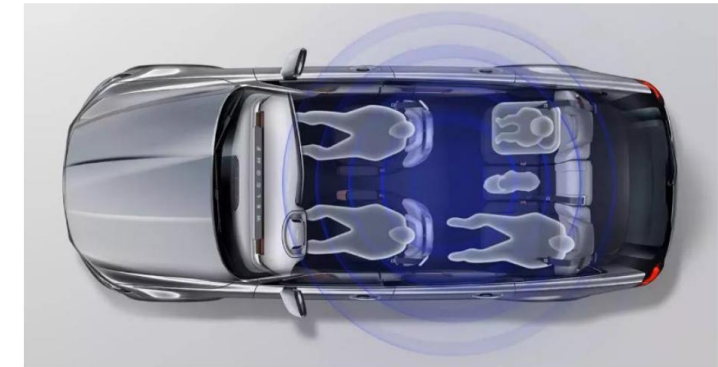


<https://www.renesas.com/us/en/blogs/why-do-we-need-radar>

Internal radar (InCabine)

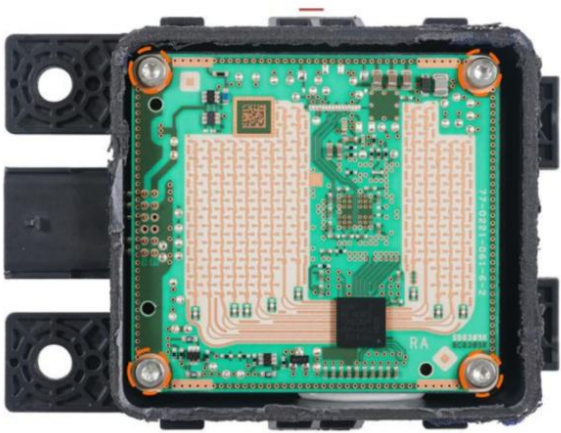


source: Valeo



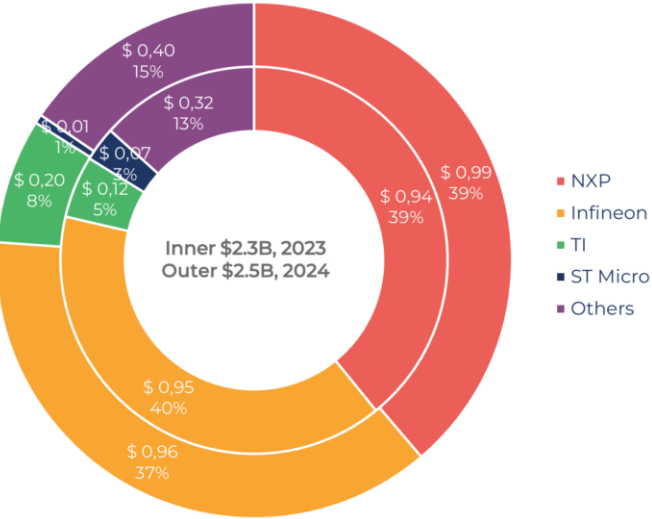
source: Forvia

Automotive Radar – 2/2

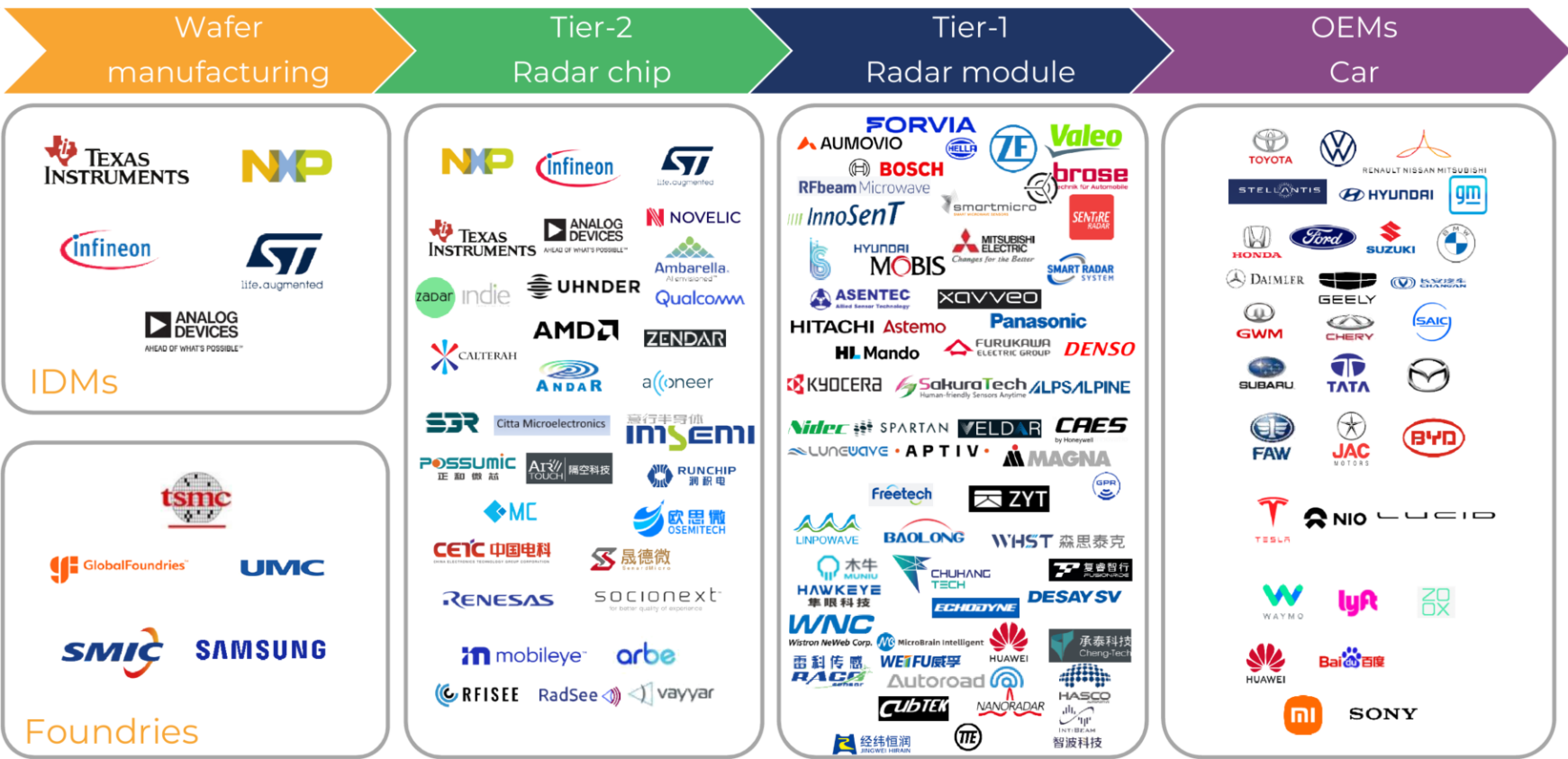


Hella's RS5.3 short-range radar with PCB antenna.

2023 - 2024 overall radar device market share, in \$B

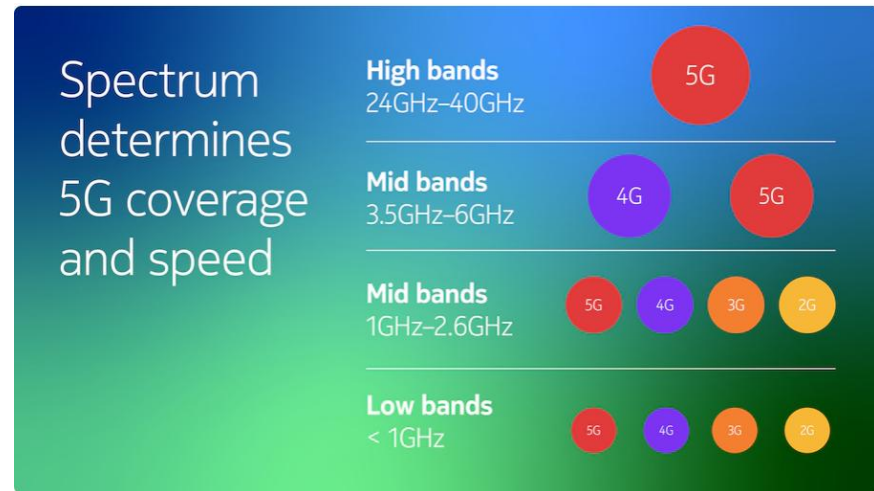


External Radar: Global Market Share



5G/6G Communication – 1/3

■ 5G Band and Use Cases



<https://www.nokia.com/thought-leadership/articles/spectrum-bands-5g-world/>



AIR 1281
High band

<https://www.ericsson.com/en/small-cells/outdoor-coverage>

$$C = BW \cdot \log_2(1 + SNR)$$



Surveillance and video streaming/broadcast



Crowded area capacity



Last mile fiber/copper complement



Everywhere AR/VR



Smart factories industry 4.0

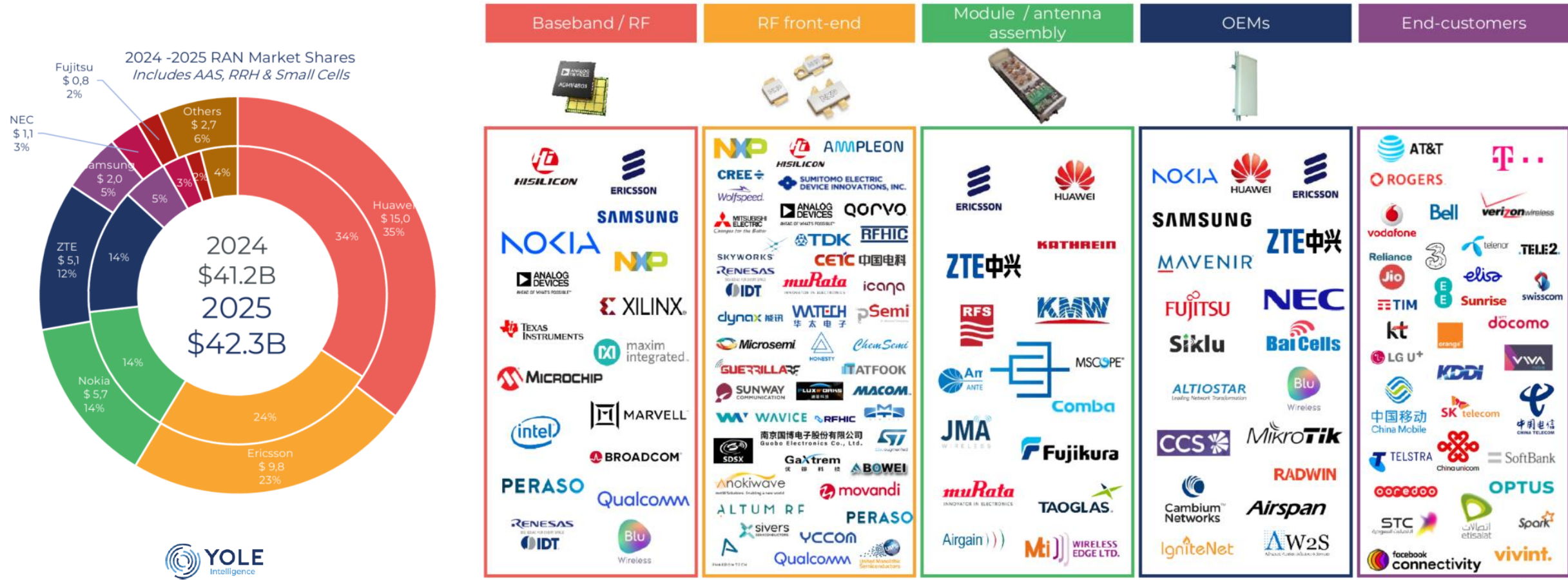


Street macro applications

[5G Technology and Capabilities for Business | Ericsson](#)

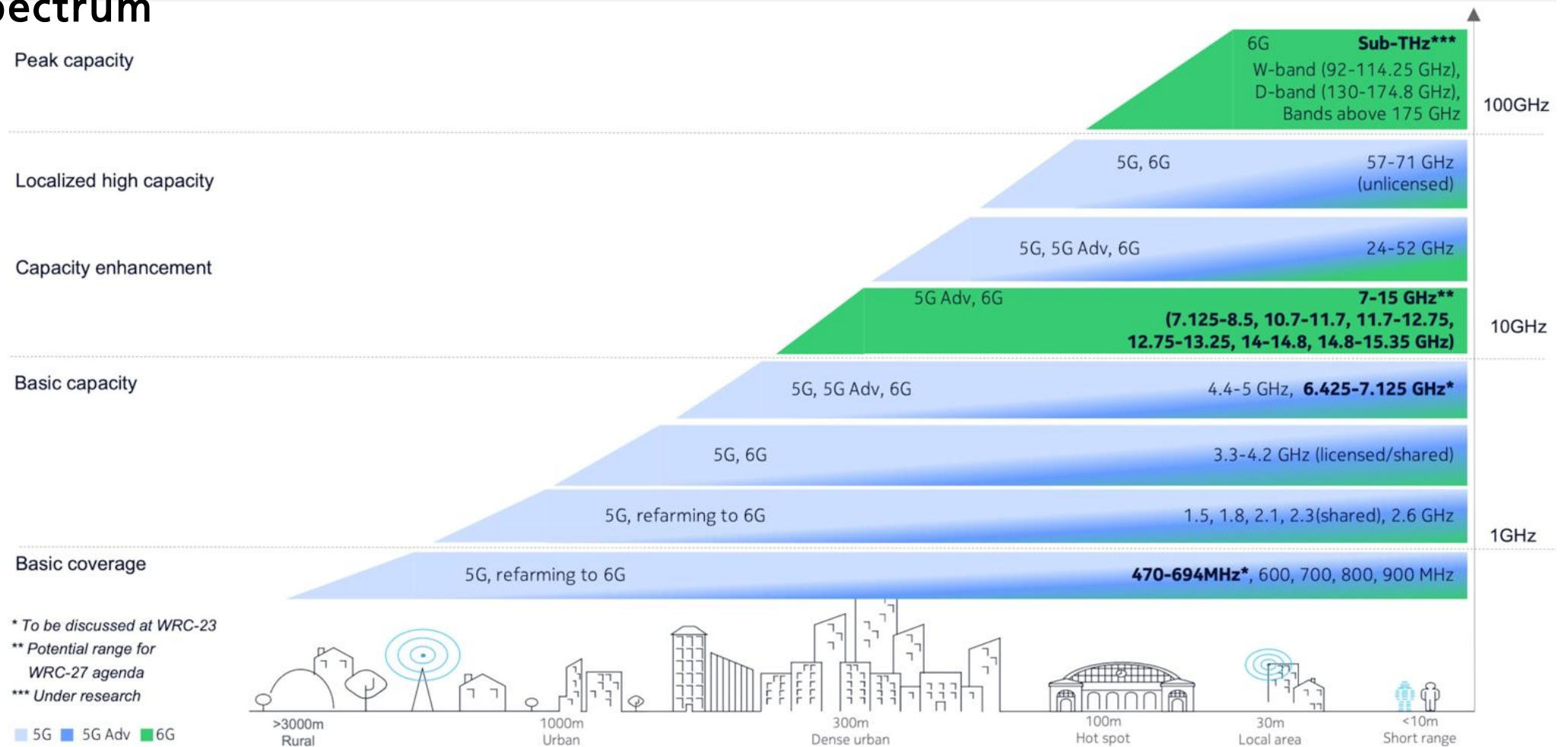
5G/6G Communication – 2/3

■ 5G Cellular Infrastructure (Base Station) Ecosystem



5G/6G Communication – 3/3

■ 5G/6G Spectrum



<https://www.nokia.com/6g/spectrum-for-6G-explained/>

HPC & AI for Data Centers – 1/2

■ Key Drivers

Data-intensive applications



Generative AI is emerging across multiple sectors, relying on data center heavy-compute

Chat: ChatGPT, Gemini, Copilot, Claude, X, Mistral AI

Image: DALL-E, Midjourney, Adobe Firefly, Microsoft Designer

Video: OpenAI Sora, Google Veo 2, Runway, Synthesia, Colossyan

Coding: ChatGPT, GitHub Copilot, AWS CodeWhisperer, Replit, Tabnine

Translation: DeepL, Google Translate, Smartling, Microsoft Translator

Music: Mubert, Loudly, Soundraw, Boomy

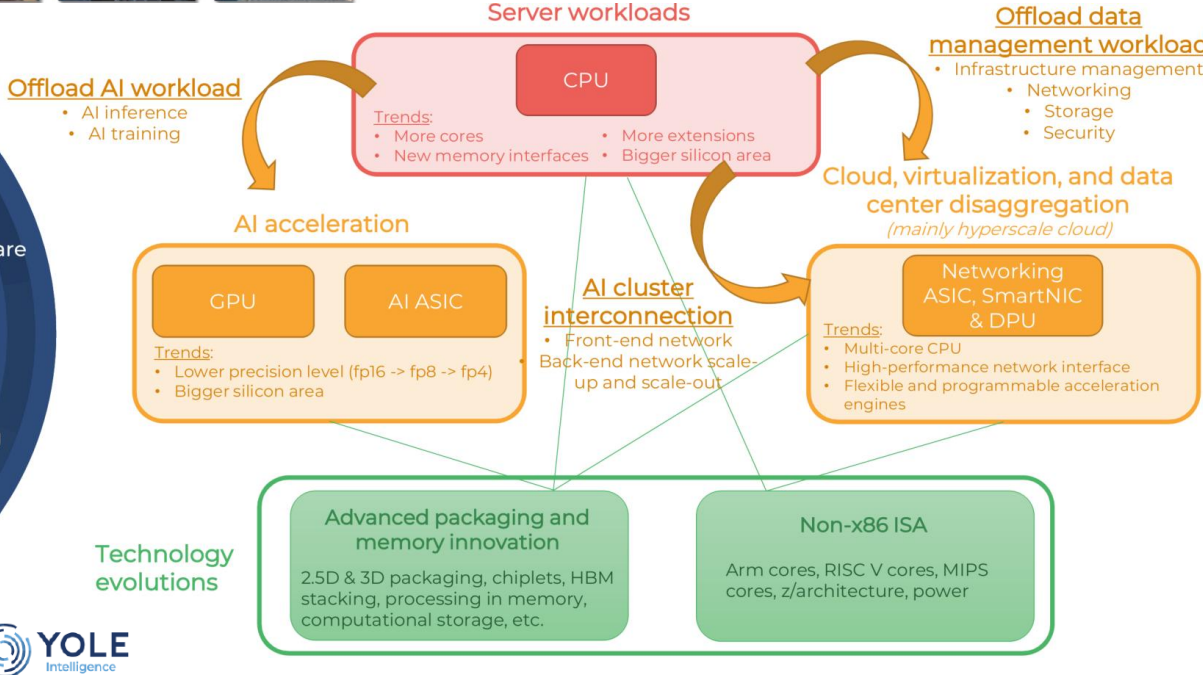
Generative AI tools for lawyers, architects, doctors, and more.

Tools based on generative AI will boost content production.

Generative AI lowers the barrier to entry in many fields that previously required highly specialized skills.

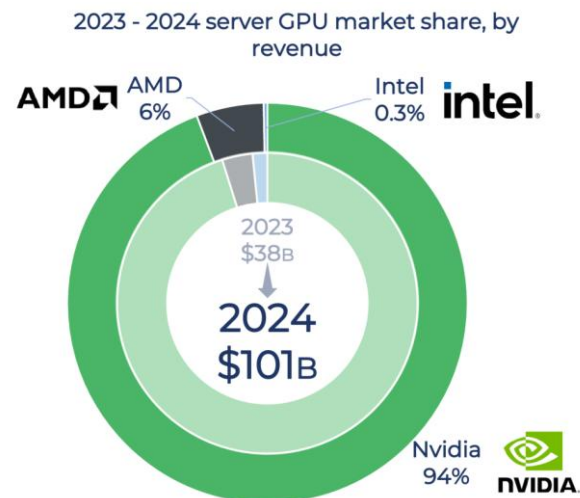
Sam Altman's bet in '20:
Today's AI models are the right ones; the bottleneck is computing.

How to convince investors to put up billions for electricity and AI chips?

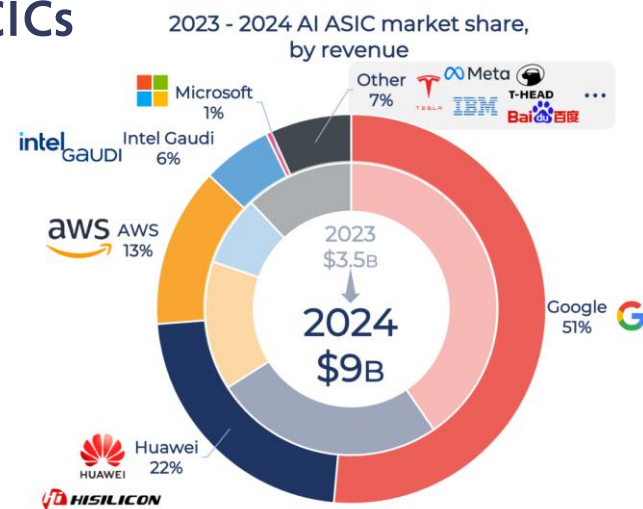


HPC & AI for Data Centers – 2/2

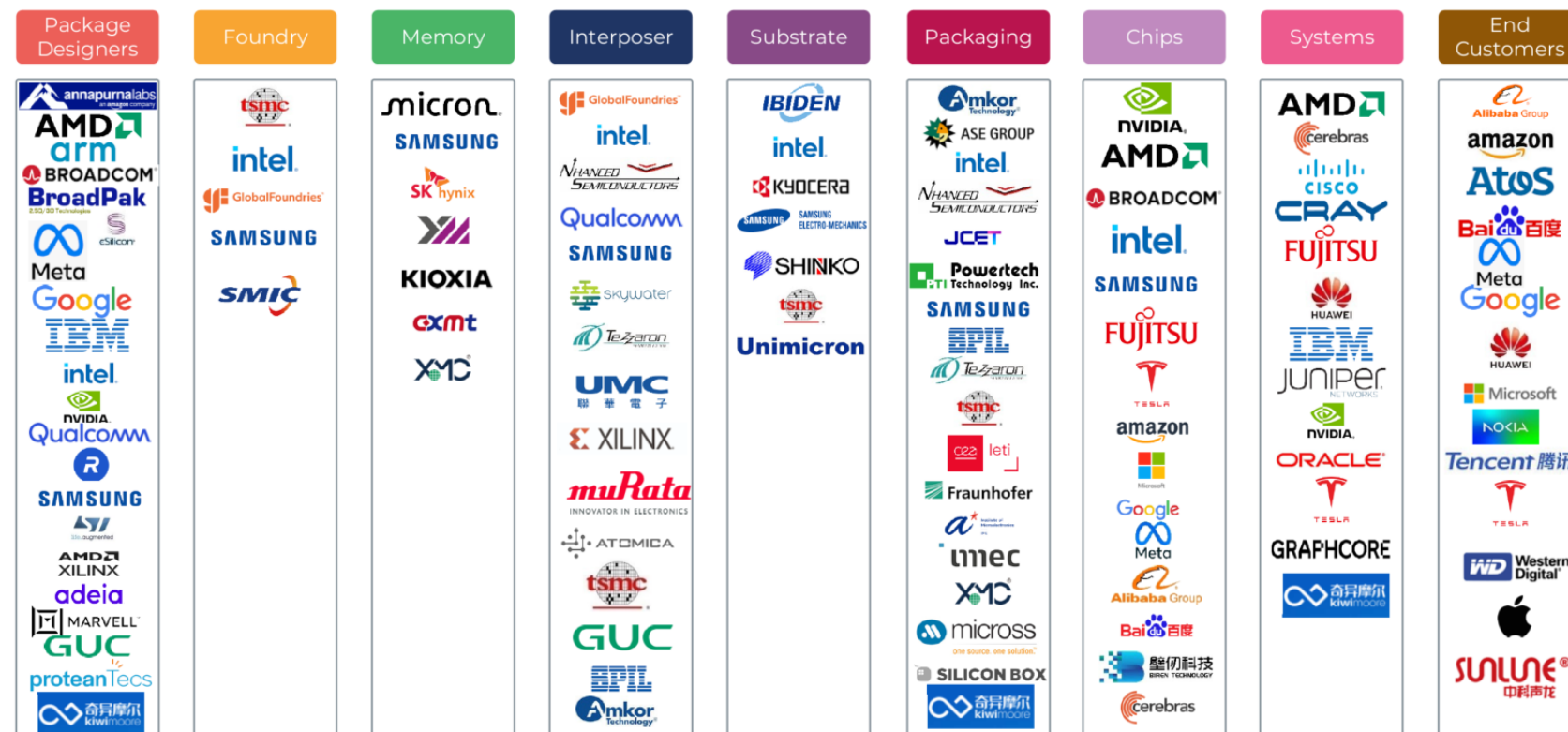
GPUs



AI ASICs

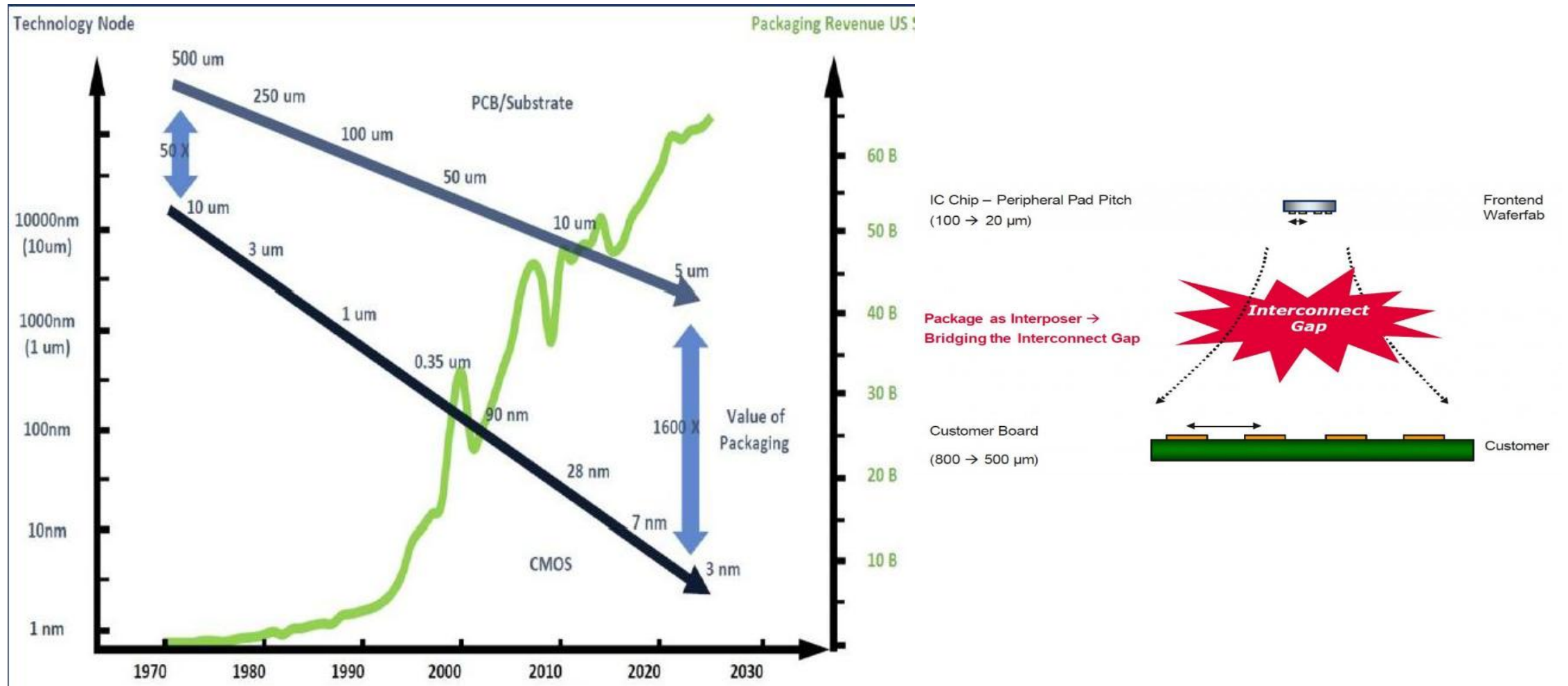


DATACENTER PROCESSOR – FULL SUPPLY CHAIN



Materials and Fabrication Processes for Advanced Packages

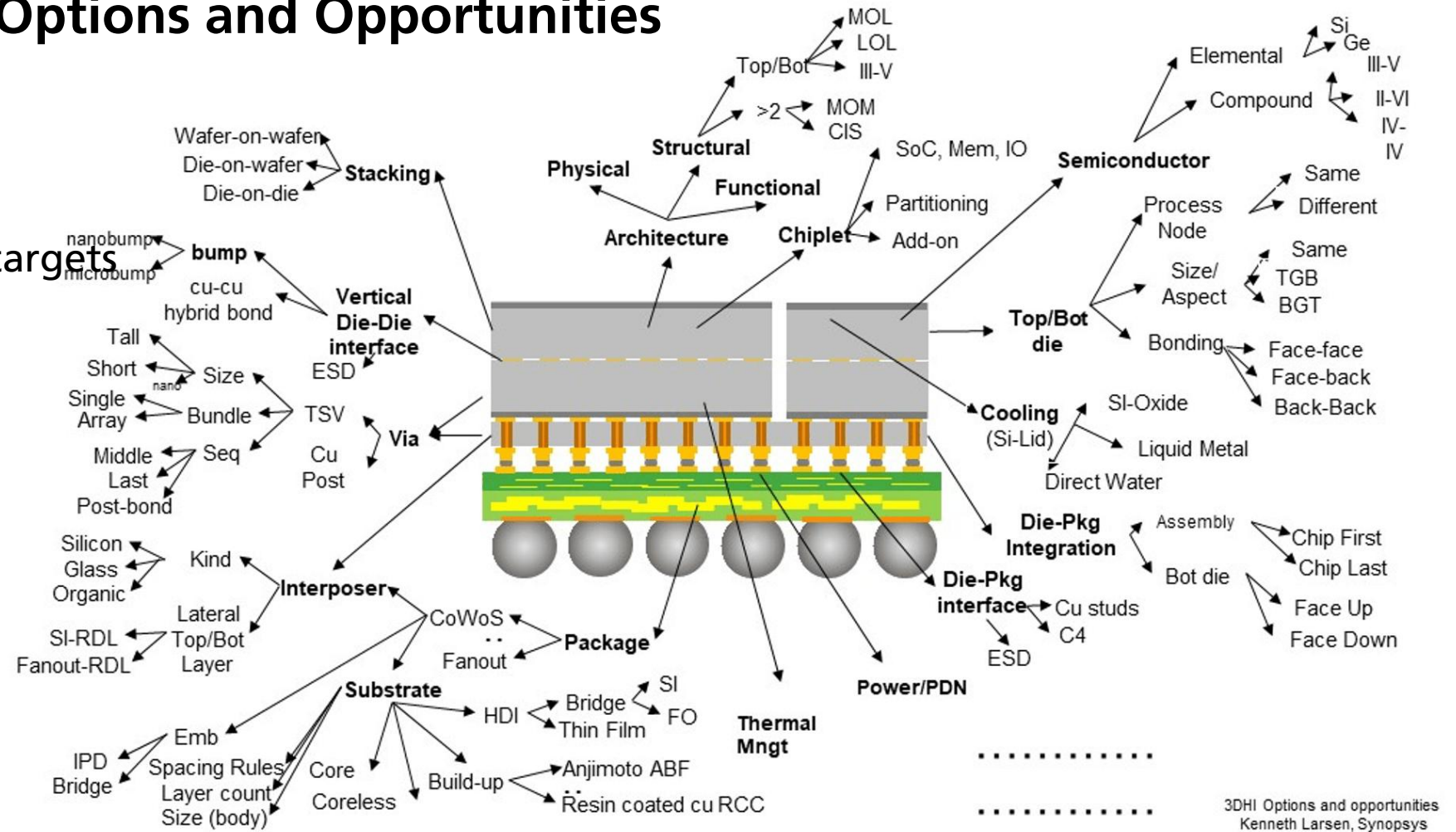
Drivers for Advanced Packaging



Dr. Sam Salama© Hyperion Technologies; IPC APEX EXPO 2023

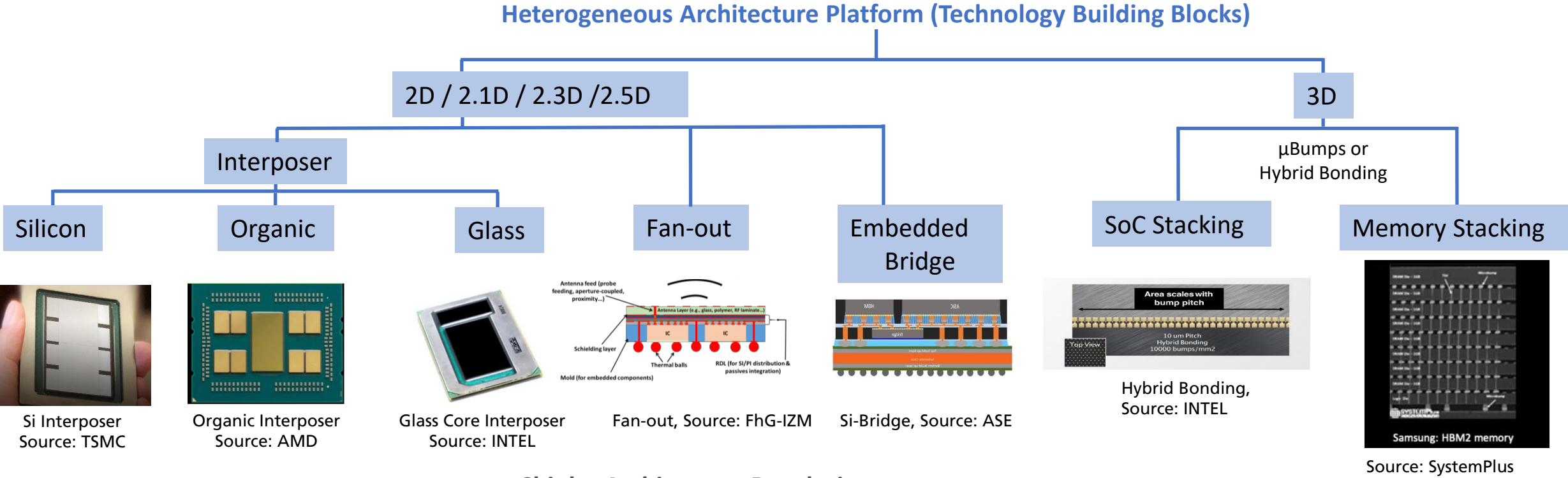
Advanced Packaging Options and Opportunities

- Adv. Pkg. have different targets
- Performance
- Miniaturization
- Functionalization



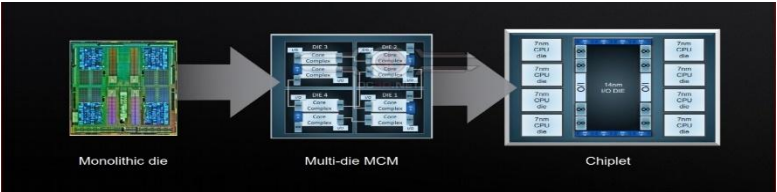
There are a multitude of choices in multi-die packaging from the high-level layout to substrates, materials, bonding methods, and cooling materials. Source: Synopsys

Advanced Packaging Technologies



Chiplet Architecture Revolution

Different technology building blocks can be used for Chiplets



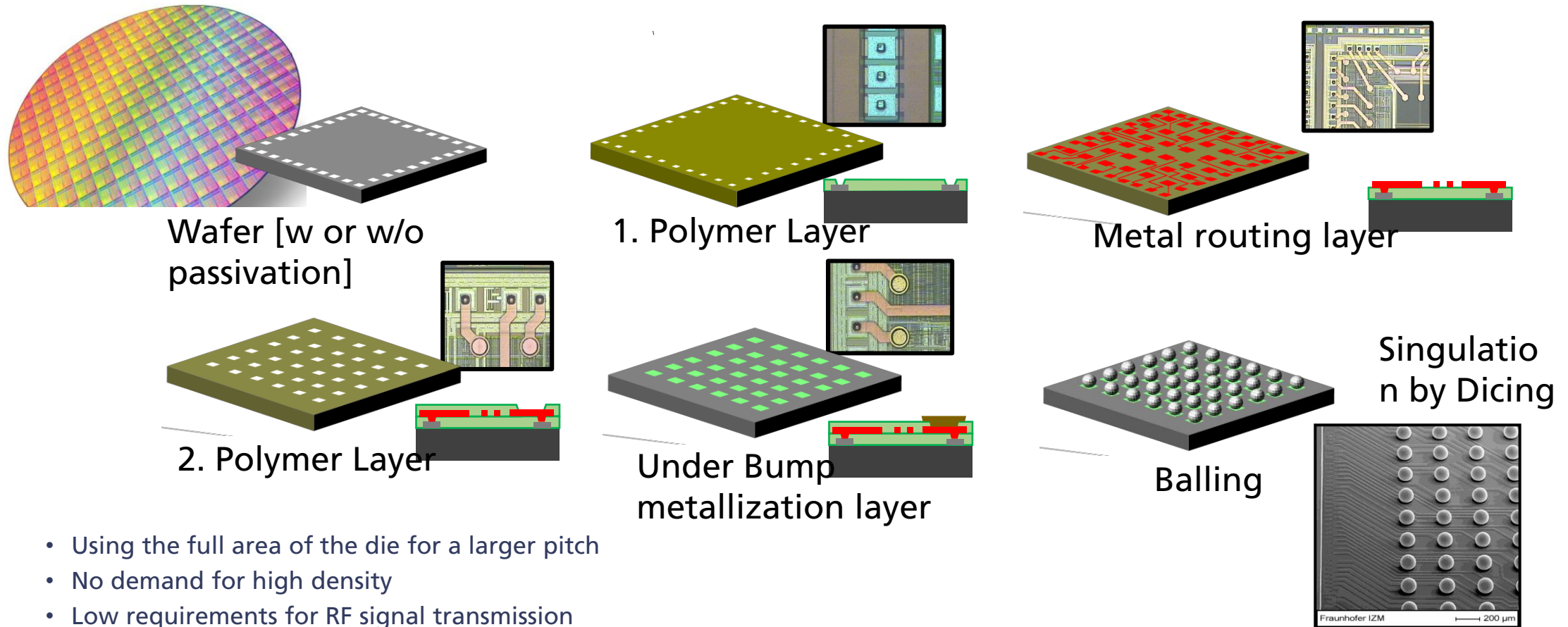
Chiplets will be a key enabler for next 10-15 years

Source: AMD, Overclock3D.net

for HPC, AI, Automotive, Industrial Automation, 5G/6G, Health Care, Energy, Aerospace, ...

WLP using Redistribution Technology

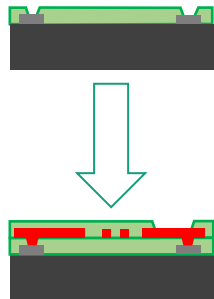
WLP - a 4 layer (4 Lithography steps) Semi-Additive Process (SAP)



- Using the full area of the die for a larger pitch
- No demand for high density
- Low requirements for RF signal transmission

IZM Wafer Level Packaging Line (RDL)

Flow for one RDL layer



Seed Layer → Resist Process → Lithography → Plating → Strip / Etching



Sputter



Spin Coater



Mask Aligner



Wafer Plating



Wet Etching

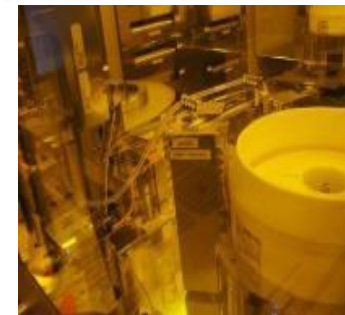
Polymer Dep. → Lithography → Development → Cure → Descum



Spin Coater



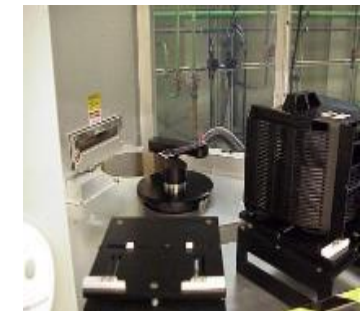
Mask Aligner



Spin Coater

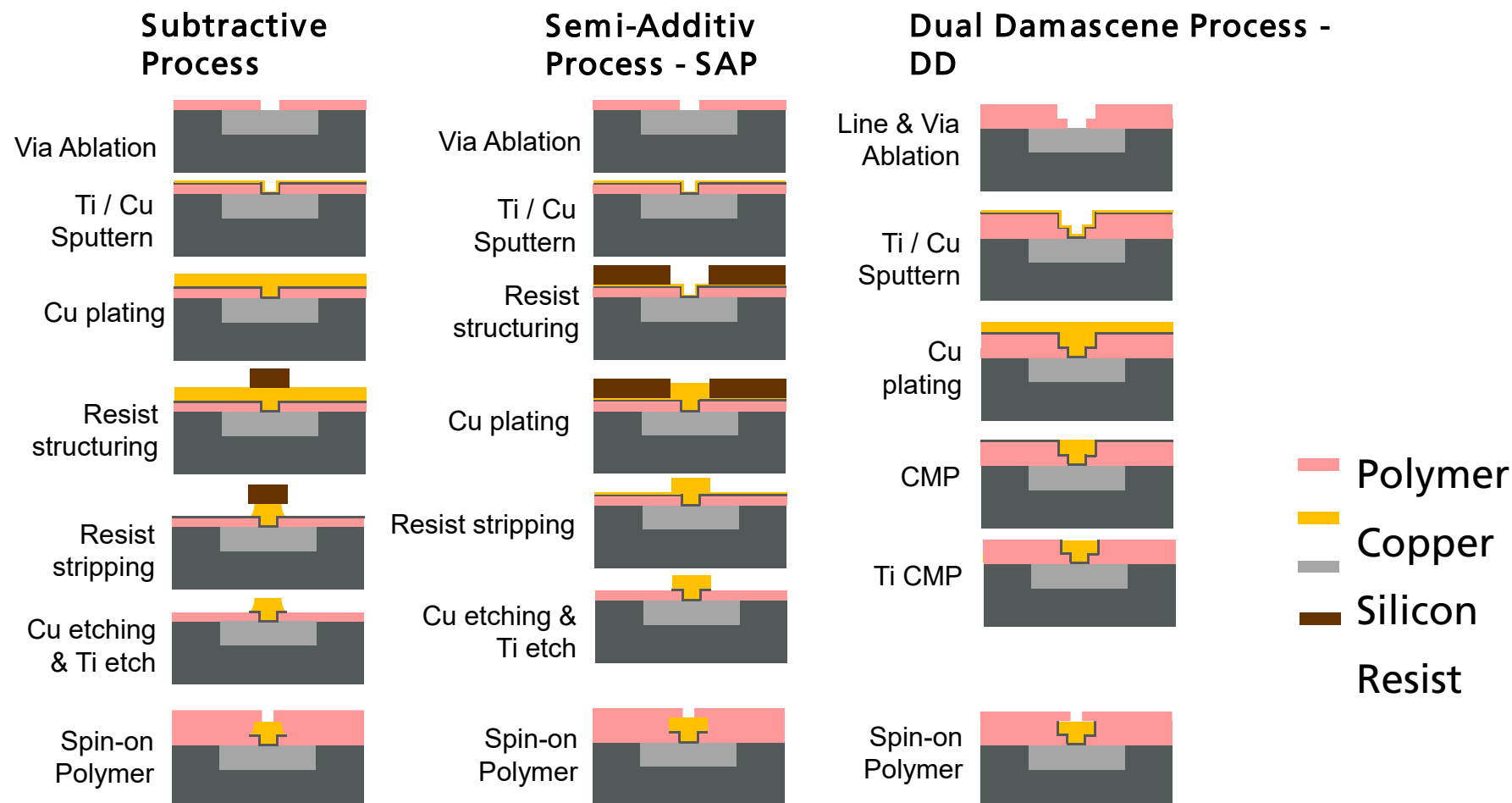


N2 Oven



RIE

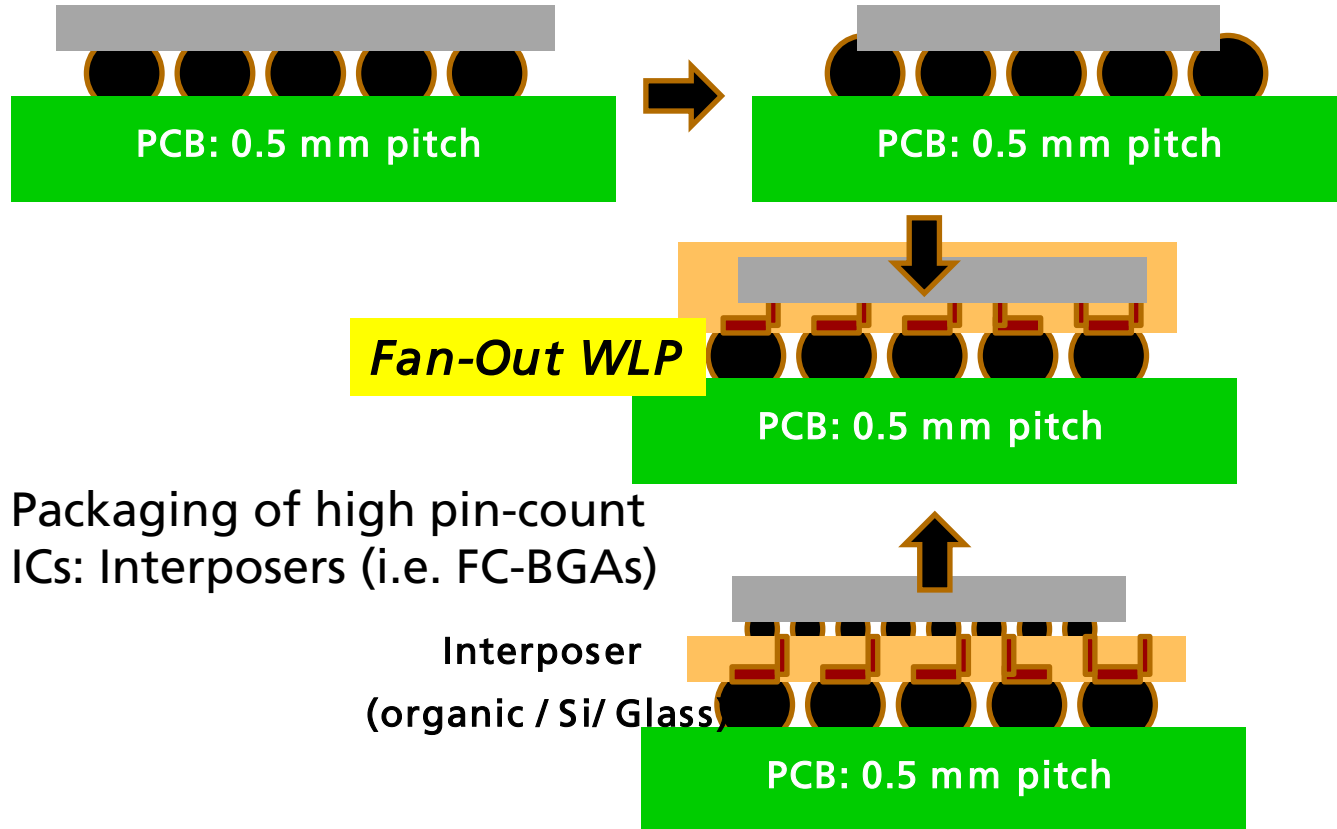
Processing technologies for RDL



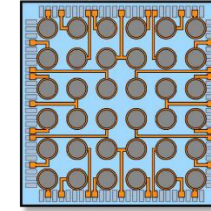
FO-WLPs/PLPs Processes

Why Fan-Out

Fan-In WLP: Issue with miniaturization in Front-End (CMOS)

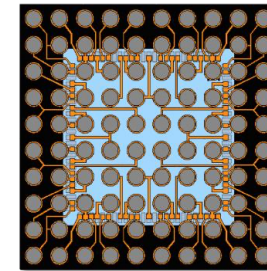


Packaging of high pin-count ICs: Interposers (i.e. FC-BGAs)



“Fan In”

All RDL traces are routed in towards the center of the die



“Fan Out”

RDL traces are routed both in and outwards beyond the limits of the die

Source: ASE 2017

FOWLP/FOPLP Process Flow Options

Mold first

face-down

Apply thermal release tape on carrier



Face-down die assembly on carrier



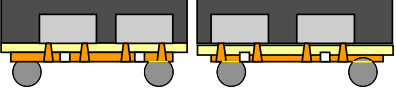
Wafer/panel overmolding



Carrier release



RDL (e.g. thin film, PCB based, ...),
balling, singulation



RDL
generation

„eWLB“

„RCP“

face-up

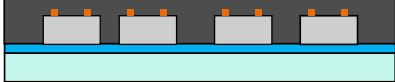
Apply temporary bond layer on carrier



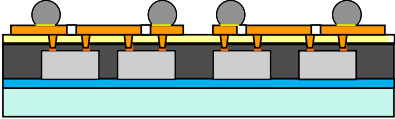
Face-up die assembly on carrier



Wafer/panel overmolding

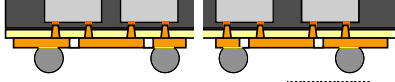


Mold back grinding and RDL



RDL
generation

Carrier release and singulation



„InFo“

„M-Series“

RDL first

Apply release layer on carrier

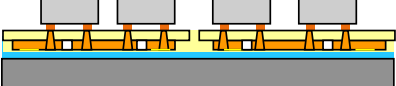


RDL (e.g. thin film, PCB based, ...)

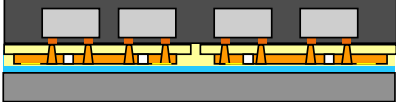


RDL
generation

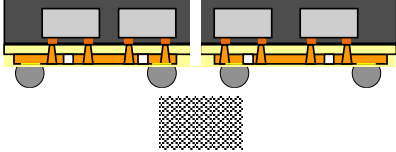
Die assembly on carrier



Wafer/panel overmolding



Carrier release, balling, singulation

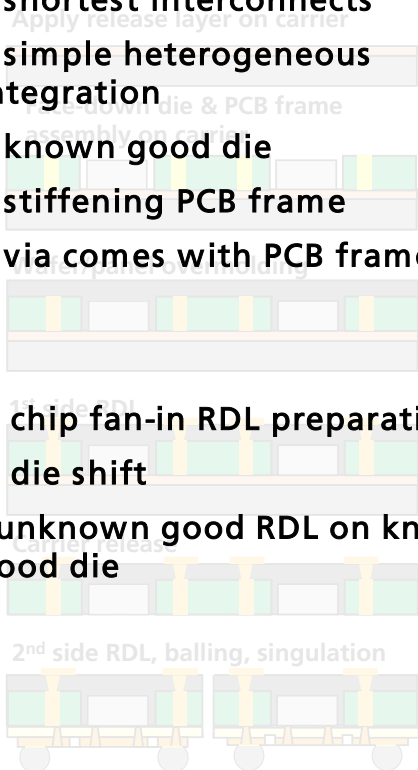


FOWLP/FOPLP Process Flow Options

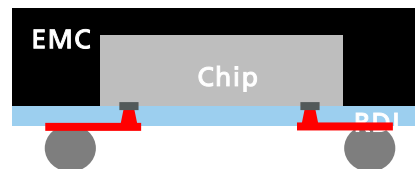
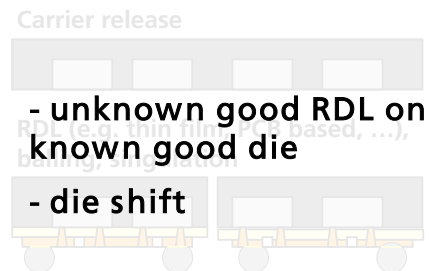
Mold first

face-down

- + shortest interconnects
- + simple heterogeneous integration
- + known good die
- + stiffening PCB frame
- + via comes with PCB frame
- chip fan-in RDL preparation
- die shift
- unknown good RDL on known good die

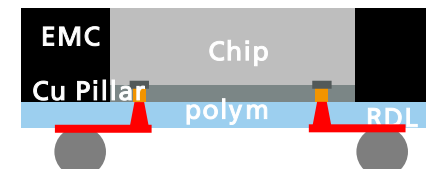
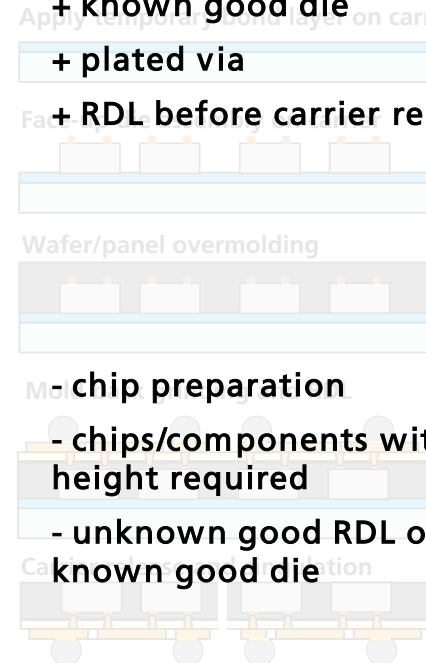


- + no chip preparation
- + shortest interconnects
- + simple heterogeneous integration
- + known good die
- + various via technologies
- + fine line RDL first



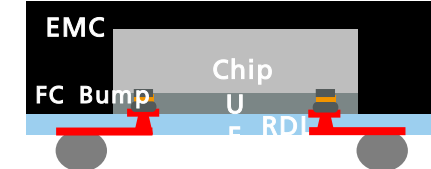
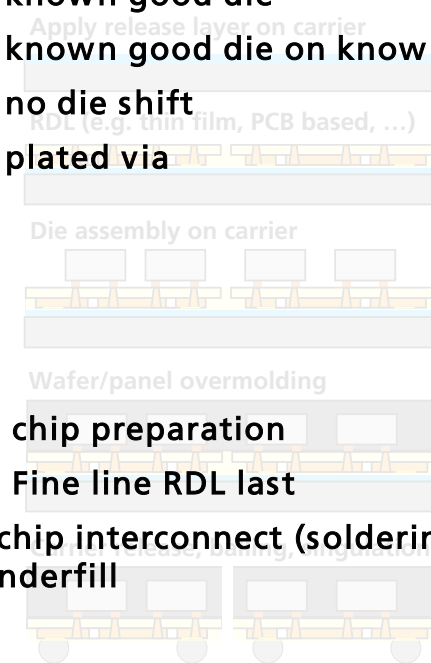
face-up

- + known good die
- + plated via
- + RDL before carrier release
- chip preparation
- chips/components with same height required
- unknown good RDL on known good die



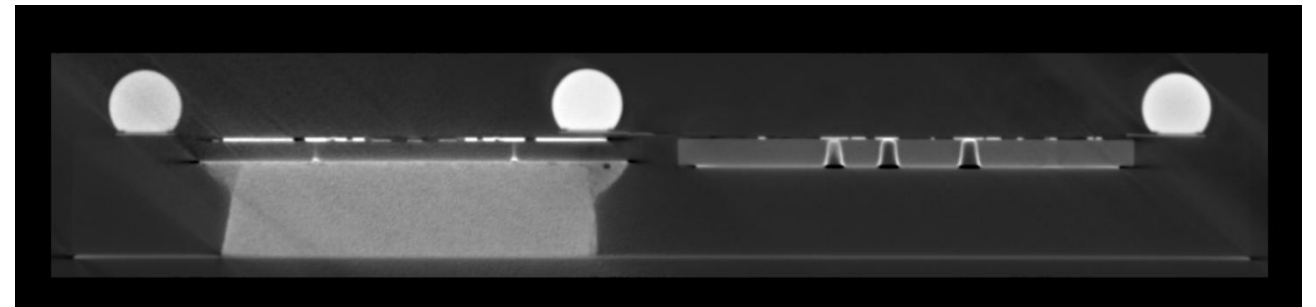
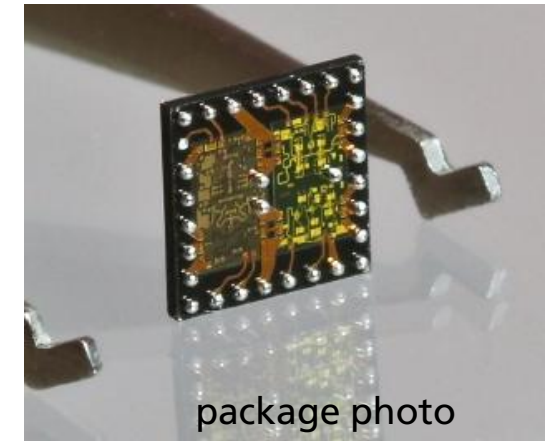
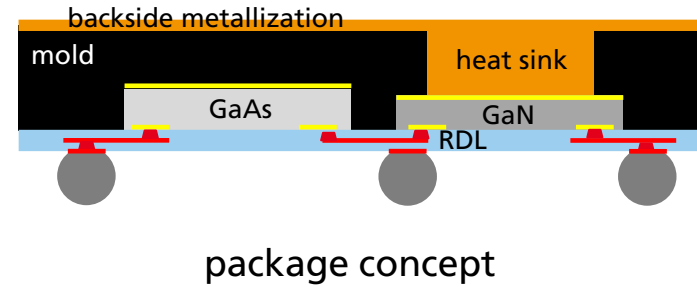
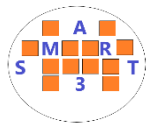
RDL first

- + known good die
- + known good die on known good RDL
- + no die shift
- + plated via
- chip preparation
- Fine line RDL last
- chip interconnect (soldering) & underfill

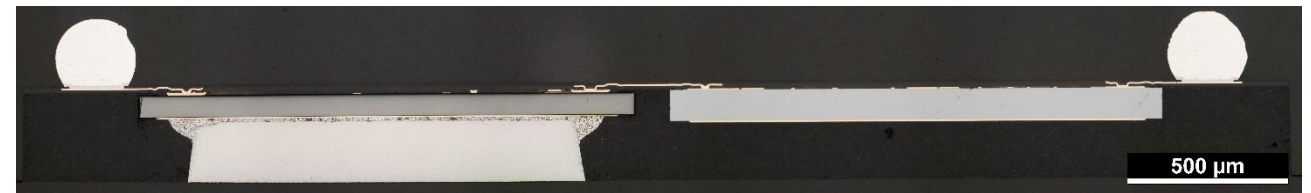


FOWLP GaN & GaAs Integration

- Successful integration of one **GaN** and one **GaAs** die in a FOWLP package
- Direct attach of heat sink on GaN backside and integration in package
- Cu metallization on package backside by direct metallization on epoxy molding compound and heat sink
- 5G HPA (High Power Amplifier) and LNA (Low Noise Amplifier) integration in one package



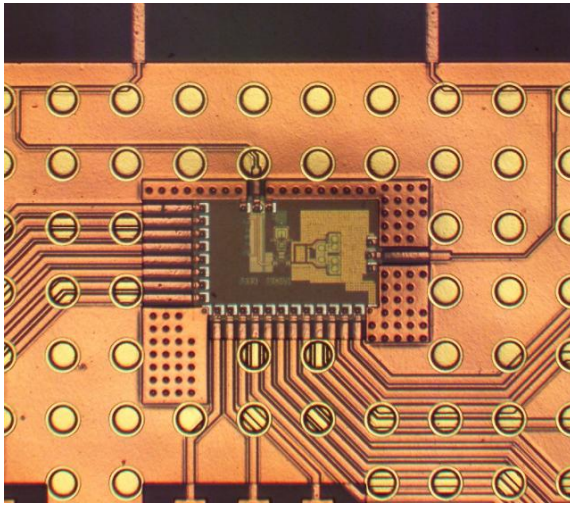
X-ray CT cross section



Multi-layered RDLs

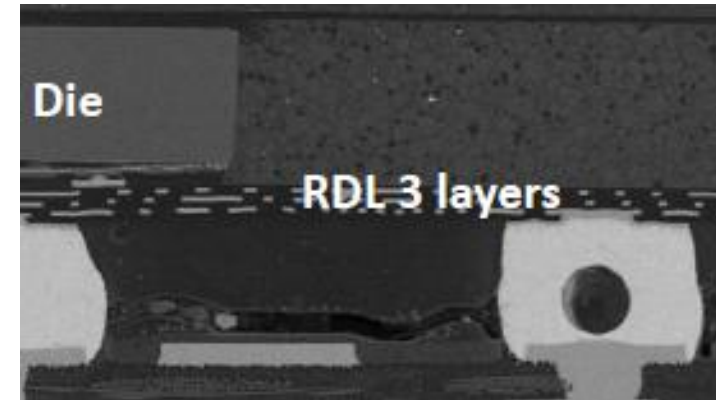
Drivers for High Density / Multi Layer Routing (Focus on FanOut)

RF Application



- Medium/ low I/O routing
- L/S defined by signal integrity
- Multi die integraton
- **Multi layers for shielding layer**

Application Processor

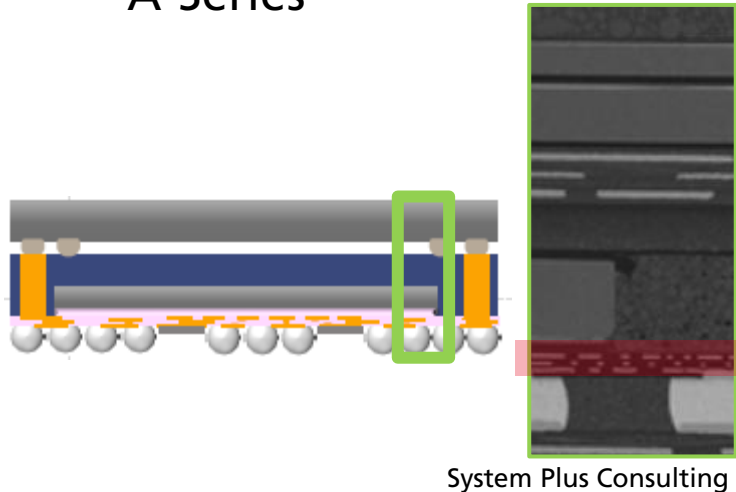


System Plus Consulting

- High I/O routing
- High demands on L/S (layer reduction)
- **Multi layer for managing of routing efforts**

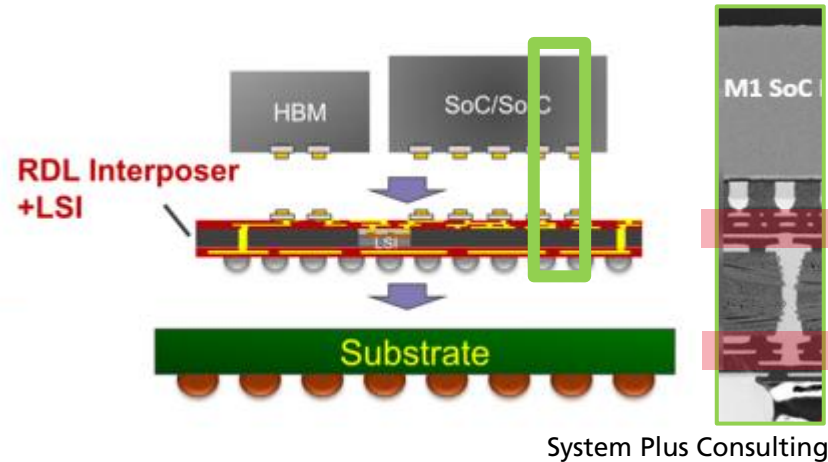
RDL in Advanced Packages Today

inFO+ PoP
A-Series



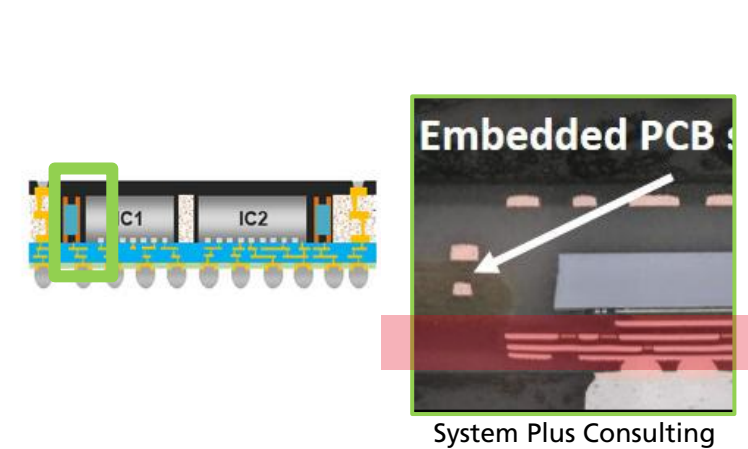
- Application: Smartphone
- 3-layer redistribution
- Single side build-up

CoWoS-L
M-Series



- Application: Pads, Laptop
- 3+2+2 organic substrate
- Double side processing

ePLP
Exynos



- Application: Smart Watch
- 4-layer redistribution
- Single side build-up

Organic Interposer is one of the key words in advanced packaging (conferences like IEEE-ECTC 2022)

Source: System plus consulting

RDL-First for hybrid-Substrat Generation

- Using carrier technology from FO RDL-First for high density RDL routing

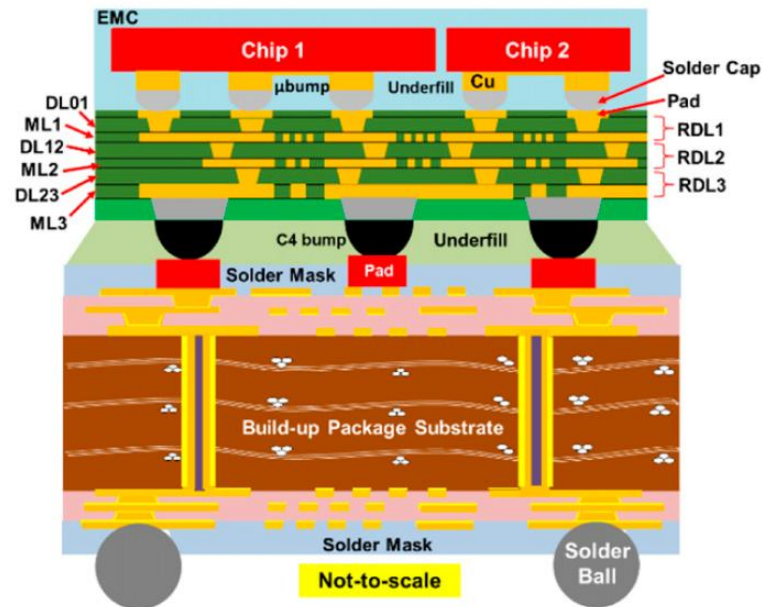


Fig. 3. Schematic of heterogeneous integration of chips on a hybrid substrate.
Unimicron 2022

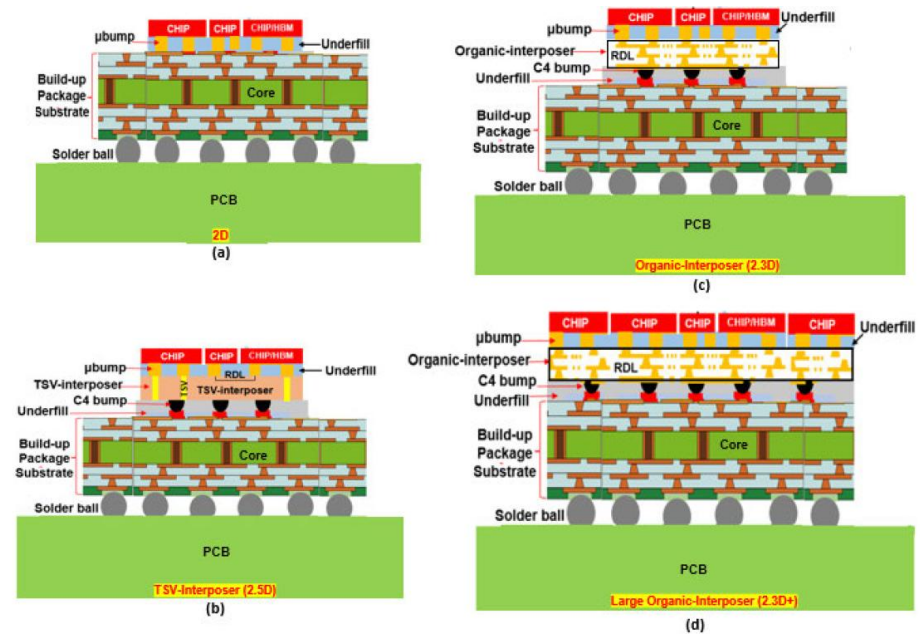


Fig. 1. (a) 2-D IC integration. (b) 2.5-D IC integration. (c) 2.3-D IC integration. (d) 2.3-D+ IC integration.

Unimicron 2023

Packing Integration - SiP

- Advanced Packages → SiP → challenges for RF integration

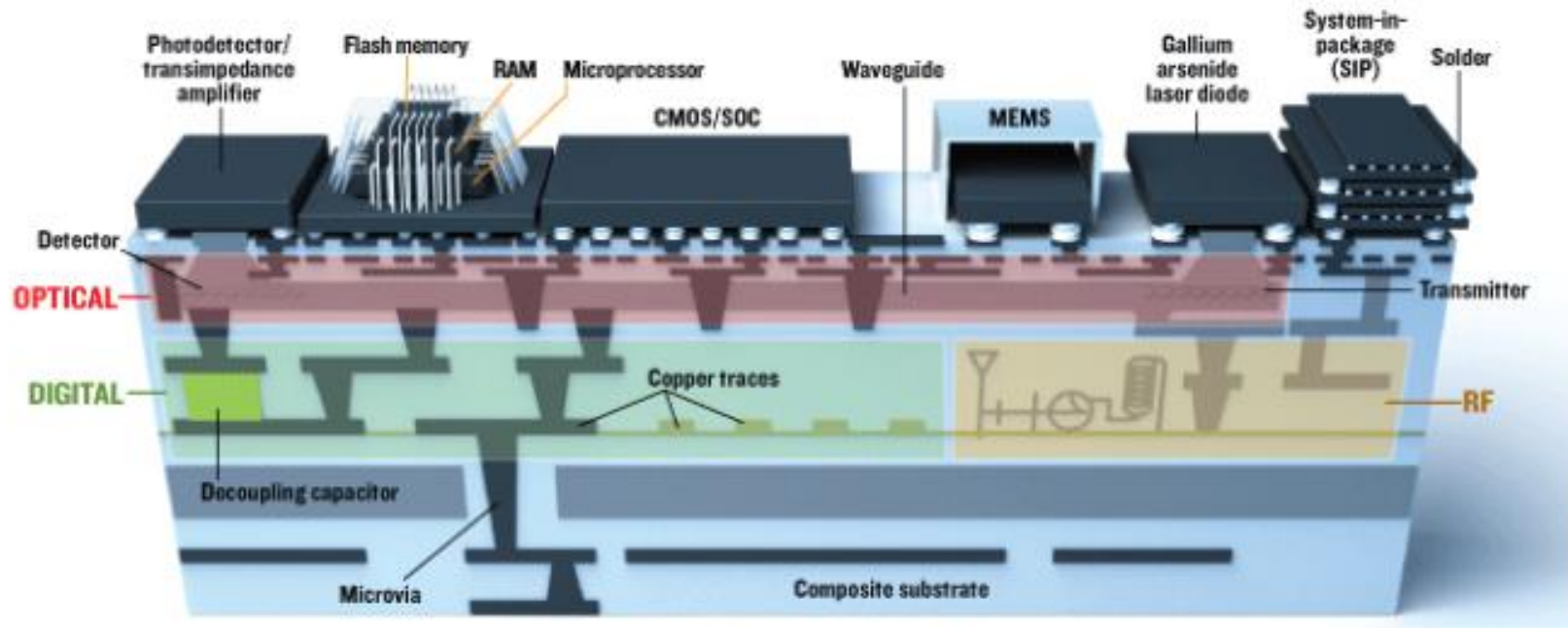
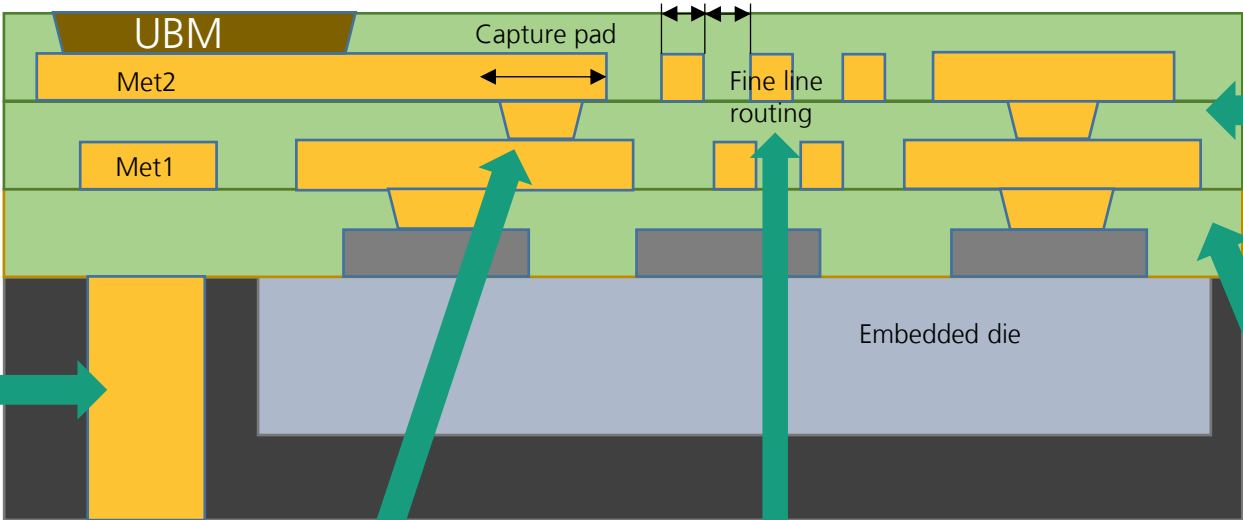
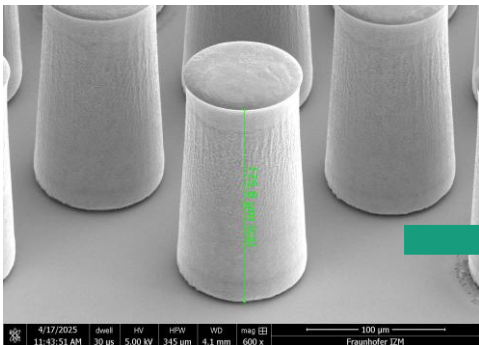


Figure 4: 3D heterogeneous integration

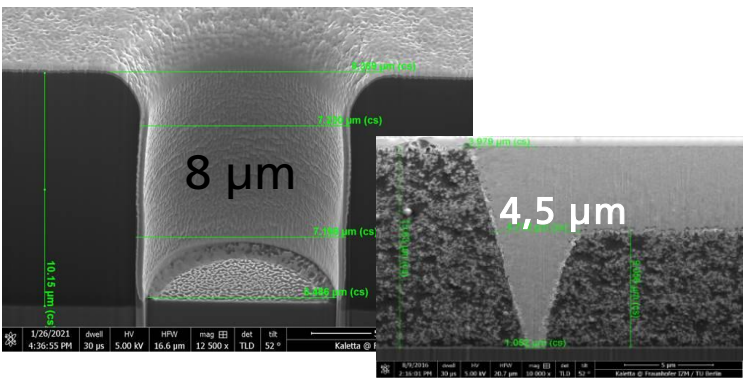
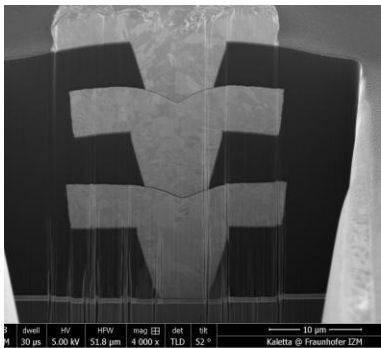
Heterogeneous Integration Roadmap
2019

R&D Topics for Advanced RDL

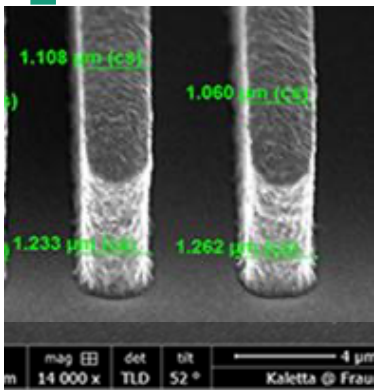
Tall pillar plating



High resolution polymers/ vias

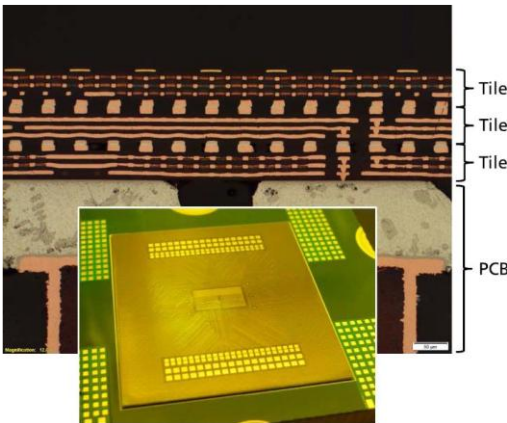


Fine line routing



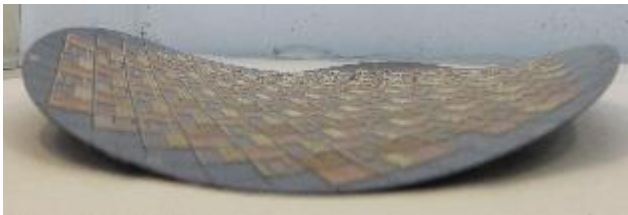
Cu-ion migration stability

Multi-layer processing



IZM multi-RDL stacking (35mmx35mm) with 9 layers of 8 μm L/S – organic interposer

Thick RDL layer - Warpage management



Fillers could Improve the Signal Integrity

-Various materials could be added in the interdielectric layer polymer matrix for decreasing of dielectric constant and dielectric loss

Table 1. Dielectric properties and densities of fillers

Fillars	Dk	Df	densities
Zeolite A	3.3	0.0237	1.5
Zeolite B	3.8	0.0261	1.8
Boron nitride	4.7	0.0012	2.3
Talc A	5.1	0.0047	2.7
Talc B	5.3	0.0003	2.7
Fired talc A	5.8	0.0026	2.9
Magnesium oxide	5.9	0.0036	2.7
Fired talc B	6.1	0.0026	3.0
Aluminum oxide	7.5	0.0010	4.0
Fused silica	3.4	0.0017	2.2
Filler A	2.9	0.0010	1.8

Source: Mitsubishi Gas Chemicals, ECTC 2018

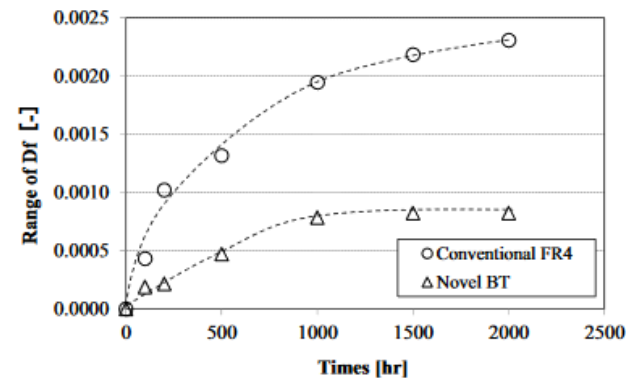
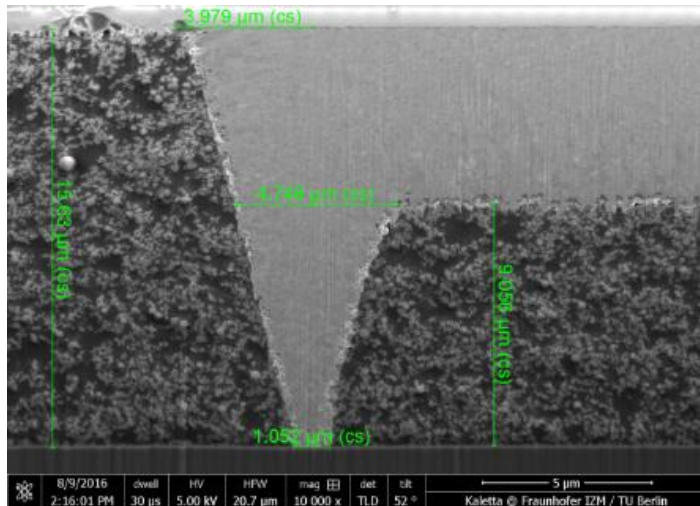


Figure 17. Df change at 125 deg C

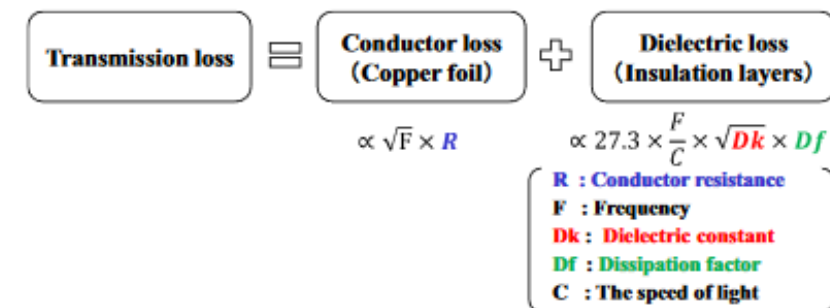


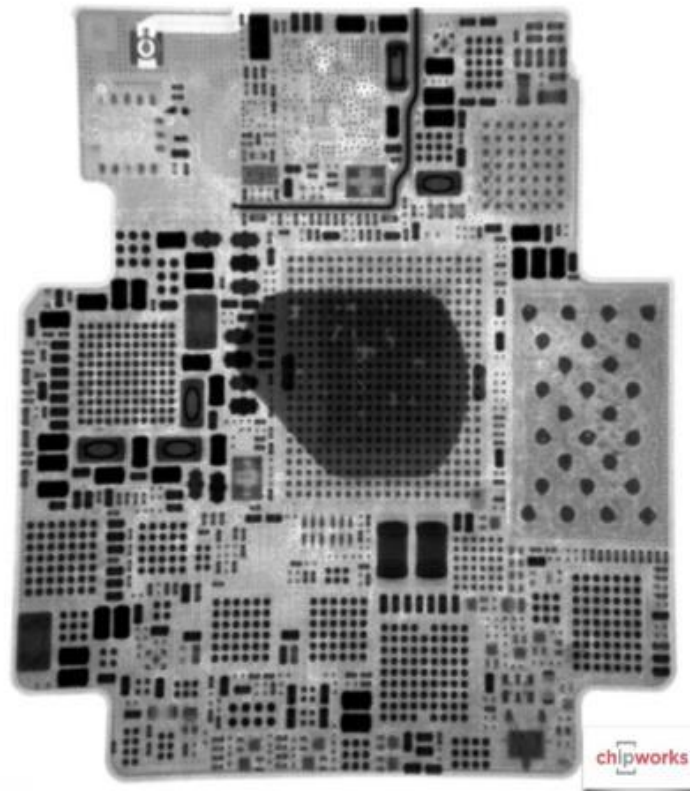
Figure 1. The relationship of Transmission loss

Advanced 3D Packaging

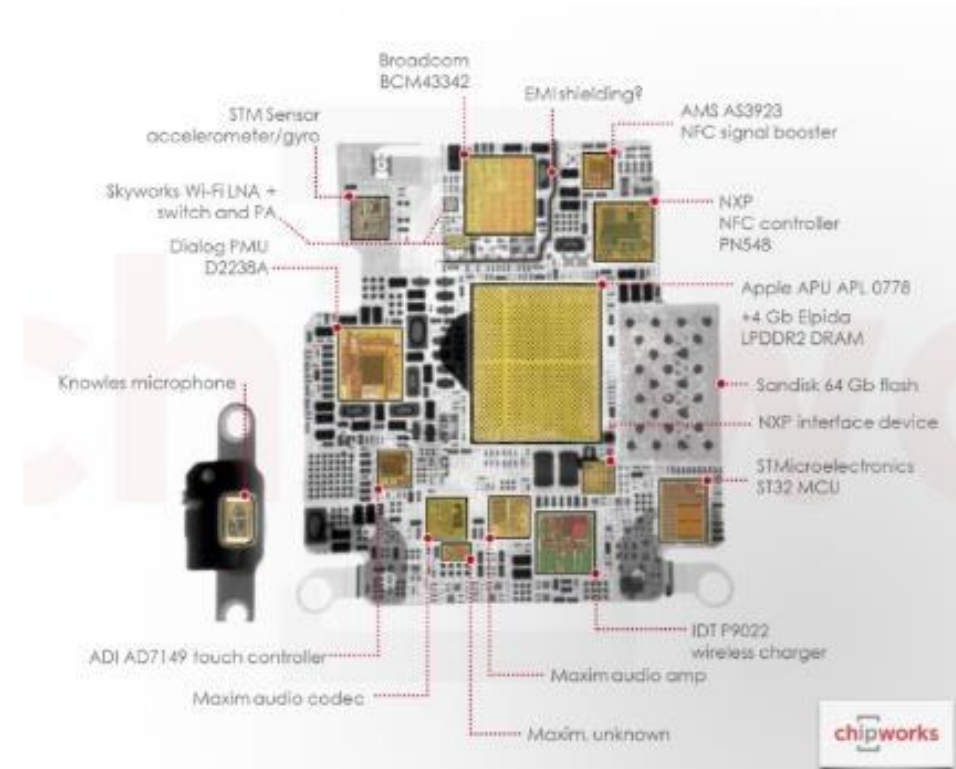
Issue with WLP: Chip Shrinkage

*For SMD-Assembly 0.5/0.4 mm ball pitch is required
(yield and speed of assembly)*

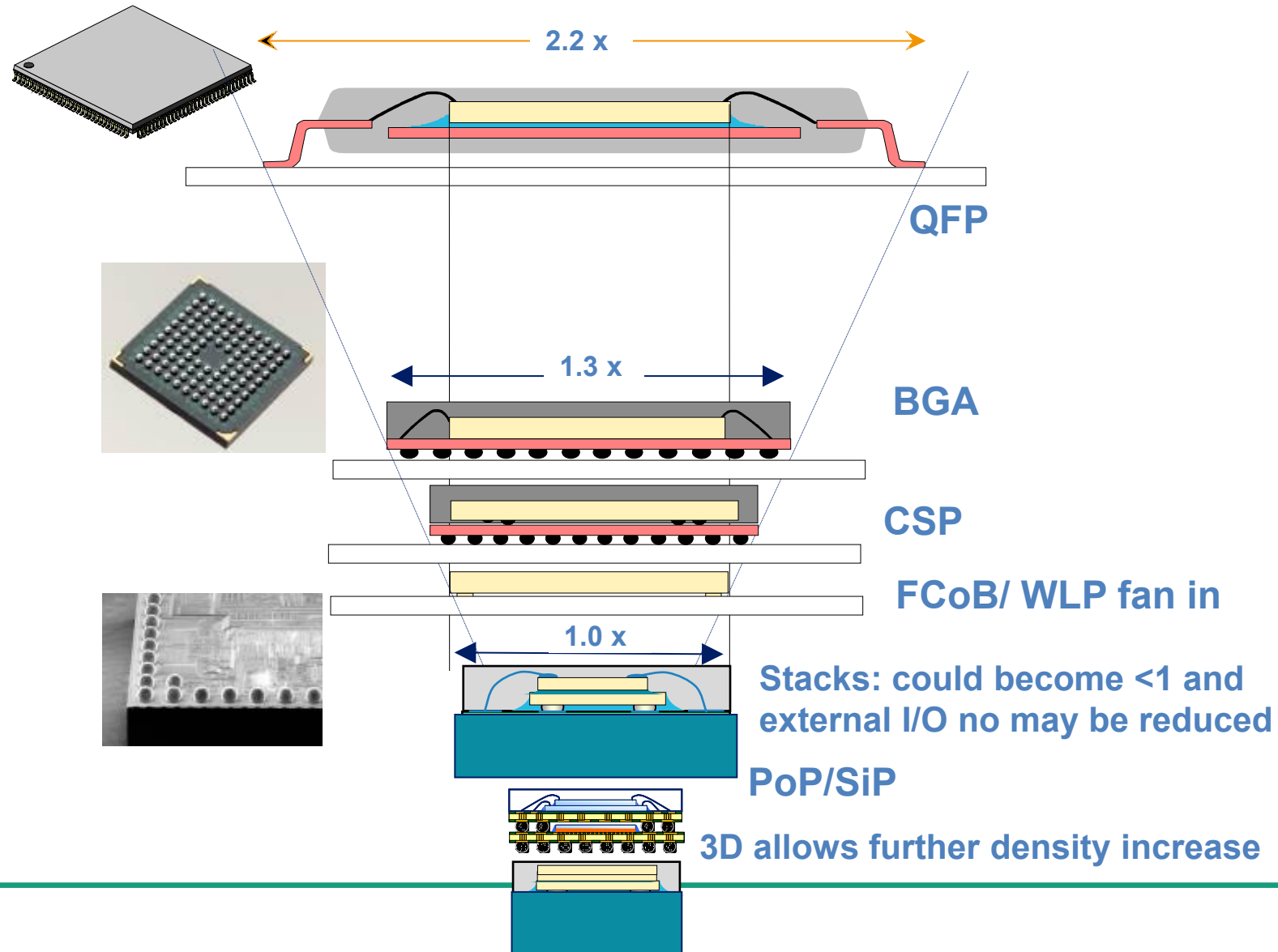
iWatch



(Yole 2015)



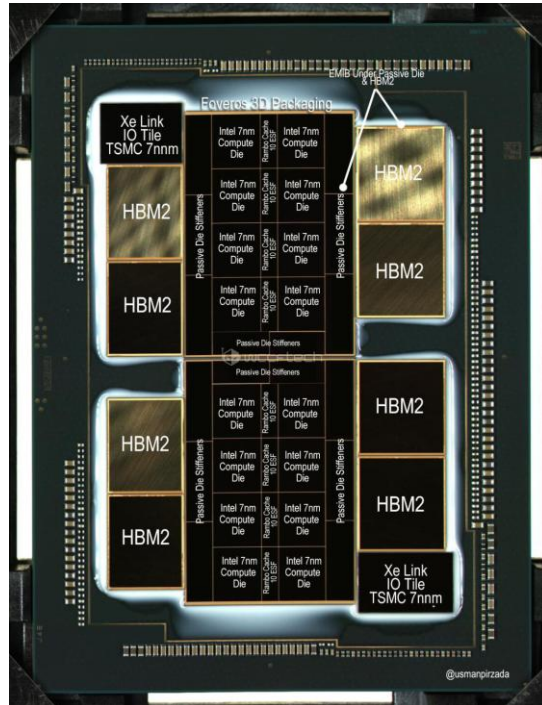
Advanced Packaging – 3D



Advanced Packaging - Intel's First 7nm GPU Xe HPC

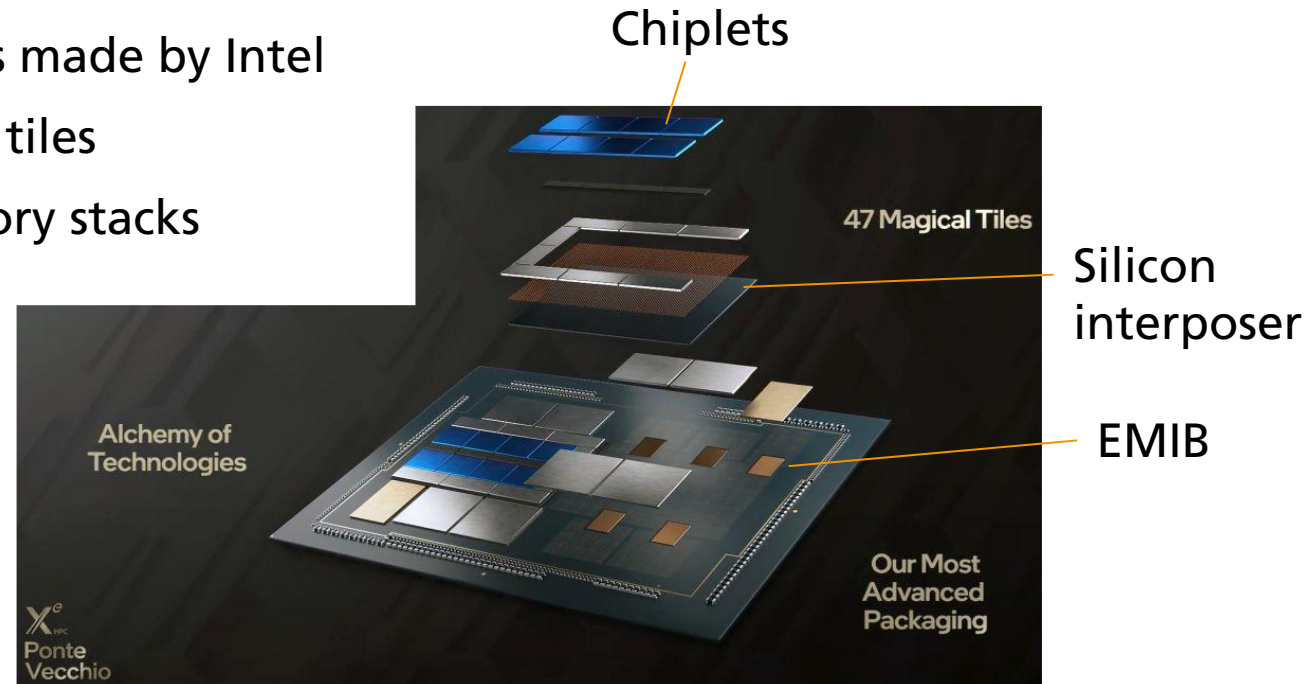
Intel's Xe HPC 2-tile (PVC) GPU uses a blend of Intel 7nm, Intel 10nm ESF, and TSMC 7nm process technology brought together by Foveros

- 2 base tiles
- 16 compute tiles
- 8 Rambo cache tiles
- 11 EMIB links made by Intel
- 2 Xe Link I/O tiles
- 8 HBM memory stacks

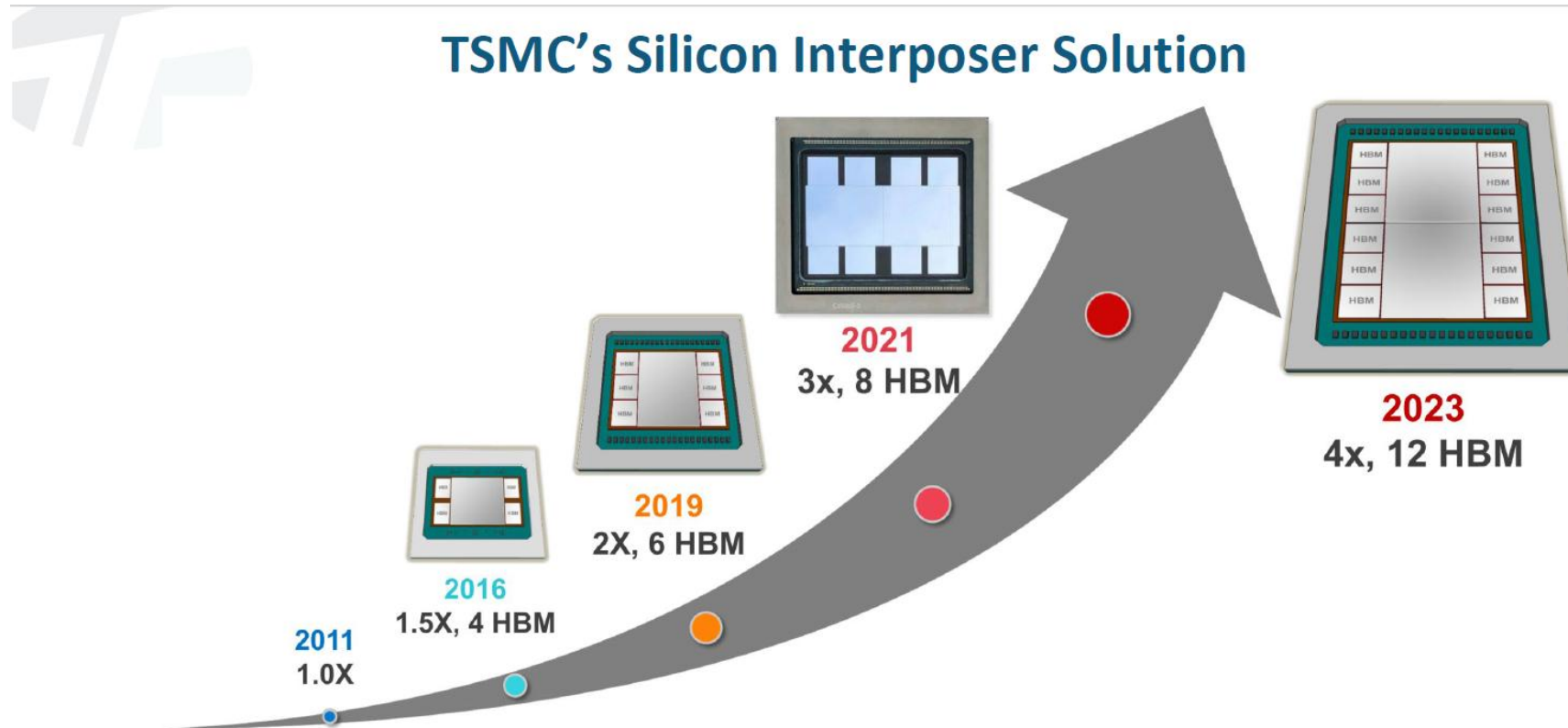


Decrease of latences based on interposer and micro bump interconnect!

<https://wccfttech.com/intel-7nm-xe-hpc-gpu-diagram-ponte-vecchio/>



MCMs with Interposers



- Applications include FPGA, GPU, AI accelerators
- Increasing size of interposer to support logic + multiple HBMs
 - Package body sizes of 65 mm x 65 mm, 75 mm x 75 mm, increasing to 100mm x 100mm body size
 - Silicon interposer provides highest density, but it is expensive!

techsearchinc.com

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Next trend ? - Multiple FO-Stacking

- Minimized signal influence by the interconnect of the stacks (small solder contact)

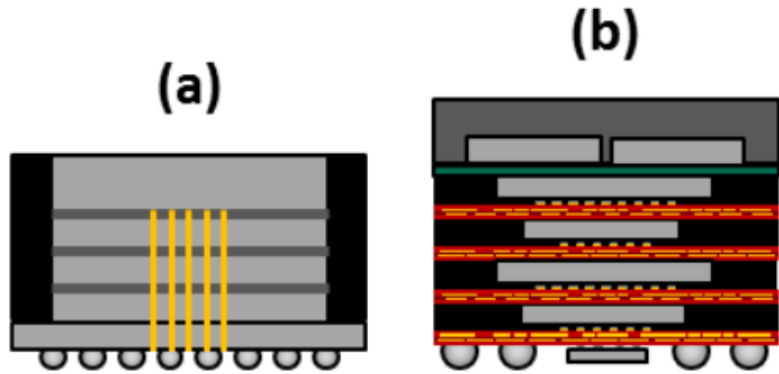
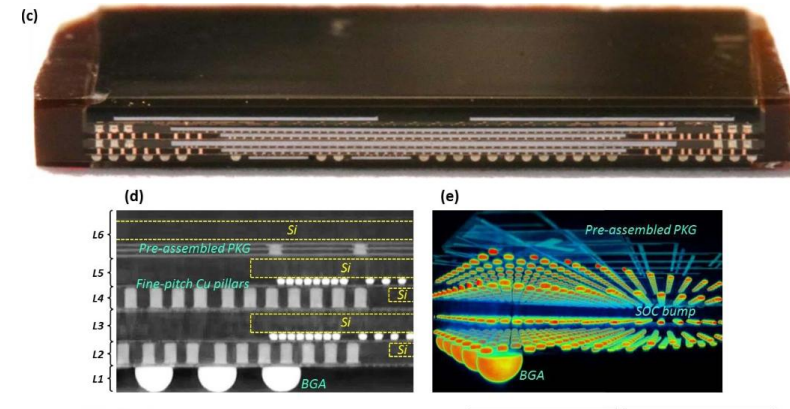


Figure 1. Multi-layer stacking sketches for heterogeneous integration of devices. Two representatives, arranged from left to right, are (a) 3D IC chip stacking through TSV and (b) 3D fan-out stacking. Note that the vertical interconnects for fan-out package in (b) are not particularly shown in the sketch.



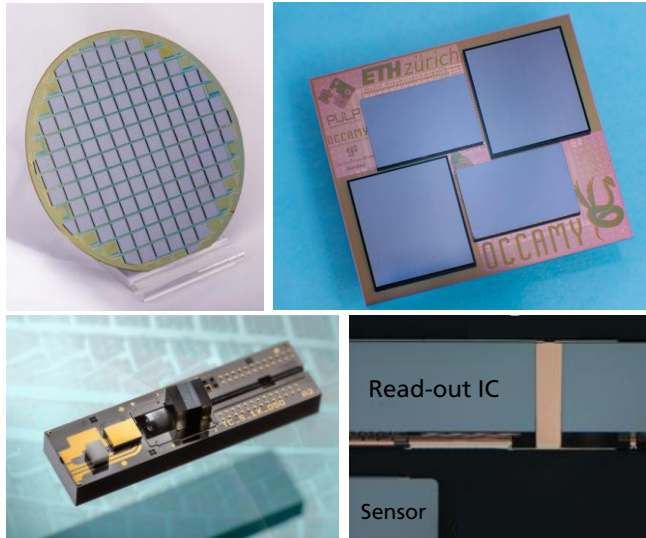
Source: TSMC, ECTC 2018

Interposer and Embedding Substrates

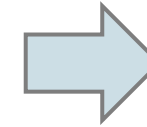
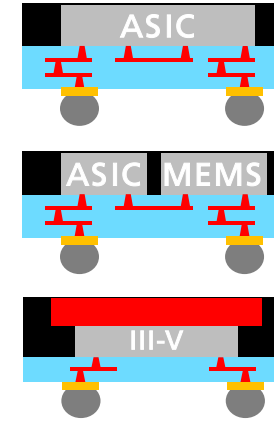
MATERIAL SELECTION

- Process ecosystem: via generation (etching, laser), passivation (CVD, polymer), electroplating, temporary carrier bonding, wafer thinning, wafer bonding
- Applied material compliments / enables functionality or robustness for specific applications (co-design)

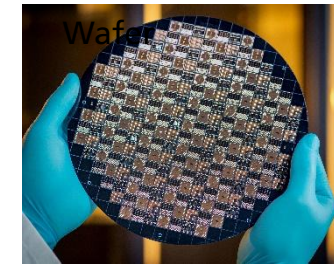
Silicon/SiC



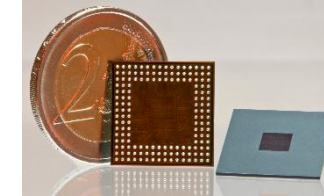
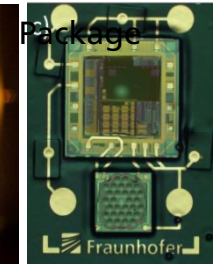
Epoxy Molding Compound



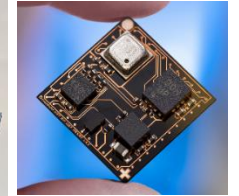
Multi Project



MEMS-

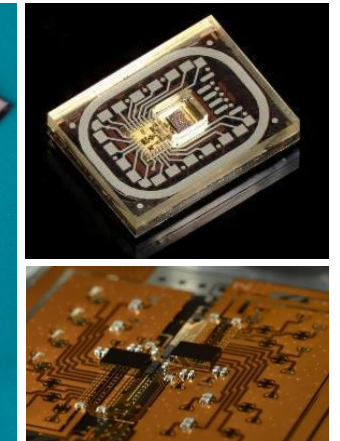
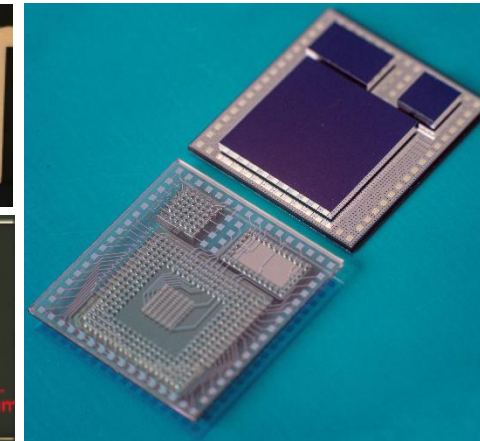
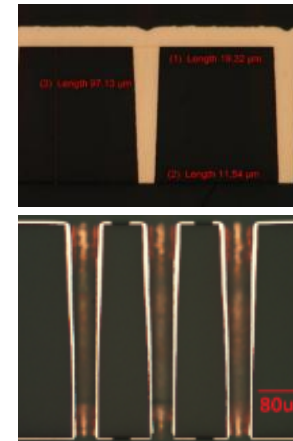


Package



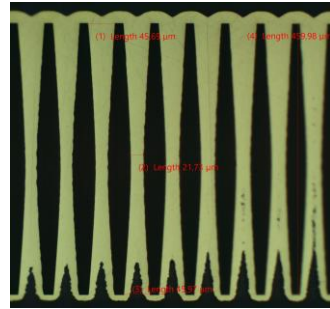
Package

Glass



Application adapted TGV metallization processes

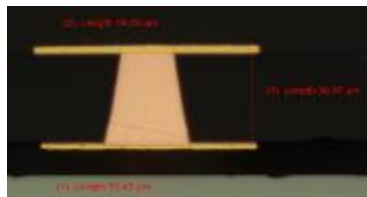
Complete via filling



450µm



100µm



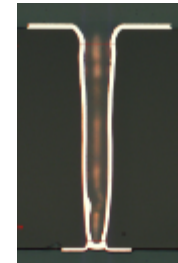
40µm

Hermetic filling

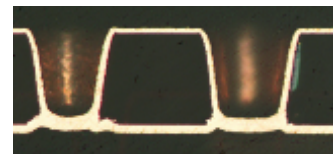
300µm



470µm



300µm



50µm

Conformal coating



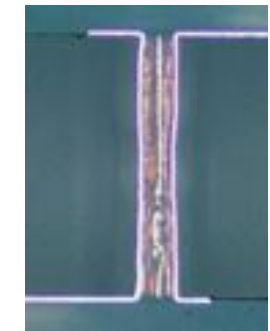
300µm



200µm



470µm



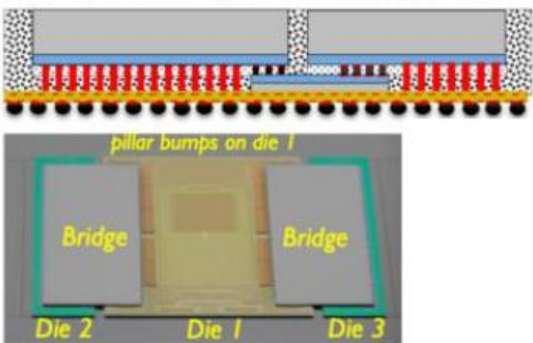
300µm

Aspect ratio / via size / substrate thickness

Cost / density

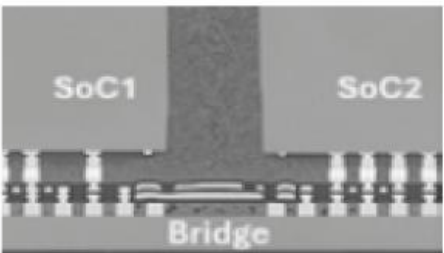
Chiplet – Bridges

Fan-out WLP with embedded Si-bridge interposer



Die placement and bridge bonding

Source: IMEC 2024



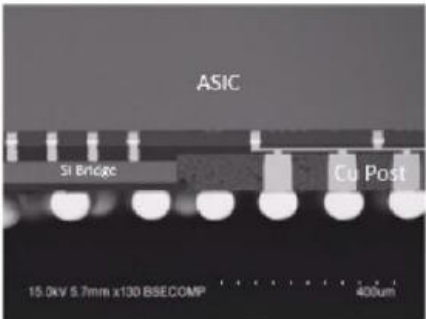
Source: ASE 2024



Figure 1: Schematic and cross-section of IBM's DBHi Si Bridge technology. (Courtesy of IBM)
Source: IBM



Source: TSMC 2022



Source: SPIL2020

Intel® Embedded Multi-Die Interconnect Bridge (EMIB)

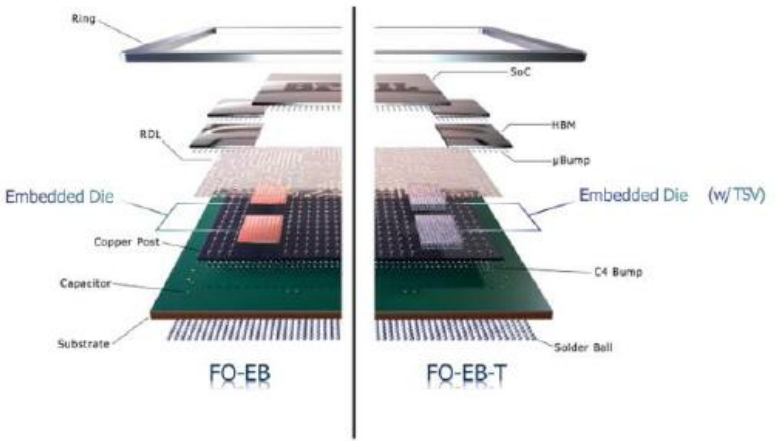
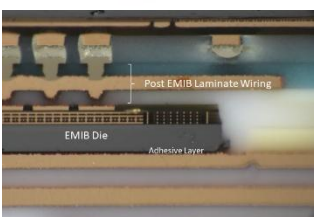
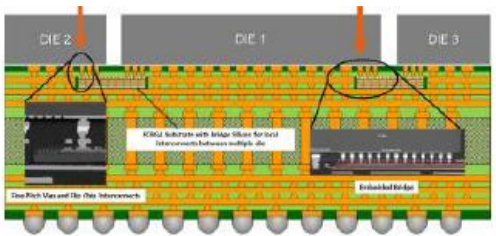


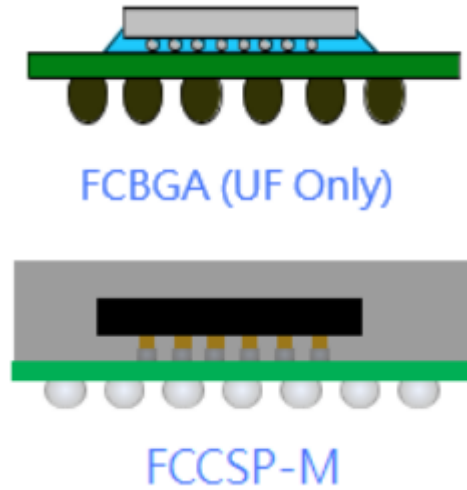
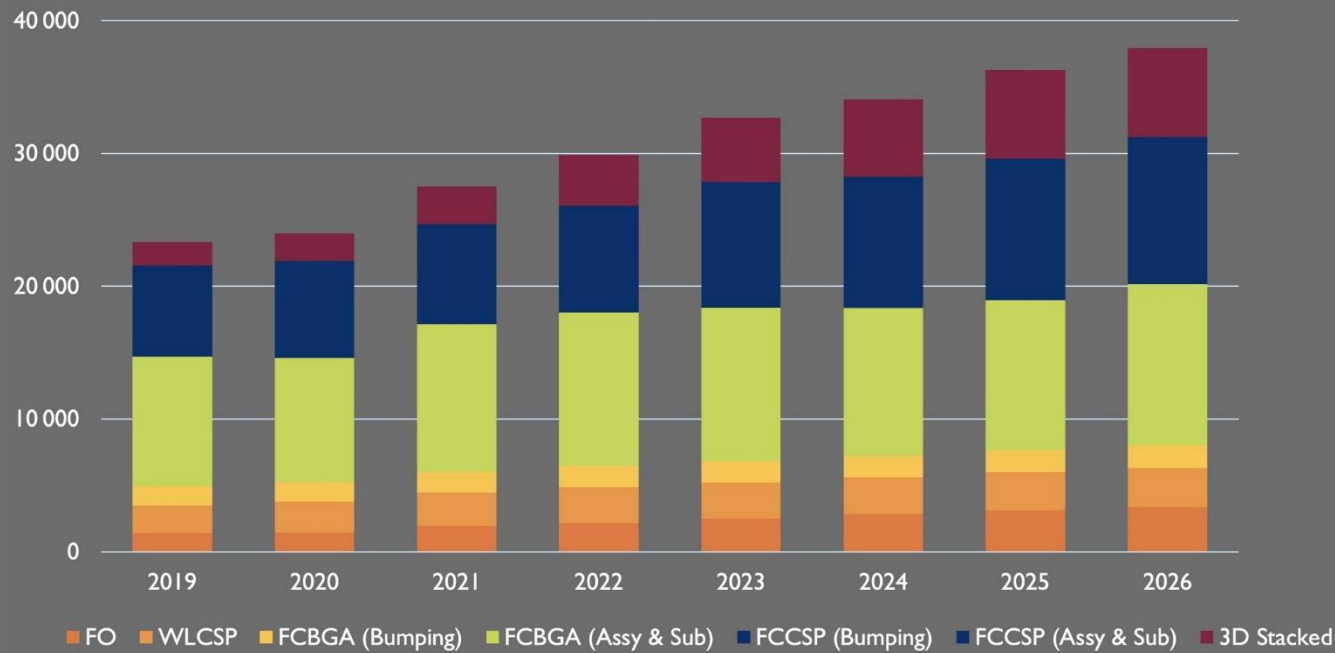
Fig.11: Advantage of FO-EB-T

Source: SPIL2024

Package Types

2020 – 2026 Total advanced packaging market – Revenues in US\$ million

(Source: Advanced Packaging Quarterly Market Monitor, Q1 2021, Yole Développement)

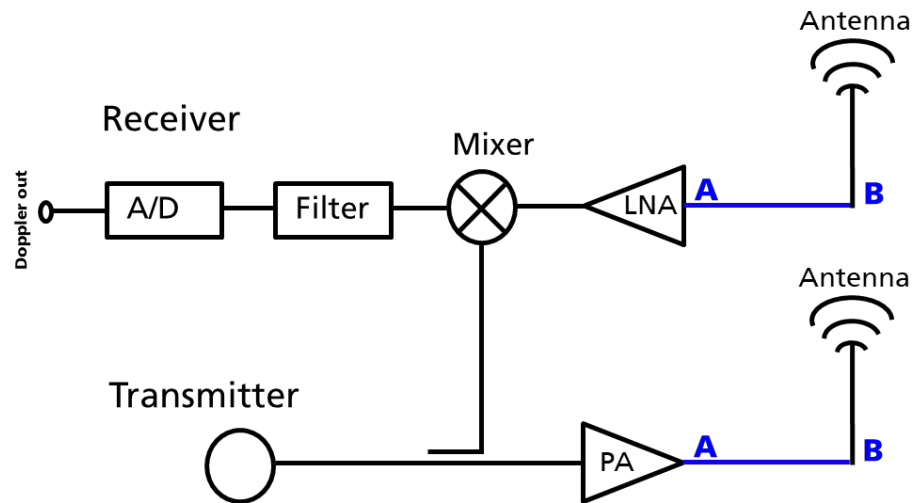


Requirements on Advanced Packages, Packaging Architectures and RF Design Considerations

Advanced Packages for **RF Applications** – Wireless Communication and Radar Applications

Requirements of Radar and Communication Systems on Packages – 1/3

- Signal-to-Noise Ratio (SNR) is the fundamental metric of radar that tells us the ability of a radar to reliably detect an object at a given distance away.
- **SNR** is directly proportional to the output power of the power amplifier (P_t), square of antenna gain (G) and inversely proportional to the total system losses (L)
- Packaging architecture, interconnects and materials have direct impact on P_t , G and L and thus on **SNR**



https://www.researchgate.net/figure/CW-radar-transceiver-block-diagram_fig2_253022485

$$SNR = \frac{P_t G^2 \lambda^2 \sigma}{(4\pi)^3 R^4 k T_s B_n L}$$

Requirements of Radar and Communication Systems on Packages – 2/3

■ Impact of Packaging on P_t

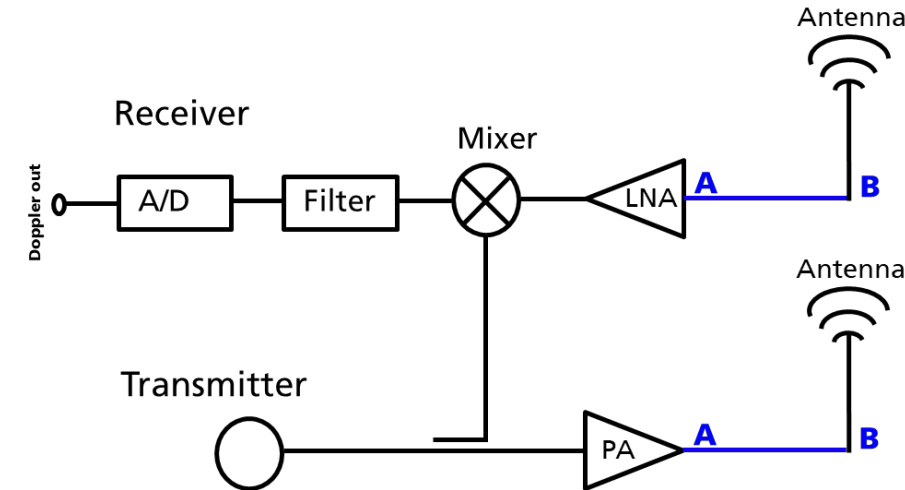
- P_t reduces with increased heat => Packaging architecture must ensure that heat generated by PA is properly conducted out of package, so as not to reduce P_t and SNR
- Parasitic inductance of packaging interconnects used to assembly amplifier reduces P_t

■ Impact of Packaging on G

- G depends on antenna efficiency, which inturn depends on packaging materials and interconnects used to develop antenna

■ Impact of Packaging on L

- Packaging architecture, materials and interconnects especially between A and B have severe impact on L

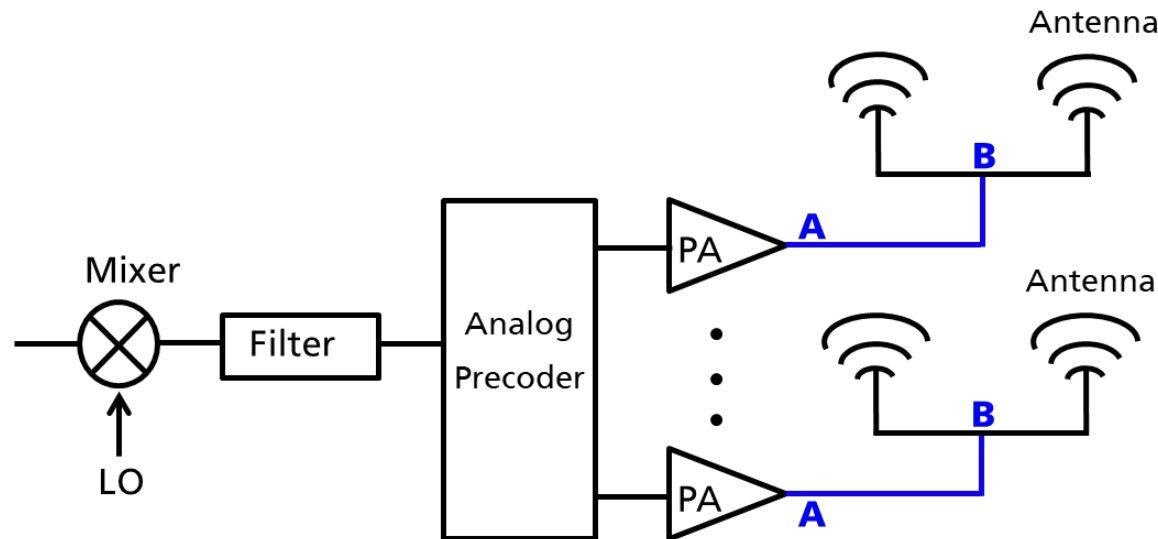


https://www.researchgate.net/figure/CW-radar-transceiver-block-diagram_fig2_253022485

$$G(\vartheta, \varphi) = D(\vartheta, \varphi) * e_{diel.} * e_{cond.} * e_{mat.}$$

Requirements of Radar and Communication Systems on Packages – 3/3

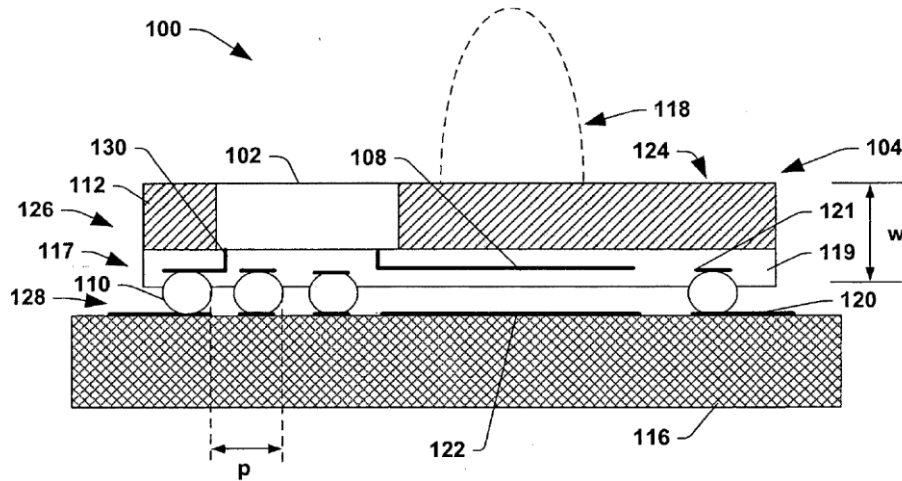
- **Equivalent Isotropic Radiated Power (EIRP)** of wireless communication systems tells us the „strength“ of the signal leaving the transmitter. It is key to determine the system performance
- **EIRP** increases with the output power of the power amplifier (P_t) and antenna gain (G), but reduces with the losses between amplifier and antenna (L)
- **Packaging architecture, interconnects and materials** have direct impact on P_t , G and L and thus on **EIRP**



https://www.researchgate.net/figure/CW-radar-transceiver-block-diagram_fig2_253022485

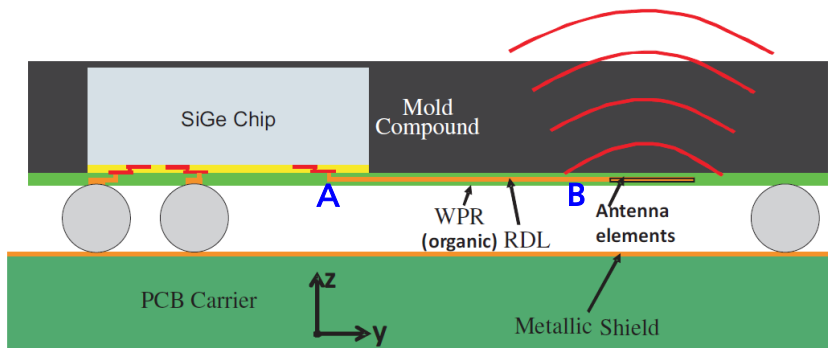
$$EIRP = P_t + G_{ant.} - L_{AB}$$

Ex.1: Fan-out Wafer Level Packages for RF: Embedding in Mold and Glass – 1/1



Infineon (Germany)
DE102010001407A1

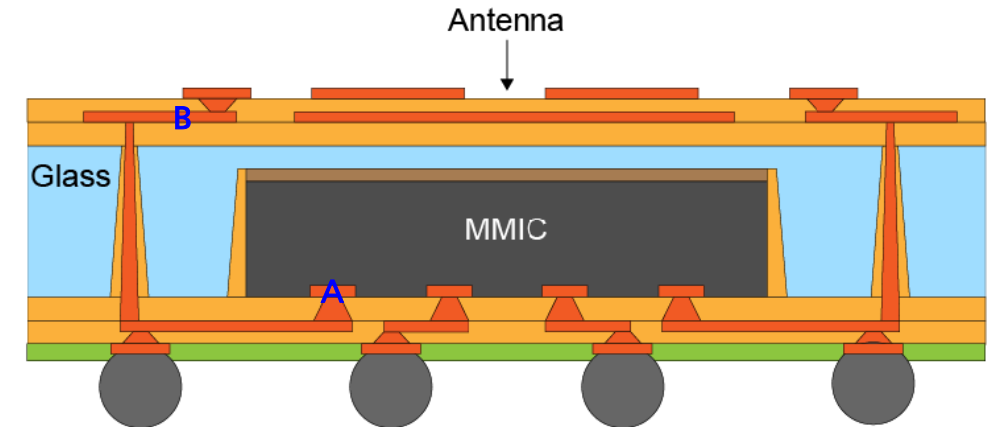
$$SNR = \frac{P_t G^2 \lambda^2 \sigma}{(4\pi)^3 R^4 k T_s B_n \mathbf{L}}$$



(b) An eWLB package with an antenna

Fig. 1: Antenna in eWLB package concept

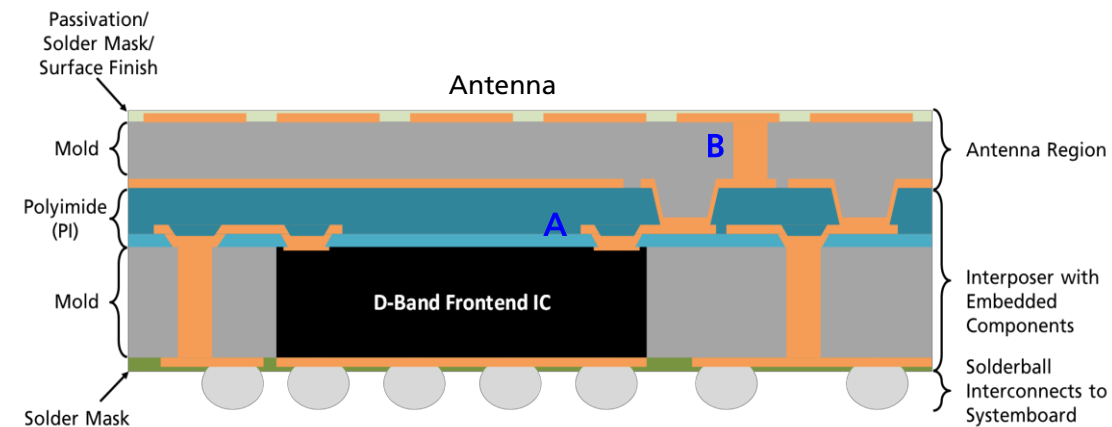
M. Al Henawy and M. Schneider, "Integrated antennas in eWLB packages for 77 GHz and 79 GHz automotive radar sensors," *2011 41st European Microwave Conference*, Manchester, UK, 2011, pp. 1312-1315



Georgia Tech (USA)

S. Erdogan et al., "Characterization of Chip-to-Package Interconnects for Glass Panel Embedding (GPE) for Sub-THz Wireless Communications," *2021 IEEE 71st Electronic Components and Technology Conference (ECTC)*, 2021, pp. 2328-2333,

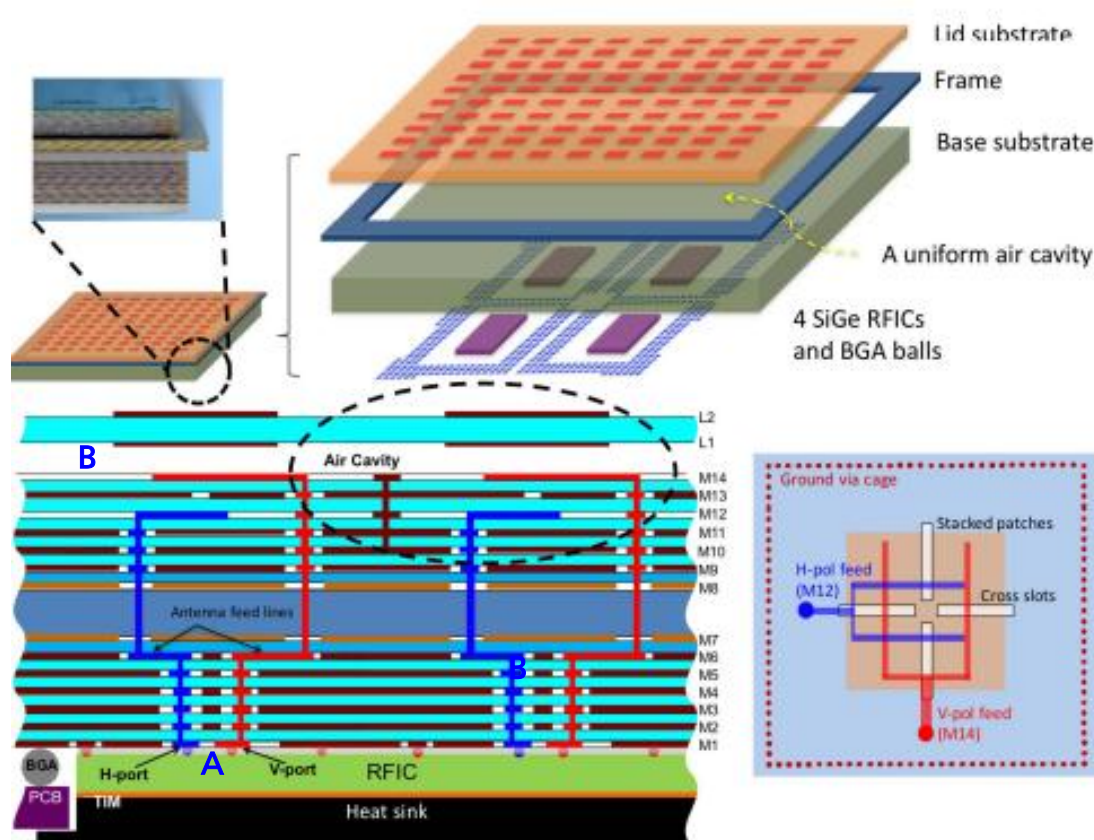
$$EIRP = P_t + G_{ant.} - L_{AB}$$



Fraunhofer IZM (Germany)

(US Patent: US10978778B2; EU Patent: EP3 346 493B1; German Patent: DE 10 2017 200 122 B4)

Ex.2: Organic Packages for RF: Multilayered Orangic and PCB Embedding – 1/1

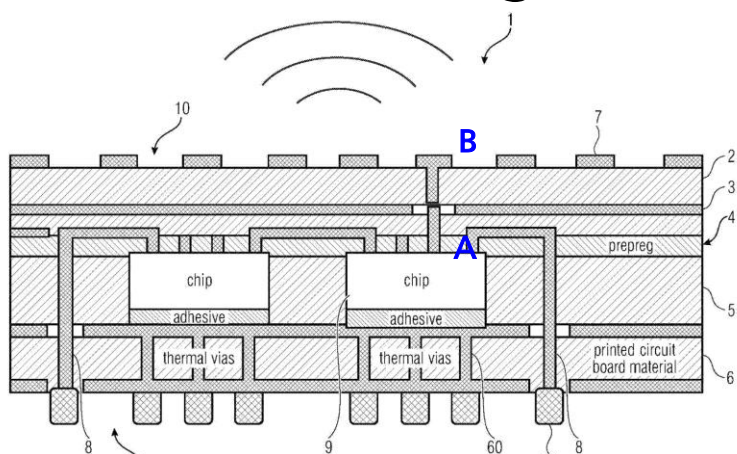


IBM (USA) – Flip-chip based ML Organic

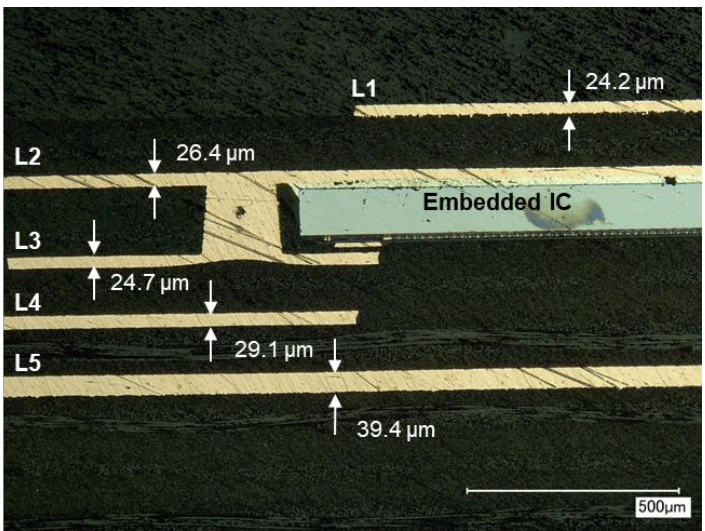
Xiaoxiong Gu et al., "Development, implementation, and characterization of a 64-element dual-polarized phased-array Antenna module for 28-GHz high-speed data communications", IEEE Transactions on MTT, vol. 67, no. 7, pp. 2975-2984, July 2019.

$$SNR = \frac{P_t G^2 \lambda^2 \sigma}{(4\pi)^3 R^4 k T_s B_n L}$$

$$EIRP = P_t + G_{ant.} - L_{AB}$$



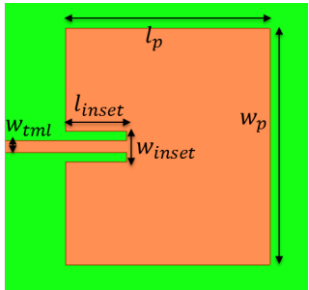
Fraunhofer IZM's (Germany) (US Patent: US11394109B2)



Cross-section of manufactured package at Fraunhofer IZM

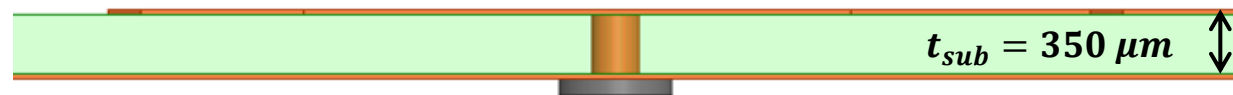
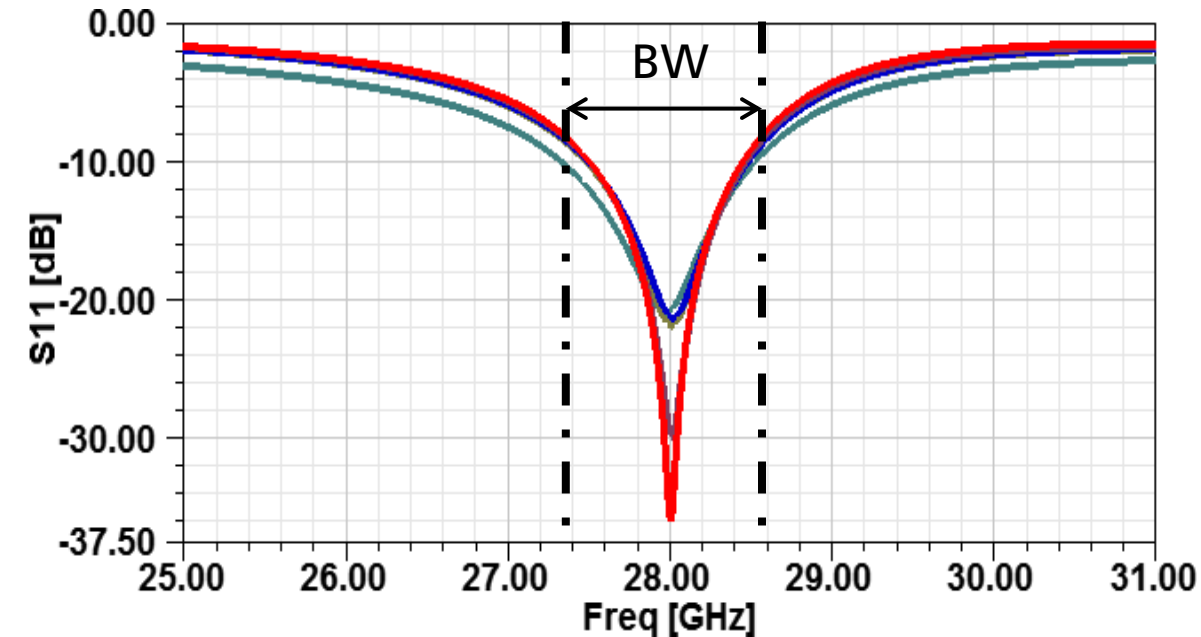
Impact of Packaging Materials on Antenna Gain, EIRP and SNR – 1/3

■ Example: Impact on 5G mmWave antennas



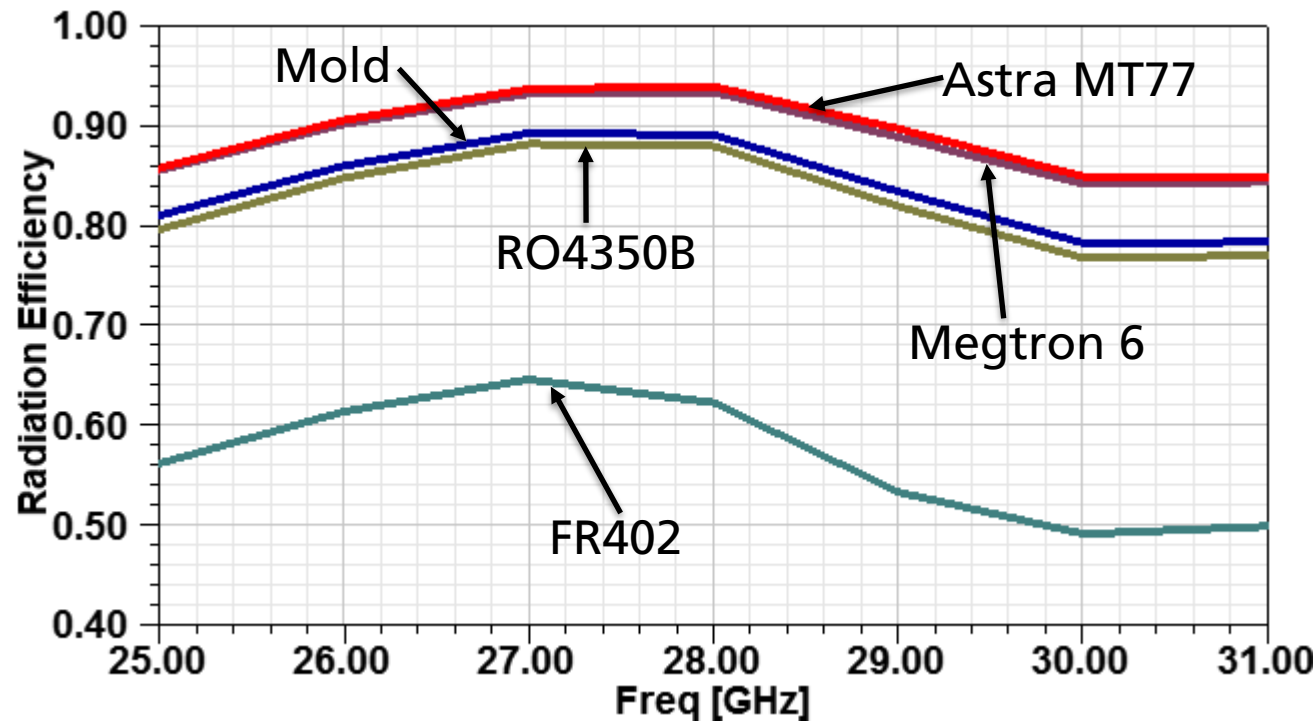
	$l_{aw} \times w_{aw} [\mu m]$
RO4350B	1800 X 520
Astra MT77	1900 X 520
Megtron 6	1850 X 520
Mold	1800 X 520
FR402	1700 X 520

	DK	DF
RO4350B	3.66	0.004
Astra MT77	3	0.0017
Megtron 6	3.35	0.002
Mold	3.65	0.0035
FR402	4.3	0.015



Impact of Packaging Materials on Antenna Gain, EIRP and SNR – 2/3

■ Example: Impact on 5G mmWave antennas



	DK	DF
RO4350B	3.66	0.004
Astra MT77	3	0.0017
Megtron 6	3.35	0.002
Mold	3.65	0.0035
FR402	4.3	0.015

Substrat	Peak Gain [dB]
RO4350B	12.17
Astra MT77	12.64
Megtron 6	12.45
Mold	12.23
FR4	10.7

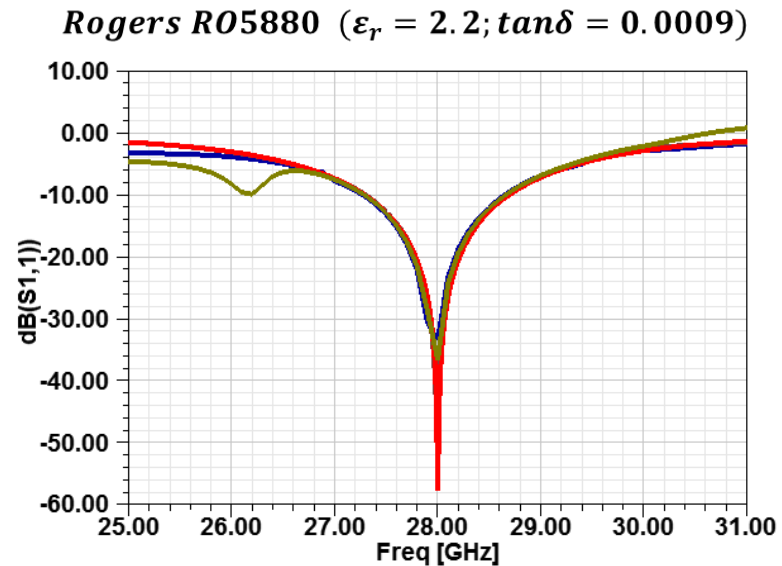
$$G(\vartheta, \varphi) = D(\vartheta, \varphi) * e_{diel.} * e_{cond.} * e_{mat.}$$

$$SNR = \frac{P_t G^2 \lambda^2 \sigma}{(4\pi)^3 R^4 k T_s B_n L}$$

$$EIRP = P_t + G_{ant.} - L_{AB}$$

Impact of Packaging Materials on Antenna Gain, EIRP and SNR – 3/3

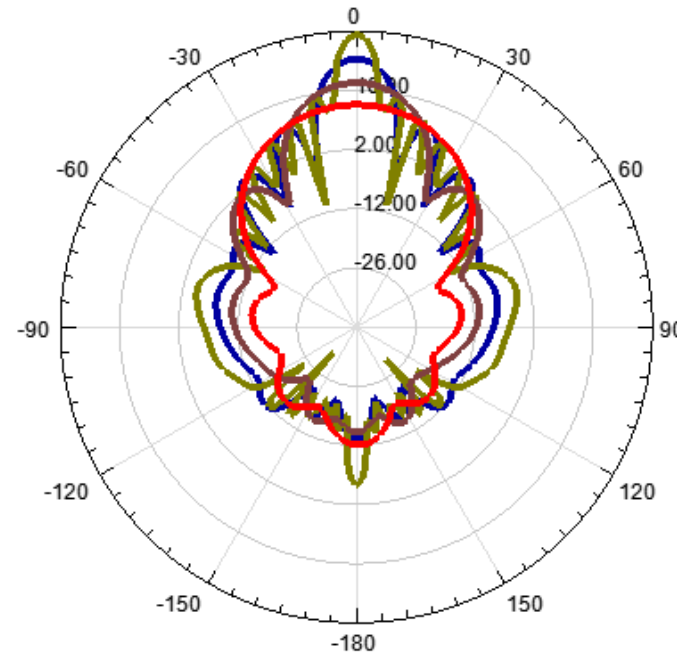
■ Example: Impact on 5G mmWave antennas



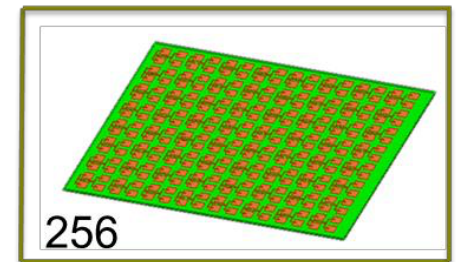
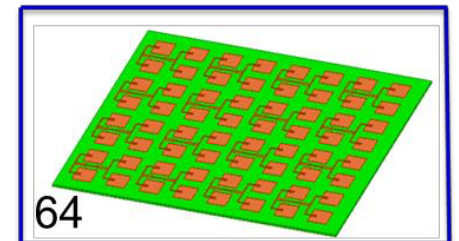
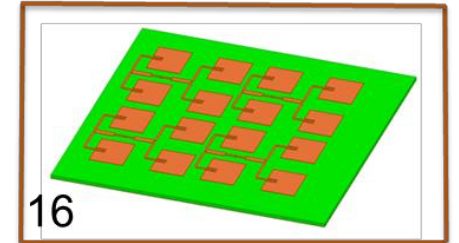
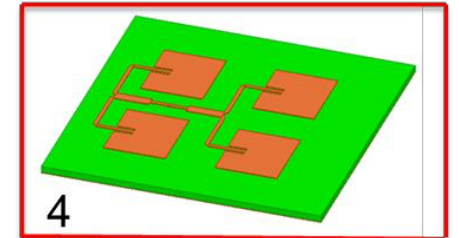
# of Elements	Gain	Beam Width
4	12.6 dBi	42°
16	17.8 dBi	24°
64	23.4 dBi	12°
256	29.4 dBi	6°

$$SNR = \frac{P_t G^2 \lambda^2 \sigma}{(4\pi)^3 R^4 k T_s B_n L}$$

$$EIRP = P_t + G_{ant.} - L_{AB}$$

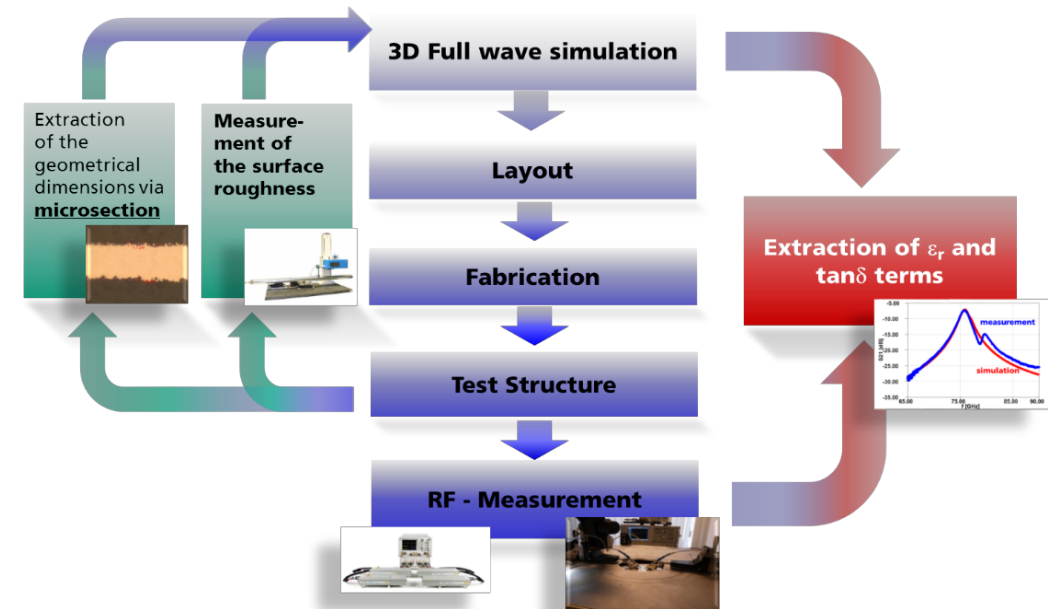
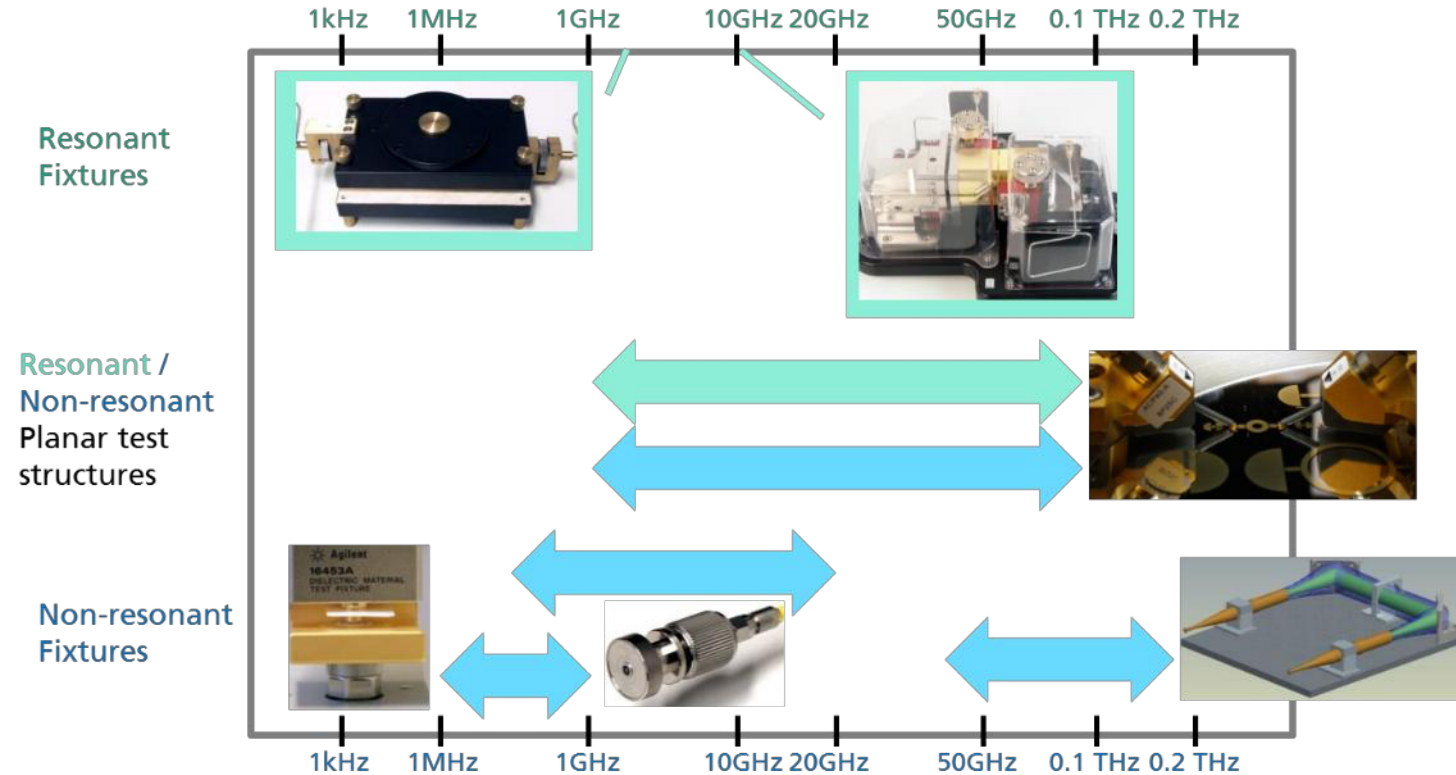


# of Elements	Substrate length	Substrate width
4	15.04 mm	15.02 mm
16	27.1 mm	27.2 mm
64	50.5 mm	48.3 mm
256	94.7 mm	92.9 mm



Characterization of Packaging Materials for RF & High-Speed Applications – 1/4

■ Measurement Methods for RF Characterization of Packaging Materials @ IZM

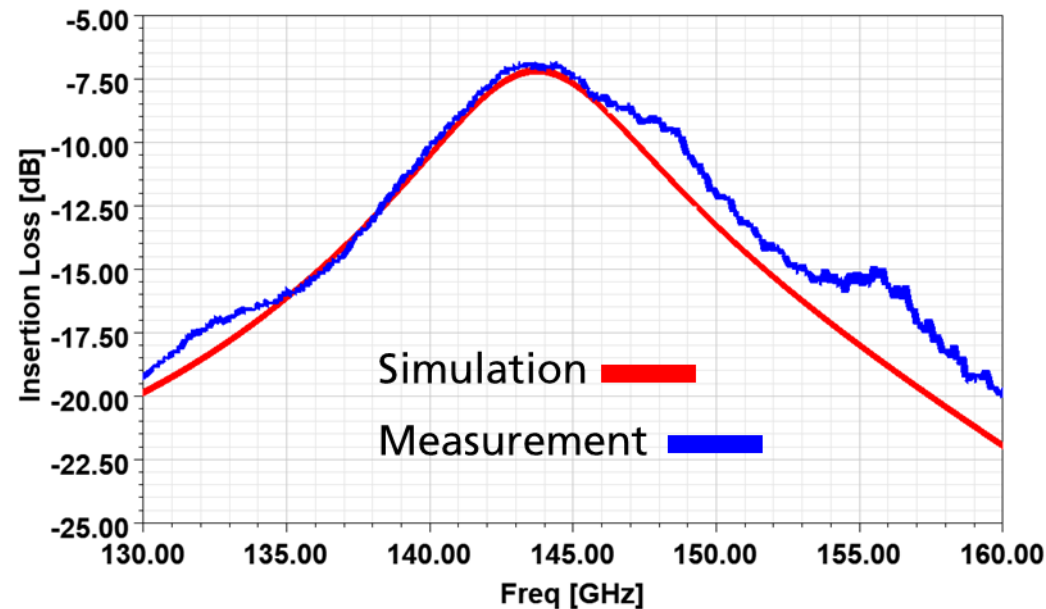


RF Material Characterization Approach @ IZM

Adapted from „Measuring Dielectric Properties using Agilent’s Materials Measurement Solutions“, Agilent Application Note 5991-2171

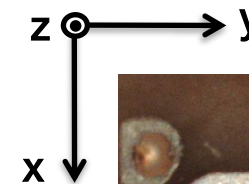
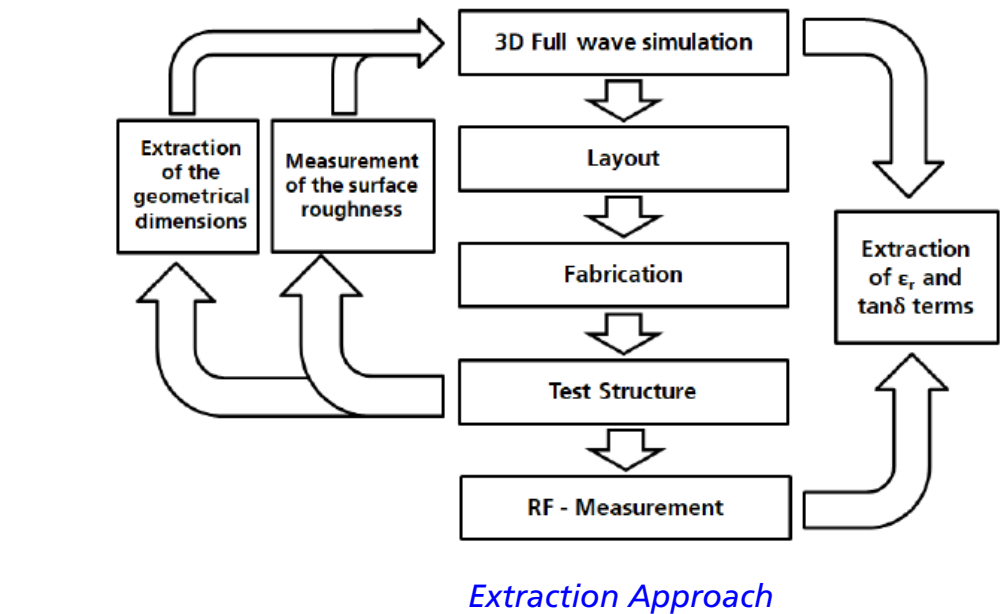
Characterization of Packaging Materials for RF & High-Speed Applications – 2/4

■ Method 1: Planar Resonators



Extracted material properties of
Isola's Astra MT77 @ 140 GHz

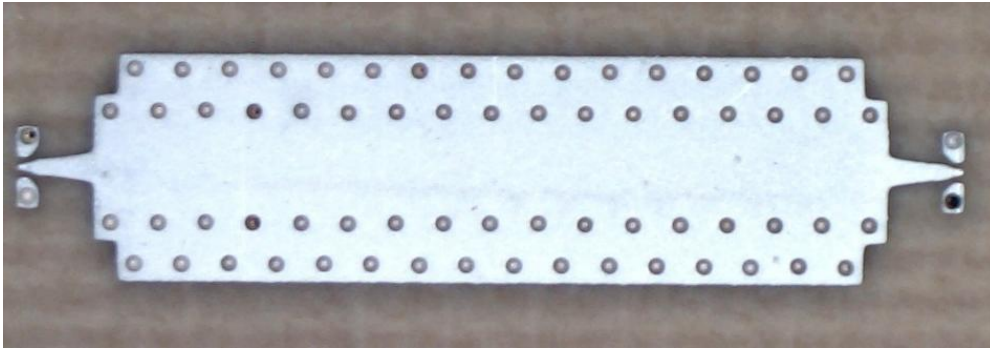
- Dielectric constant, $\epsilon_r = 3.06$
- Dissipation factor, $\tan\delta = 0.008$



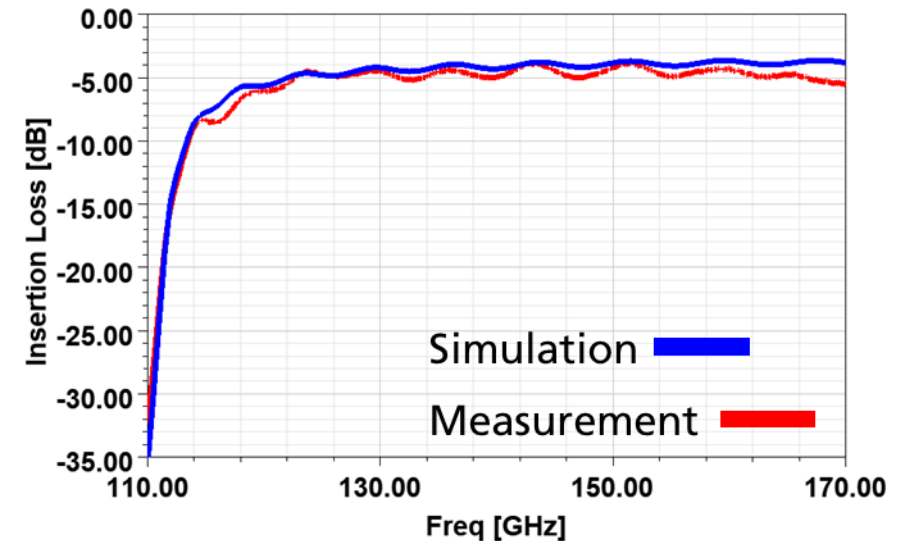
Resonator Manufactured at IZM

Characterization of Packaging Materials for RF & High-Speed Applications – 3/4

■ Method 2: Substrate Integrated Waveguide (SIW)

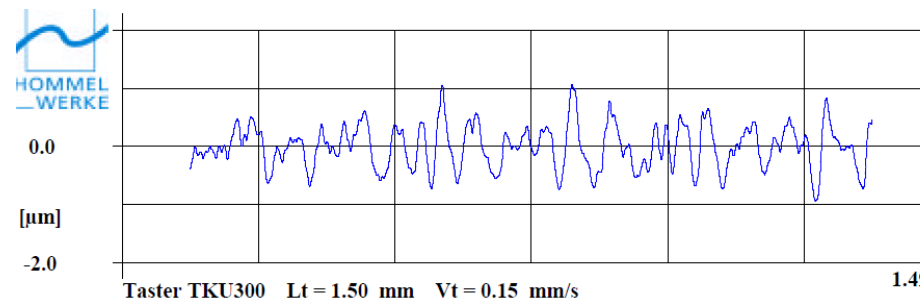


Substrate Integrated Waveguide Manufactured at IZM



Extracted material properties of
Isola's Astra MT77 @ 140 GHz

- Dielectric constant, $\epsilon_r = 3.05$
- Dissipation factor, $\tan\delta = 0.0078$



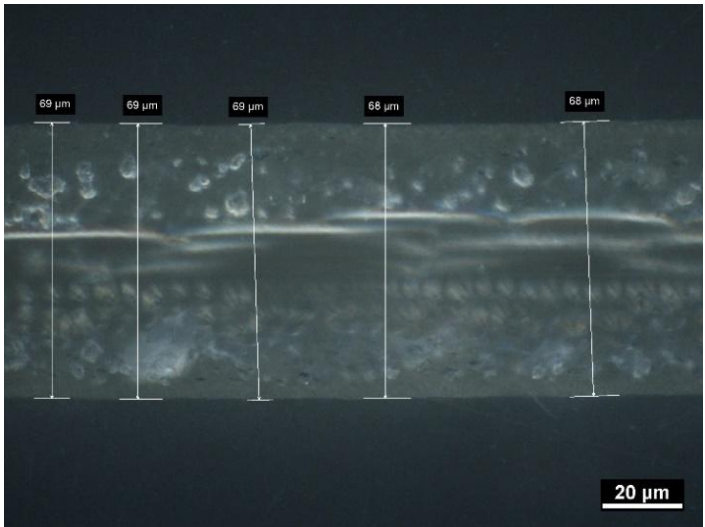
R-Profil

Ra	0.30 µm
Rz	1.63 µm
Rmax	1.82 µm
Rt	2.02 µm
Rq	0.38 µm

Roughness Profile & Applied Rq-Value

Characterization of Packaging Materials for RF & High-Speed Applications – 4/4

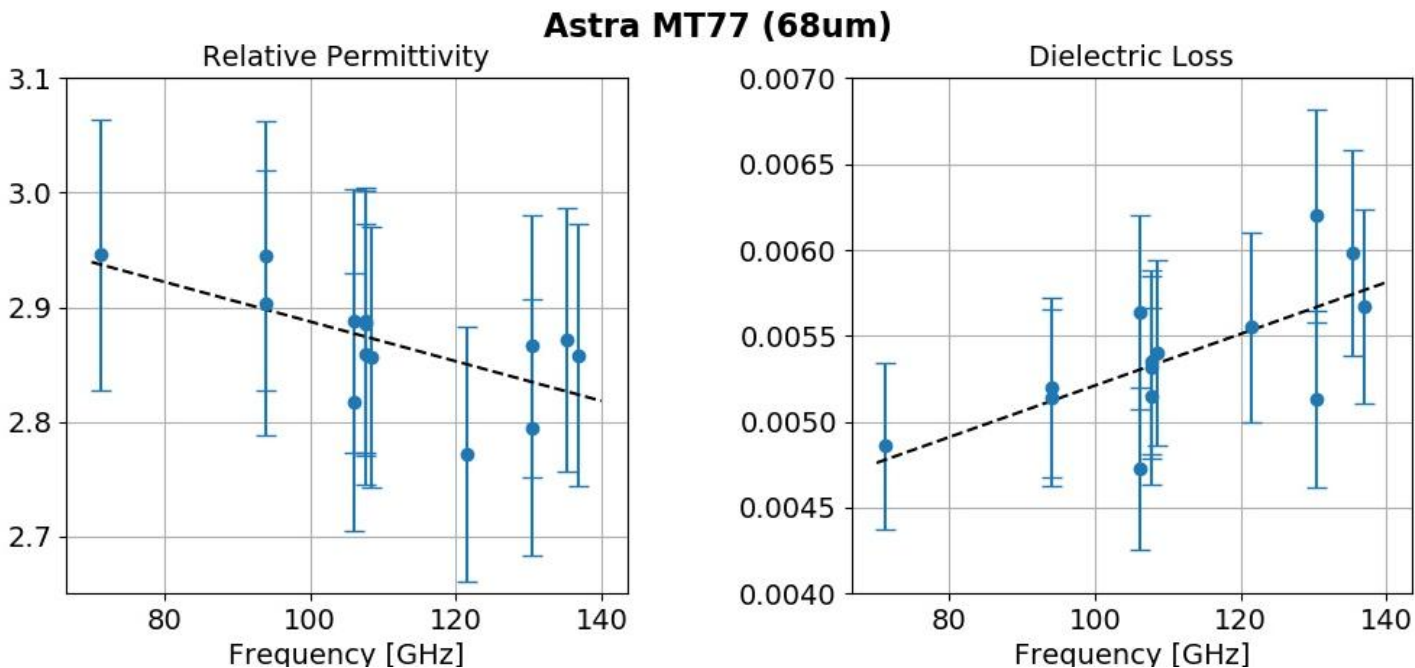
■ Method 3: Fabry Pérot Resonator (Non-metallized Substrate)



Cross Sectional View – Astra MT77 68 μm



Fabry Pérot Resonator



Frequency (GHz)	70	80	90	100	110	120	130	140
DK	2.94	2.92	2.90	2.89	2.87	2.85	2.84	2.82
DF (10^{-3})	4.8	4.9	5.1	5.2	5.4	5.5	5.7	5.8

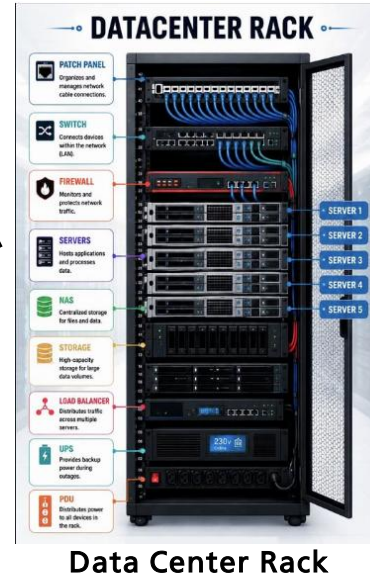
Advanced Packages for High-Performance Computing (**HPC**) and **AI** Applications

2.5D Packages for HPC & AI – 1/4

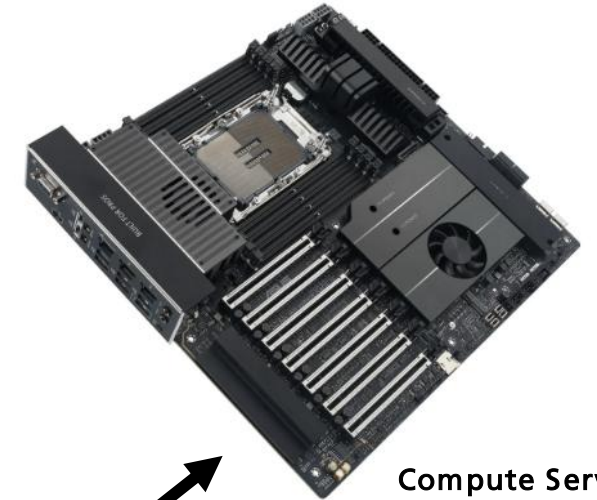
Data Center



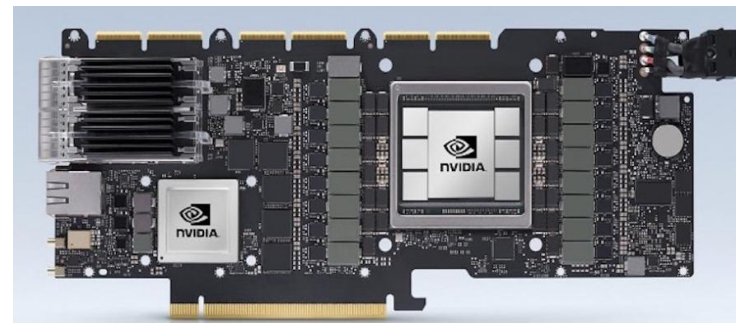
<https://www.ibm.com/think/topics/ai-data-center>



<https://www.facebook.com/netwithisrar/posts/data-center-rack-explained-behind-every-reliable-application-website-and-busines/122185703744923044/>



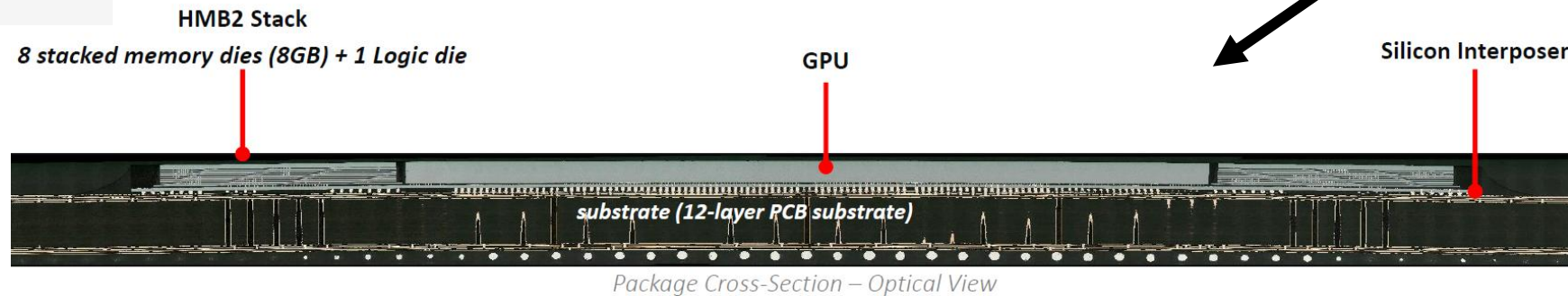
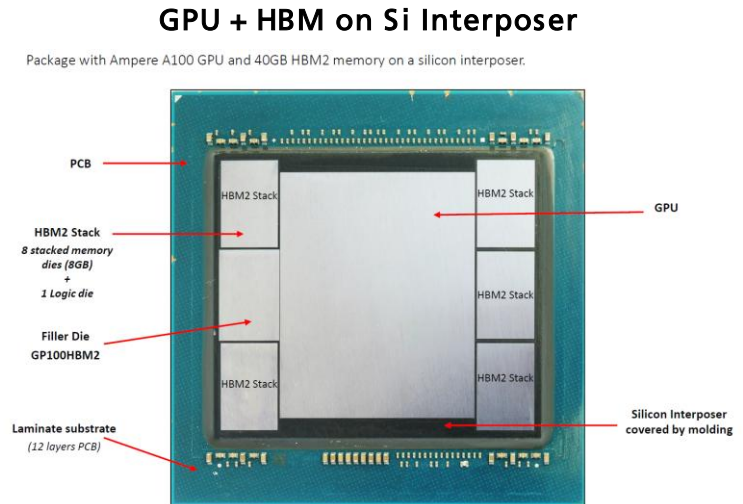
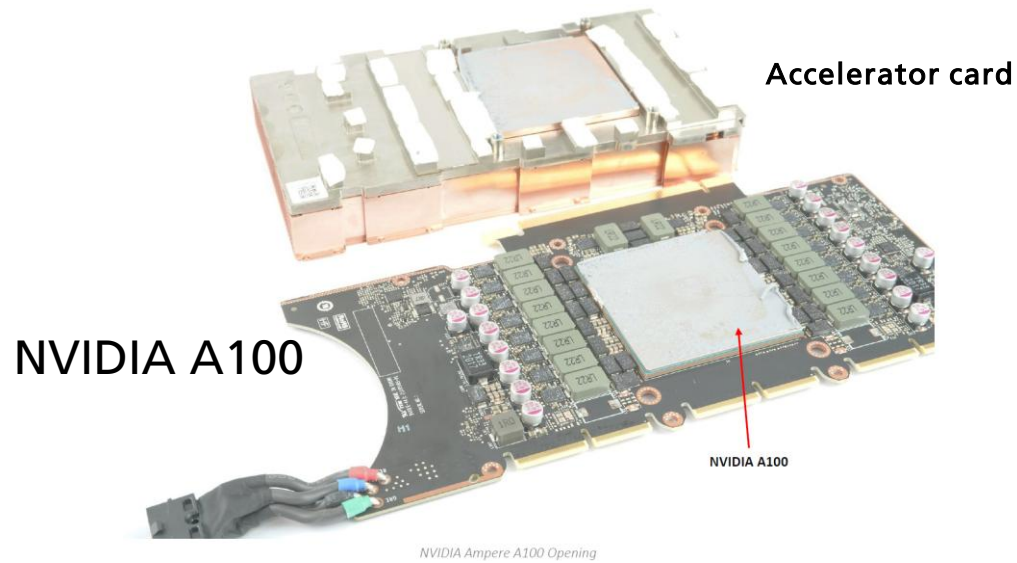
Compute Server



Accelerator card

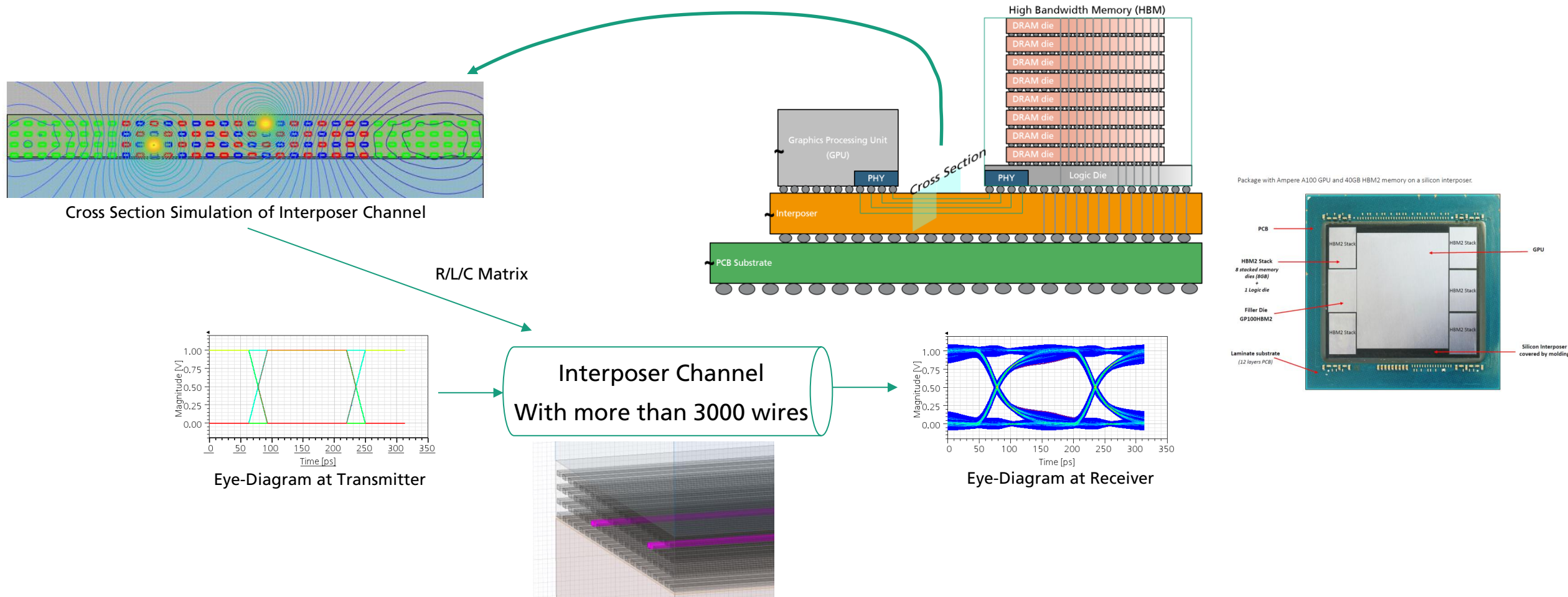
<https://developer.nvidia.com/blog/accelerating-data-center-ai-with-the-nvidia-converged-accelerator-developer-kit/>

2.5D Packages for HPC & AI – 2/4



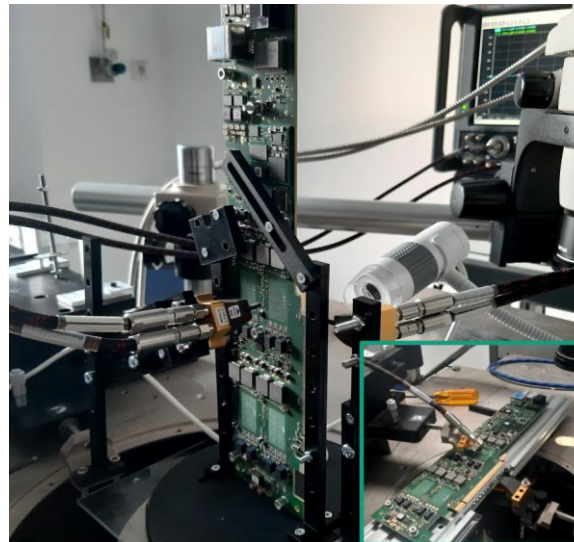
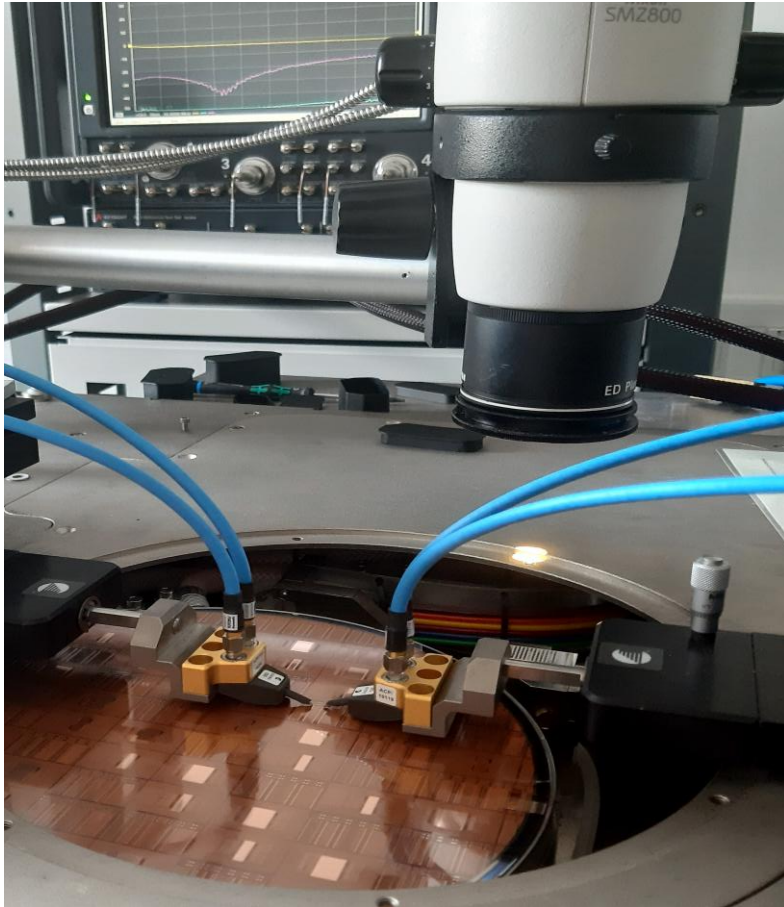
2.5D Packages for HPC & AI – 3/4

■ Signal & Power Integrity Design of Chiplets for Accelerator Cards at IZM

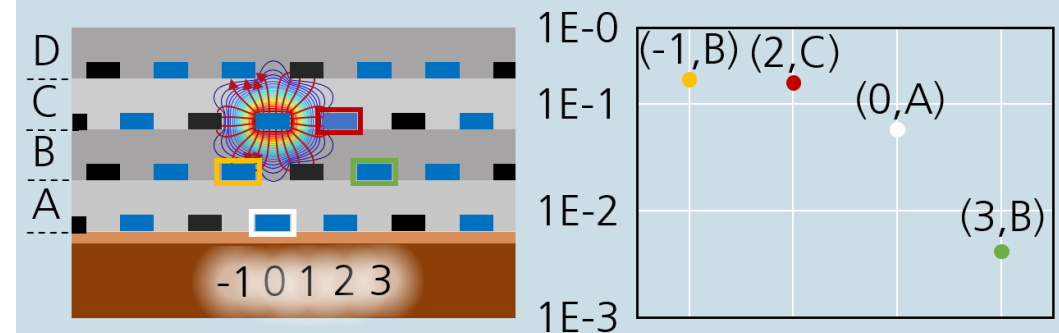
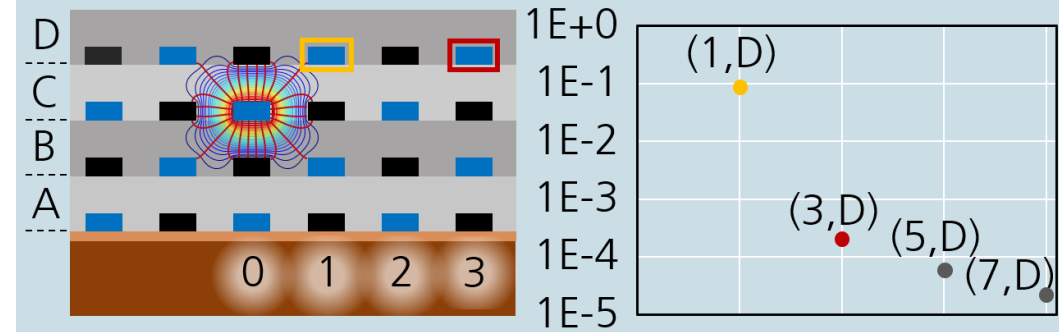


2.5D Packages for HPC & AI – 4/4

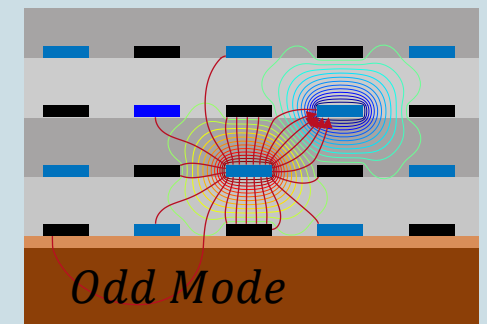
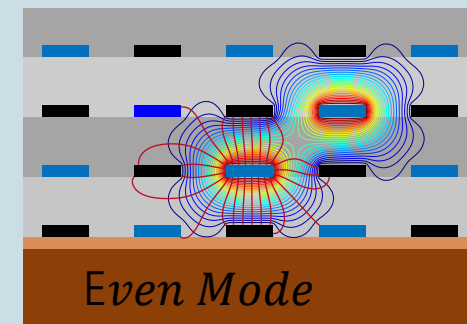
■ Design & Test of Chiplets at IZM



(0,C) Coupling Factors K_m to Neighbours

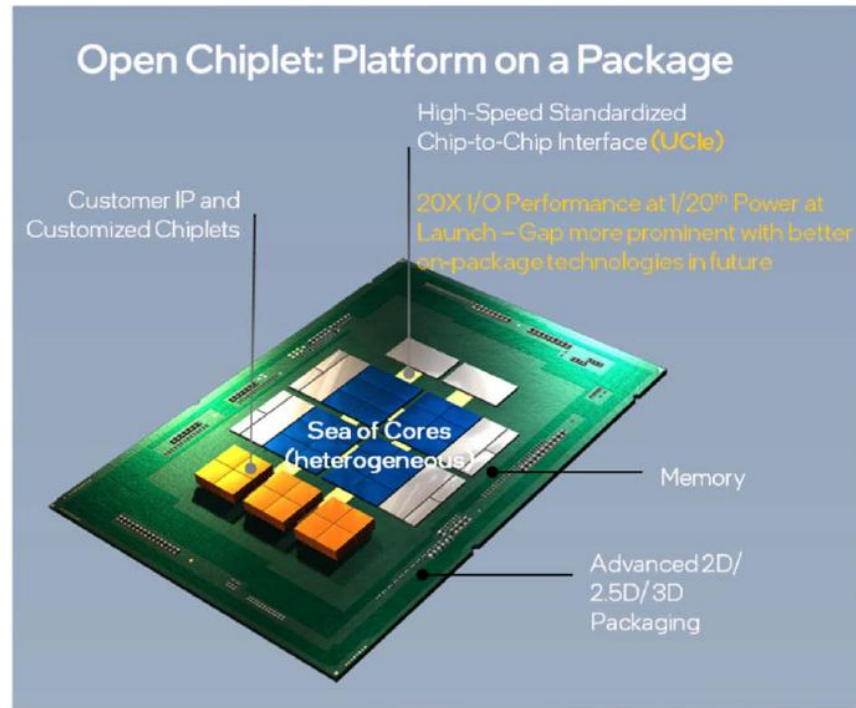


■ Signal Line ■ Polyimid ■ Silicon
■ Ground Line ■ Silicodioxide

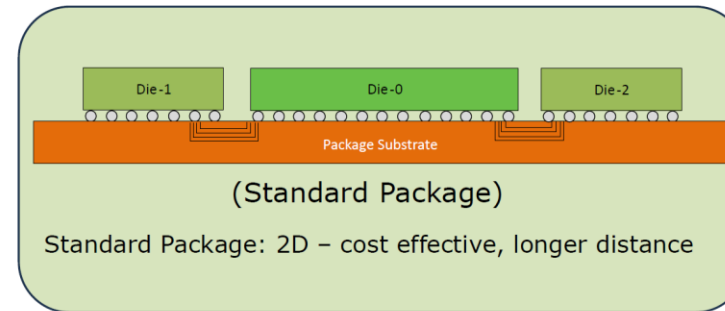


UCIe – 1/2

Universal Chiplet Interconnect Express (UCIe): open industry standard interconnect for developing an open chiplet ecosystem, where chiplets from any supplier can be packaged anywhere in an interoperable manner.

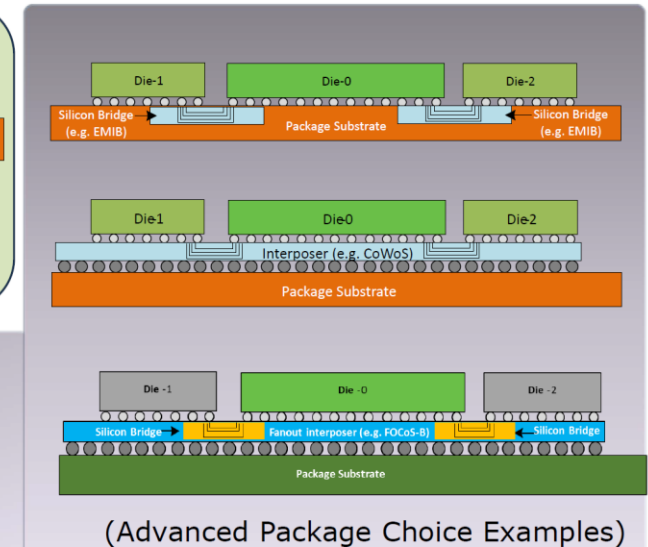


UCIe 1.0: Supports Standard and Advanced Packages



Advanced Packages: 2.5D – power-efficient, high bandwidth density

Dies can be manufactured anywhere and assembled anywhere – can mix 2D and 2.5D in same package – Flexibility for SoC designer



One UCIe 1.0 spec supports **different flavors** of packaging options to build an open ecosystem

Property of Universal Chiplet Interconnect Express™ (UCIe™) 2024

UCIe – 2/2

Key Metrics: Expanding Industry Leading KPIs to UCIe-3D

Characteristics / KPIs	UCIe-S (2D)	UCIe-A (2.5D)	UCIe 3D	Comments for UCIe 3D
Characteristics				
Data Rate (GT/s)	4, 8, 12, 16, 24, 32		Up to 4	= SoC Logic frequency – power efficiency is critical
Width (each cluster)	16	64	80	Options or reduced width to 70, 60...
Bump Pitch (µm)	100 – 130	25 – 55	≤ 10 (optimized) > 10 – 25 (functional)	Must scale so that UCIe-3D fits within the bump area, must support hybrid bonding
Channel Reach (mm)	≤ 25	≤ 2	3D vertical	FtF bonding initially; FtB, BtB, multi-stack possible
Target for Key Metrics				
BW Shoreline (GB/s/mm)	28 – 224	165 – 1317	N/A (vertical)	
BW Density (GB/s/mm ²)	22 – 125	188 – 1350	4,000 – 300,000	4TB/s/mm ² @ 9µm, ~12TB/s/mm ² @ 5µm, ~35T/s/mm ² @ 3µm, ~300T/s/mm ² @ 1 µm
Power Efficiency Target (pJ/b)	0.5	0.25	<0.05 at 9µm -> 0.01 at 1 µm	Conservatively estimated at 9µm pitch <0.02 for 3µm pitch
Low-Power Entry/Exit	0.5nS ≤ 16G, 0.5-1nS ≥ 24G		0nS	No preamble or post-amble
Reliability (FIT)	0 < FIT (Failure in Time) << 1		0 < FIT << 1	BER < 1E-27
ESD	30V CDM		5V CDM → ≤ 3V	5V CDM at introduction, no ESD for W2W hybrid bonding possible

UCIe-3D will deliver compelling power-efficient performance



Property of Universal Chiplet Interconnect Express™ (UCIe™) 2024

Summary

Advanced packages, substrates and interposers will continue to play a key role in the functionality, cost and reliability of emerging and future components, modules and systems for RF, wireless, high-speed digital communication, sensing and computing applications

Questions & Feedback