

Improving Thermal Management in 3D packaging via Bulk and Interfacial Heat Transport



❖ Joana Mendes – Diamond heat spreaders and related applications

- Diamond: What & Why?
- Integrating Diamond in Advanced Packages
- Liquid Cooling with Diamond
- Challenges & Mitigation Strategies



❖ Christo Bojkov – Thermal Interface Materials Review

- TIM definitions, TIM1/TIM 1.5/TIM2 used cases
- Material performance vs requirements
- Application criteria, Metrology and Reliability
- Future products roadmaps: 2025-2030

Thermal Management in Advanced Package Designs: The Role of TIMs and Diamond Heat Spreaders



Joana Catarina Mendes is a Researcher at the Institute for Telecommunications, Aveiro, Portugal. Her research focuses on integrating synthetic diamond into advanced packages for thermal management, addressing the challenges of high-power density in AI, HPC, and RF systems. Dr. Mendes has led and contributed to multiple international R&D projects, has over 60 peer-reviewed publications, and serves on the Steering Committee of the Workshop on Compound Semiconductor Devices and Integrated Circuits held in Europe (WOCSDICE). She chaired the 2023 and 2024 editions of the IEEE Signal and Power Integrity Workshop and is a member of the Assembly & Manufacturing Technology sub-committee of the IEEE Electronic Components and Technology Conference (ECTC).

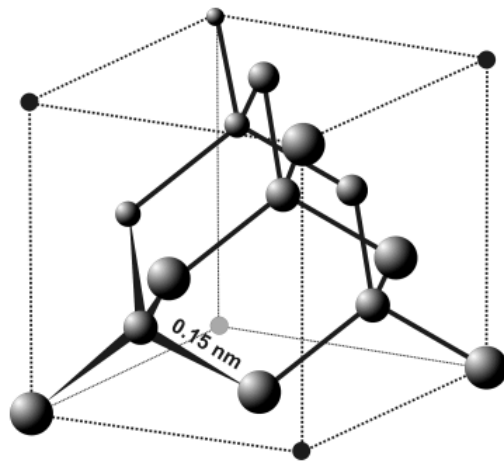


Christo Bojkov has over 36 years of experience in the semiconductor industry as Eng. Director and Senior Technical STAFF at multiple leading Integrated Device Manufacturers (IDM). He has managed large engineering groups in the Front End of line (FEOL) and back end of line (BEOL) Fabrication facilities with focus on heterogeneous integration of Cu interconnects, Cu-CMP, Pb-free Flip Chip, Cu- pillars with Cu-RDL, CSP Assembly and Test for high-power high-frequency GaN & GaAs mmWave products. Christo began his career as a Research Fellow at the Universities of Paris (France), Rome (Italy) and at the Max-Planck Institute (Germany). He provides leadership activities currently as active committee member at IMAPS and at IEEE/ECTC and as Adj. faculty at UT-Dallas.

1. Diamond: What & Why?

What is Diamond?

- “**Diamond** is a solid form of the element carbon (C) with its atoms arranged in a crystal structure called diamond cubic” (Wikipedia).
- The atom C has four valence electrons → each atom is covalently bonded to other four C atoms via sp^3 hybrid orbitals.
- C atomic radius is very small radius (C → $0.67\text{\AA}$; Si → $1.11\text{\AA}$) → covalent bonds between neighboring atoms are very strong and give diamond a set of extreme properties.

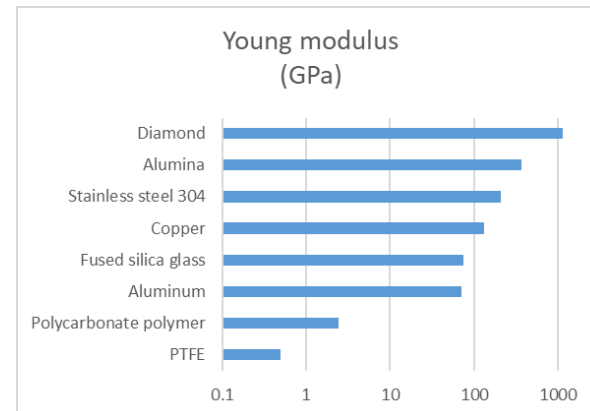
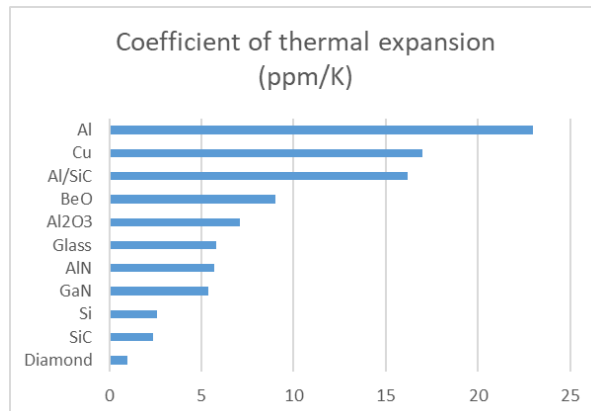
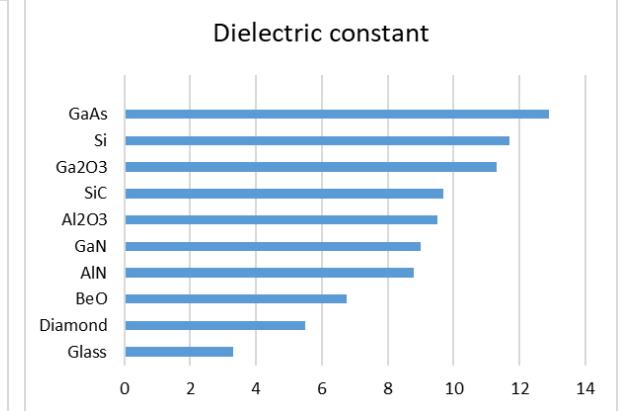
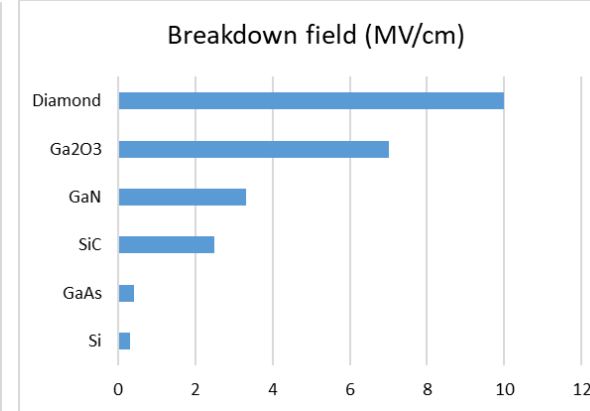
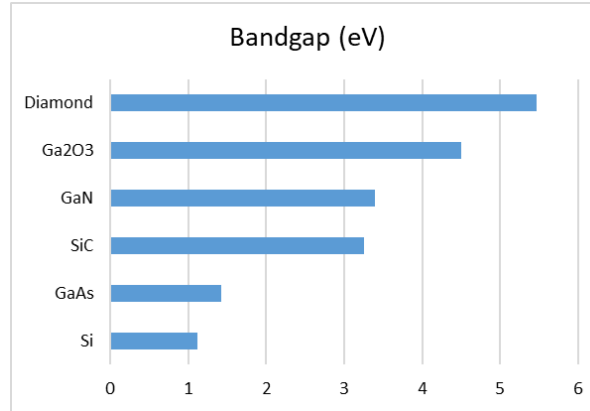
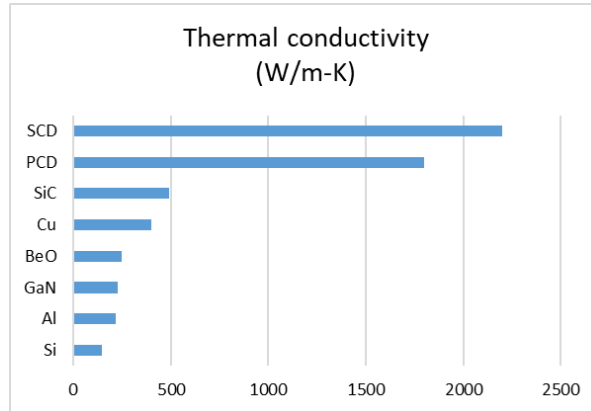


Diamond unit cell.

The Periodic Table

1 H																	2 He
3 Li	4 Be											5 B	6 C	7 N	8 O	9 F	10 Ne
11 Na	12 Mg											13 Al	14 Si	15 P	16 S	17 Cl	18 Ar
19 K	20 Ca	21 Sc	22 Ti	23 V	24 Cr	25 Mn	26 Fe	27 Co	28 Ni	29 Cu	30 Zn	31 Ga	32 Ge	33 As	34 Se	35 Br	36 Kr
37 Rb	38 Sr	39 Y	40 Zr	41 Nb	42 Mo	43 Tc	44 Ru	45 Rh	46 Pd	47 Ag	48 Cd	49 In	50 Sn	51 Sb	52 Te	53 I	54 Xe
55 Cs	56 Ba	57-71	72 Hf	73 Ta	74 W	75 Re	76 Os	77 Ir	78 Pt	79 Au	80 Hg	81 Tl	82 Pb	83 Bi	84 Po	85 At	86 Rn
87 Fr	88 Ra	89-103	104 Rf	105 Db	106 Sg	107 Bh	108 Hs	109 Mt	110 Ds	111 Rg	112 Cn	113 Uut	114 Fl	115 Uup	116 Lv	117 Uus	118 Uuo
		57 La	58 Ce	59 Pr	60 Nd	61 Pm	62 Sm	63 Eu	64 Gd	65 Tb	66 Dy	67 Ho	68 Er	69 Tm	70 Yb	71 Lu	
		89 Ac	90 Th	91 Pa	92 U	93 Np	94 Pu	95 Am	96 Cm	97 Bk	98 Cf	99 Es	100 Fm	101 Md	102 No	103 Lr	

Diamond Properties

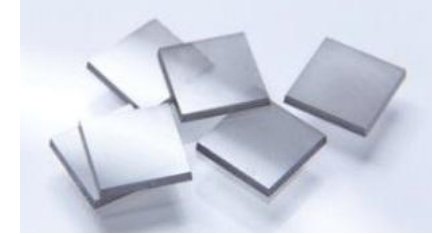
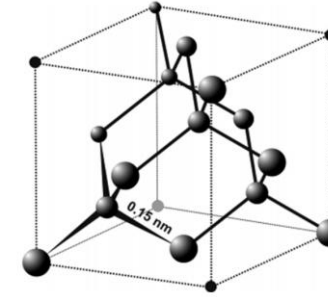


- 😊 Excellent thermal conductor + electrical insulator.
- 😊 Low parasitic capacitance + low electrical cross-talk.
- 😊 Low CTE (coefficient of thermal expansion) → smaller thermal mismatch than with Cu or Al.
- 😞 Very high Young modulus → thermal mismatch poses additional stress to TIM layers.

Types of Diamond: Pros and Cons

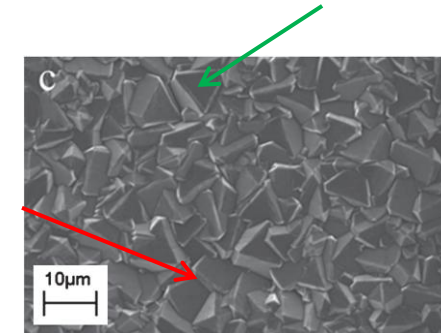
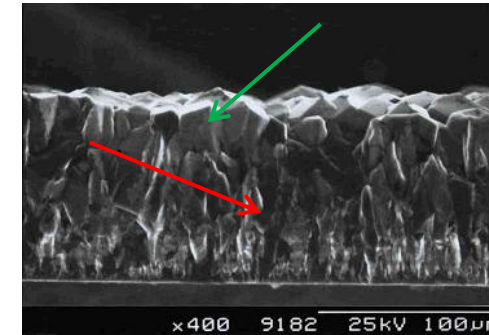
Single-crystal diamond (SCD):

- ➡ Perfect crystalline structure.
- ➡ Thermal conductivity up to 2200 W/m-K.
- ➡ Routinely available in sizes up to 10×10 mm² (HPHT); 2 and 4-inch reported (mosaic CVD).



Polycrystalline diamond (PCD):

- ➡ Polycrystalline structure, with diamond grains connected via grain boundaries (graphite, amorphous carbon, etc).
- ➡ Phonons are scattered by the grain boundaries, decreasing the thermal conductivity.
- ➡ Depending on grain/grain boundaries (sp³/non-sp³) ratio the thermal conductivity may vary between 1000-1800 W/m-K.
- ➡ Routinely available in 4-inch size; 8-inch has also been reported.

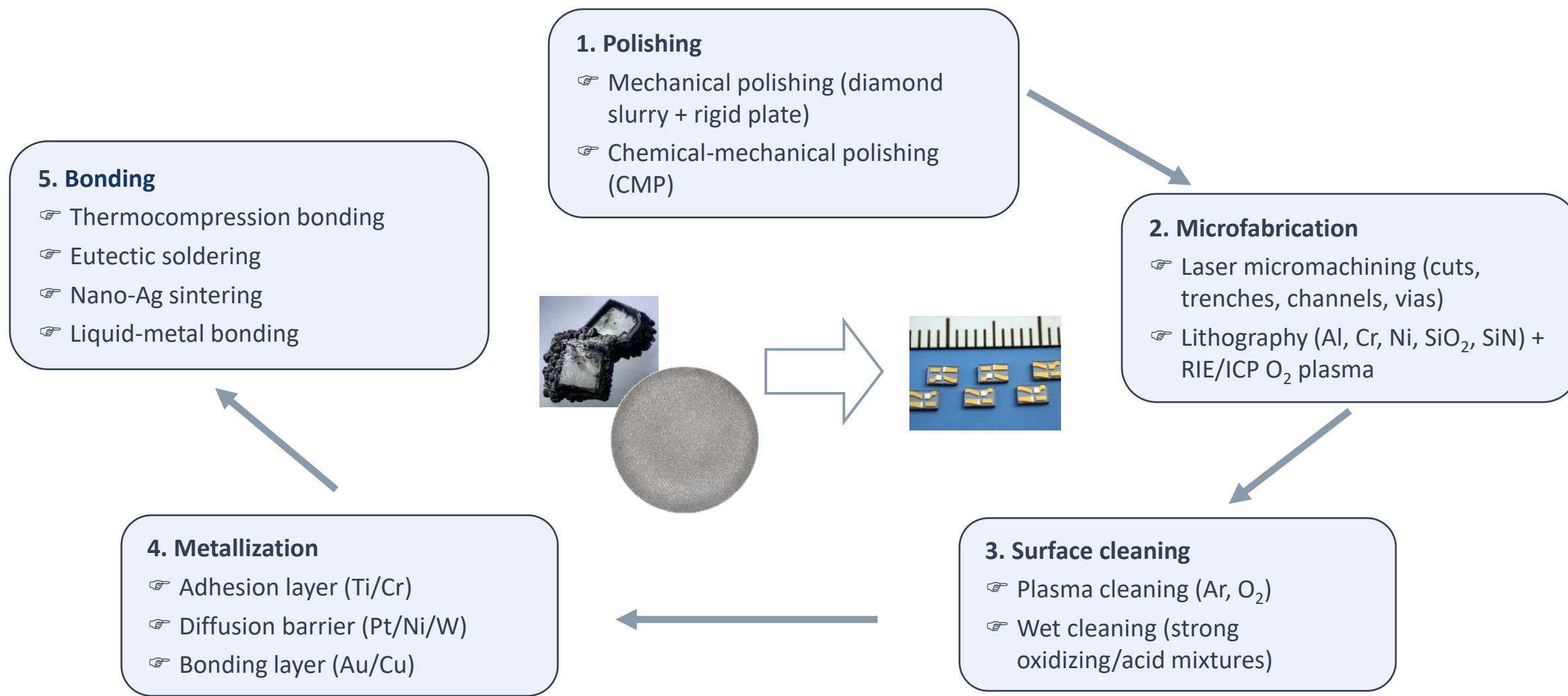


SCD and PCD is commercially available from different suppliers (US, Europe, China, India, ...)

2. Integrating Diamond & Chips

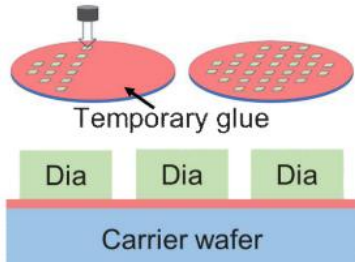
a. Heat Spreaders

Fabricating Diamond Heat Spreaders

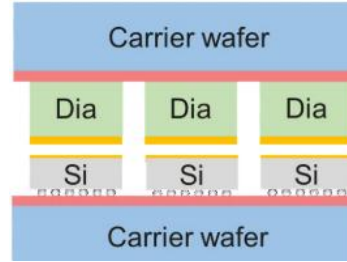
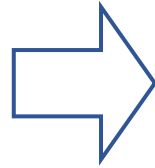


<https://www.diamond-materials.com/en/products/thermal-management/heat-spreaders/>; Mendes, IEEE EPS Newsletter Dec (2025) 1–8

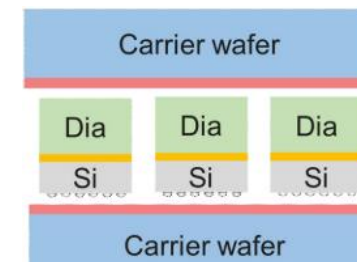
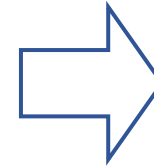
TCB of Diamond Heat Spreaders & TTVs



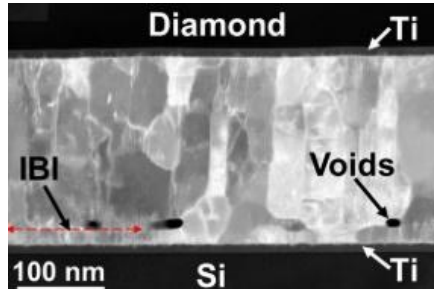
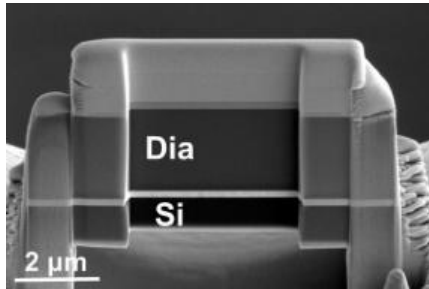
Assembling of 12x12 mm² Si chips with Sn3.5Ag solder bumps and 12x12x0.4 mm³ PCD with temporary carrier wafers.



Metallization of PCD (8/200/5/20 nm Ti/Cu/Ti/Au) and Si (8/20 nm Ti/Au).

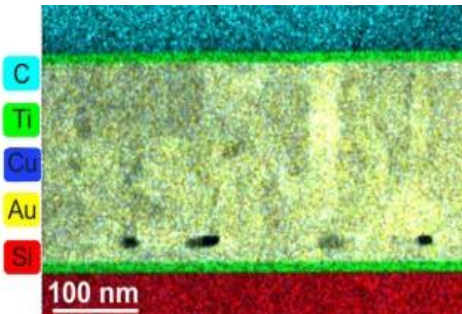


Au-Au RT cold welding + TCB @200°C, 30 min, 3 MPa



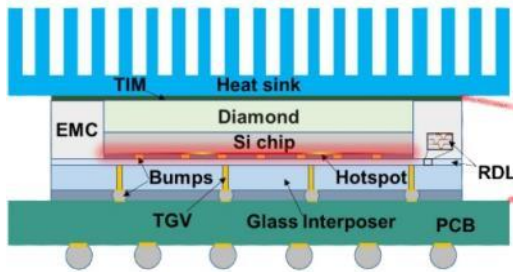
Top left: SEM and **Top right:** TEM images on PCD/Si interface.

Bottom: EDS mappings for C, Si, Ti, Cu, and Au.

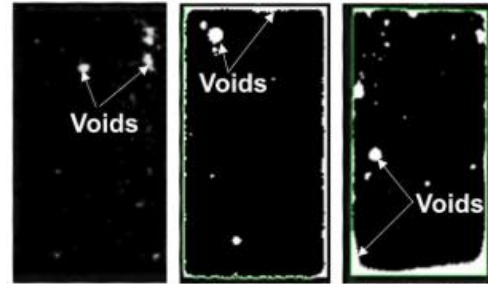


- ➡ Bonding layer with high re-melting temperature (>900°C for CuAu interlayer) can withstand multiple solder reflows @260°C.
- ➡ Bonding scheme results in uniform metal bonding layer between Si and PCD with some residual voids.
- ➡ Low TBR of **9.74 m²·K/GW**.
- ➡ Low-temperature & low-pressure die-attachment → original appearance of solder bumps restored after reflow.

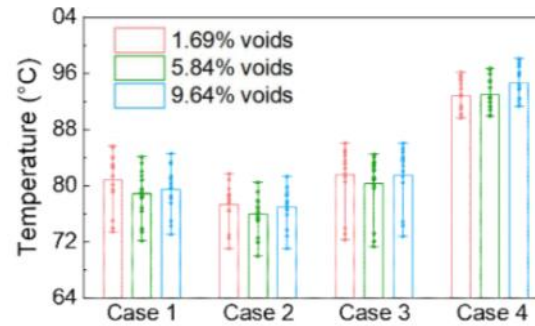
TCB of Diamond Heat Spreaders & TTVs



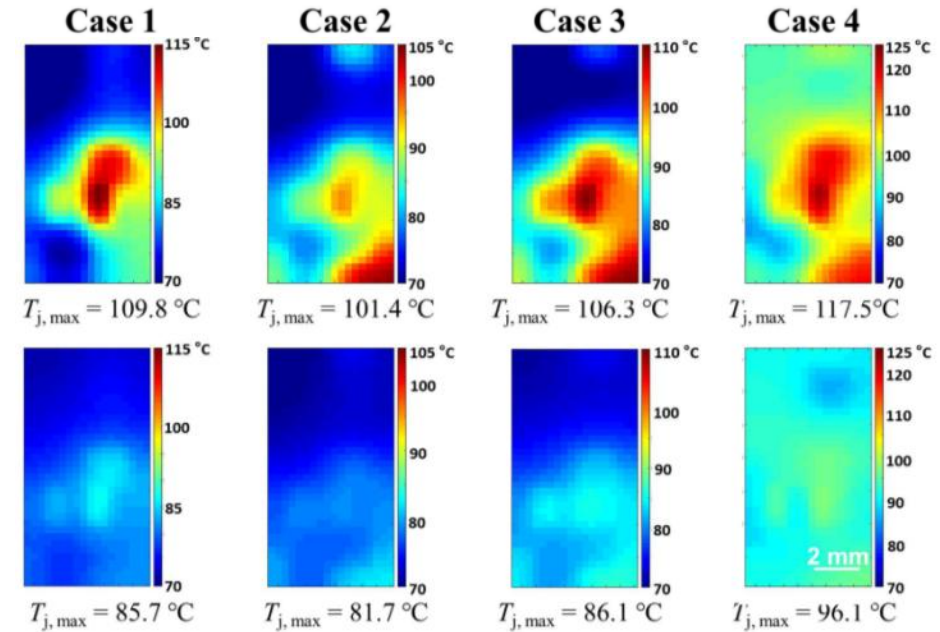
Integration of diamond-on-chip-on-glass interposer (DoCoG).



1.69% voids 5.84% voids 9.64% voids
Voids at PCD/TTV bonding interface



Impact of bonding layer porosity on hotspot temperature.



Temperatures maps for different heating conditions.



1	14		15		28
	13		16		
2	11	12	17	18	27
	10		19		
	9		20		
3	7	8	21	22	26
	6		23		
	5		24		
4					25

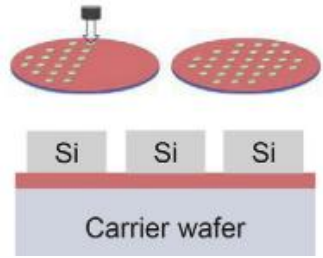
Hotspot #	Case			
	1	2	3	4
17	2	1	1.5	1.5
10 & 20	1.5	--	1	1.5
13 & 14	--	1.5	1.5	1
P_{tot} (W)	33	33	33	45
ΔT (°C)	24.1	19.7	20.2	21.4

Left: Heating zones of Si TTV. Right: Conditions for selective heating.

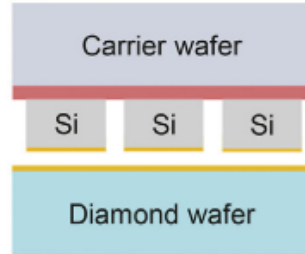
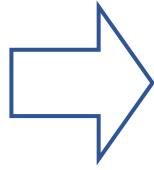
☞ Voids with porosity <10% show minimal impact on cooling capability.

- ☞ Integration of diamond **reduces hotspot temperature** and **improves temperature uniformity** for all heating conditions.
- ☞ Case 1: reduction of junction-to-ambient thermal resistance by **28.5%**.

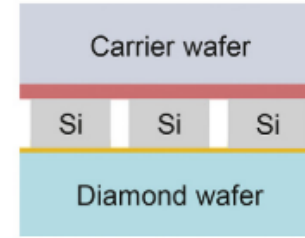
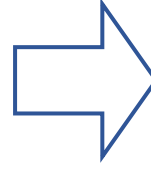
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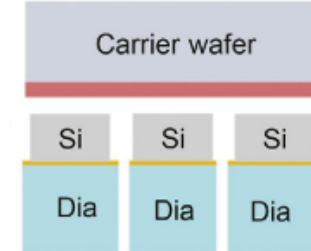
Temporary assemblage of Si dummy dies on glass carrier.



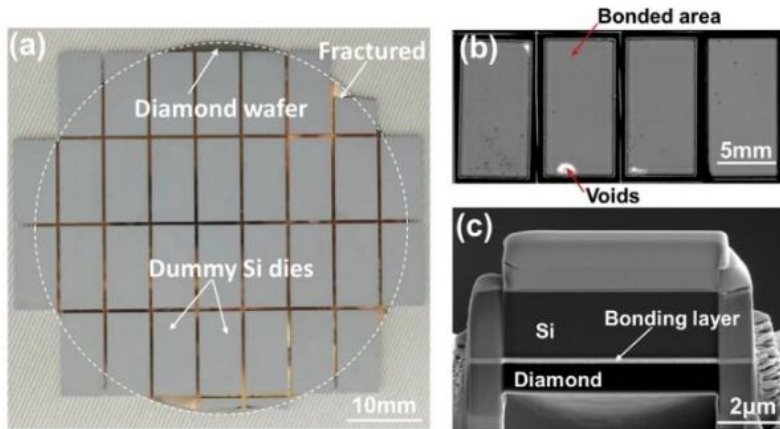
Metallization of 2-inch PCD (8/200/5/20 nm Ti/Cu/Ti/Au) and Si (8/20 nm Ti/Au).



Au-Au RT cold welding + TCB @200°C, 30 min, 2 MPa.

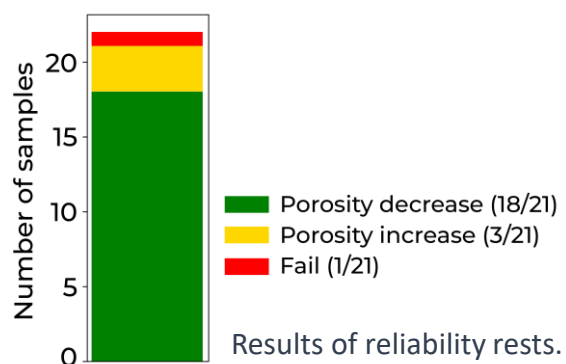
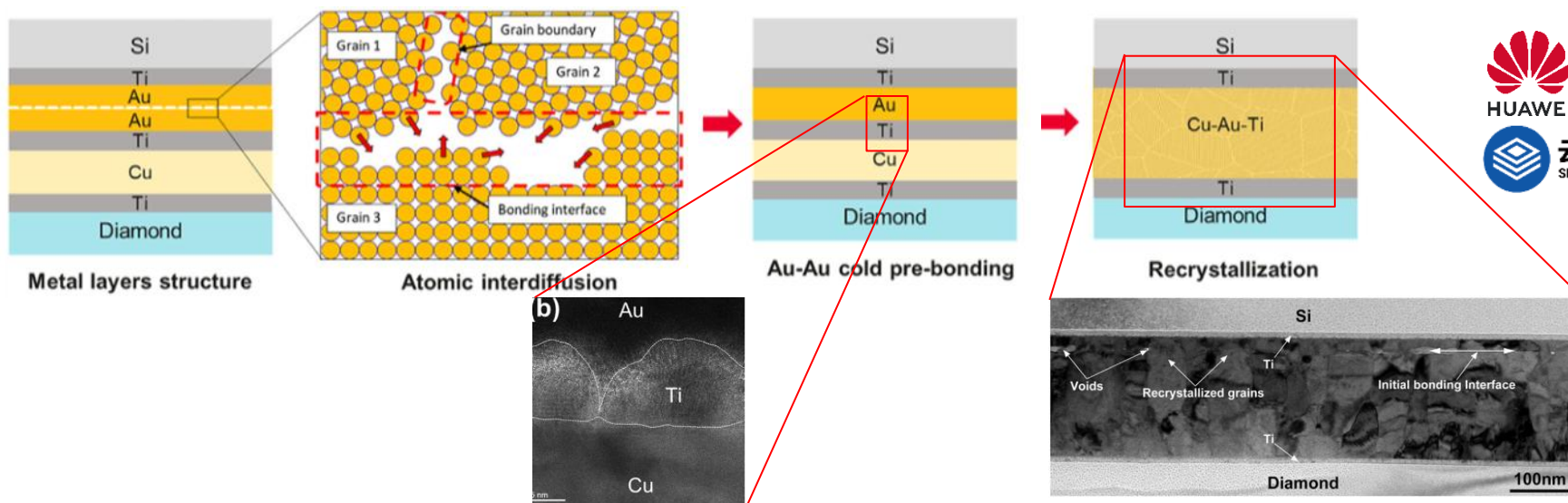
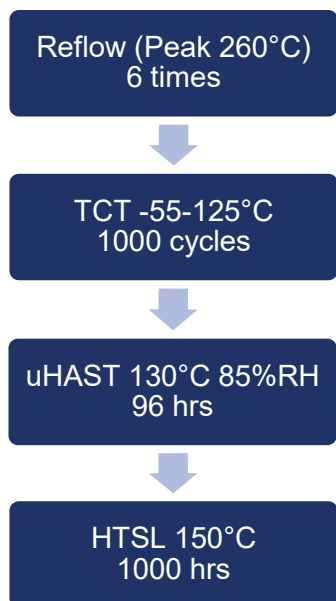


De-bonding and dicing.



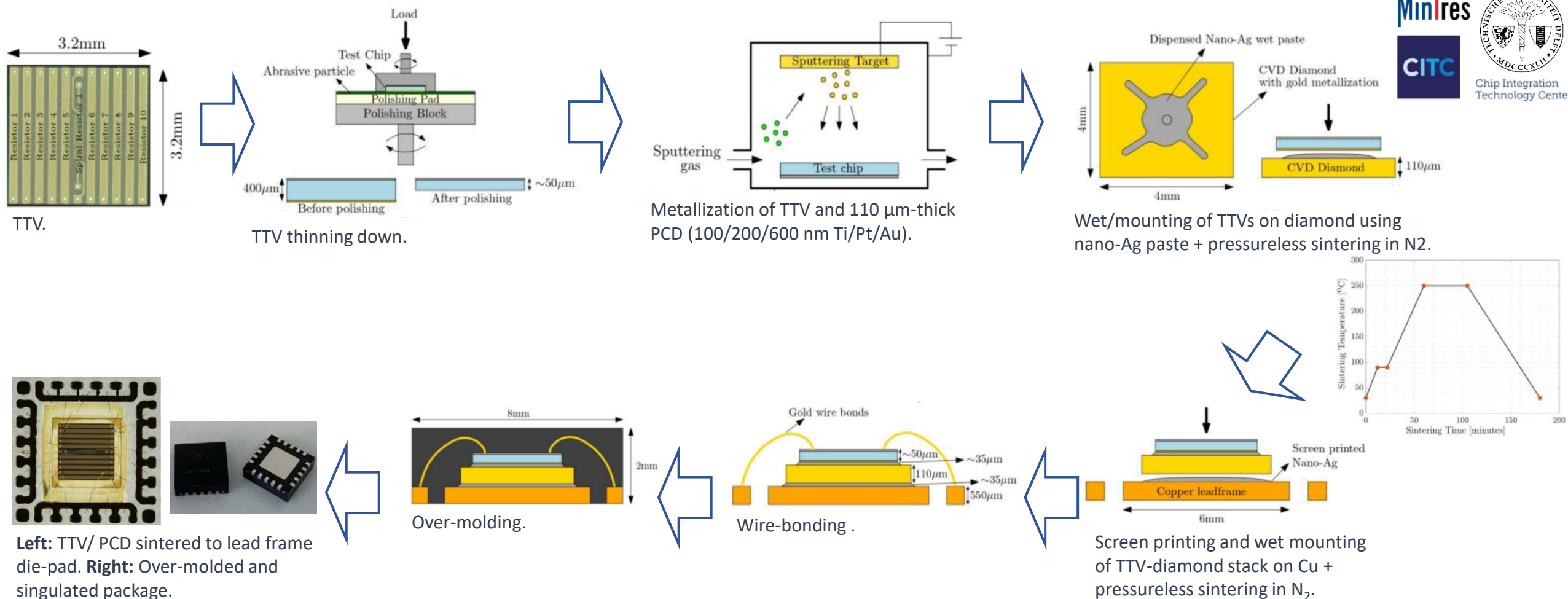
- ➡ Bonding porosity <10%;
- ➡ Pull-off tests: average bond strength Si / diamond interface = 7.73 ± 0.75 MPa.

TCB of Diamond Heat Spreaders & TTVs

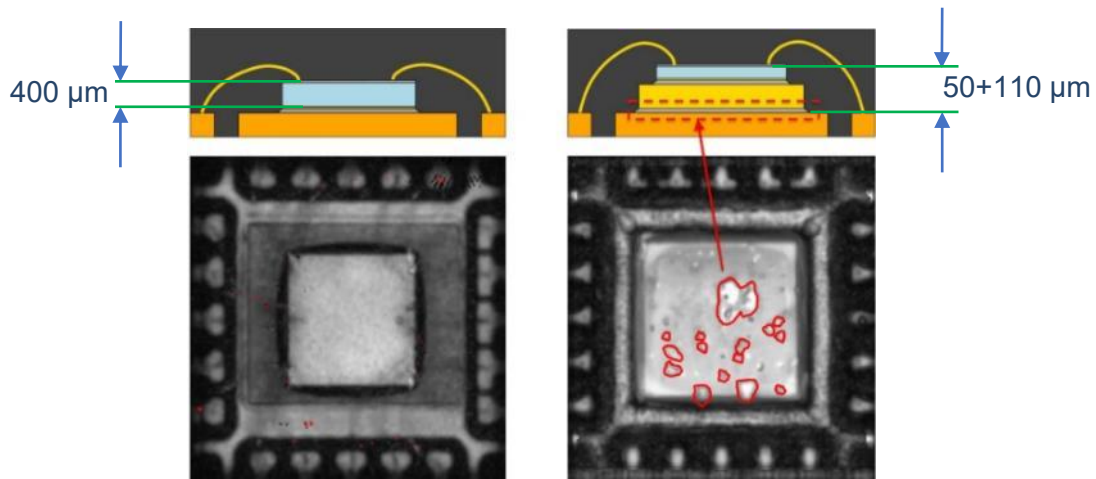


- Bonding process results in heterogeneous bonding layer with residual voids and distinct grain boundaries.
- Competing mechanisms during thermal cycling:
 - Enhanced atomic diffusion reduces residual porosity in most samples → void healing.
 - Local stress concentrations due to CTE mismatch leads to interfacial degradation in other samples → void growth.
- TCB @200°C: metastable Cu-Au-Ti nanolayer interface!

Pressureless nano-Ag Sintering, Diamond & TTVs



Pressureless nano-Ag Sintering, Diamond & TTVs

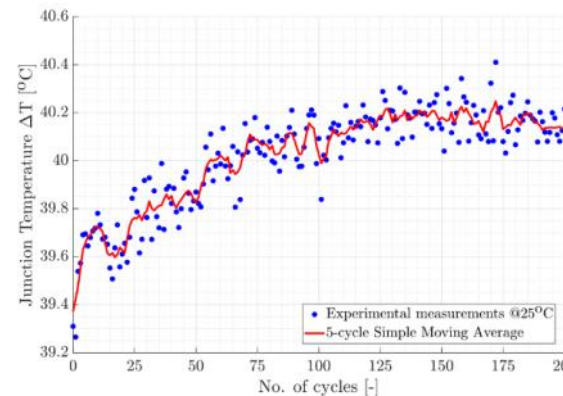


CSAM images of **Left:** standard and **Right:** PCD PQFN package. Red lines: voids at PCD-lead frame interface.

- Thickness Ag layer: $\approx 35 \mu\text{m}$.
- Voids at diamond-lead frame interface.

PACKAGE TYPE	JUNCTION TEMPERATURE ($^{\circ}\text{C}$)	MINIMUM TEMPERATURE @2 sec ($^{\circ}\text{C}$)
Standard PQFN	43.28	29.29
PCD PQFN	39.13	30.34

- 9.6% reduction in junction temperature for **6.6 W** input power.
- Decrease in thermal spread.
- Margin for improvement of sintering process.



Maximum temperature after thermal cycling from -55 to 150°C .

- 2% thermal degradation of PCD-package after **200 cycles**;
- After **200 cycles** temperature of PCD-package is $\approx 7.25\%$ lower than temperature of standard package at **0-cycle**.

Pressureless nano-Ag Sintering, Diamond & GAN HPA MMIC



Dispensing of nano-Ag paste on Ti/Pt/Au-plated diamond heat spreaders and 25.4x25.4x3 mm³ Au-plated MoCu cold plates.



Placement of 5.25x5.4 mm² GaN-on-SiC MMIC on diamond heat spreader with die-bonder and pressureless sintering in N₂.

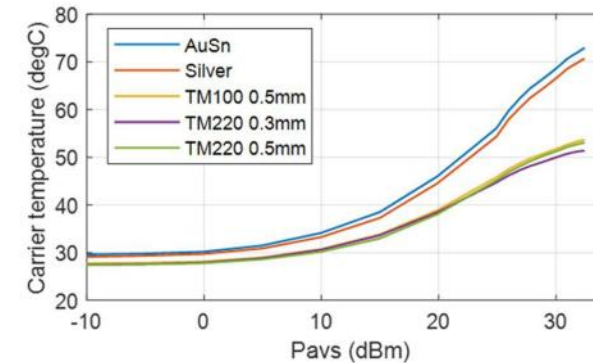
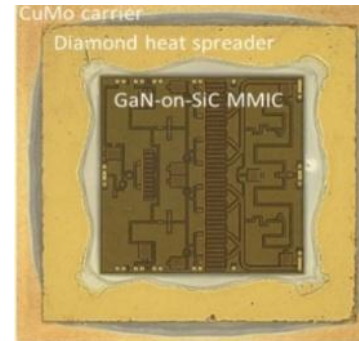


Placement of MMIC-on-diamond on MoCu cold plate and pressureless sintering in N₂.

DIAMOND ID	TC (W/m-K)	THICKNESS (μm)	AREA (mm²)
TM100_500	1000	500	8x8
TM200_300	2200	300	
TM200_500	2200	500	

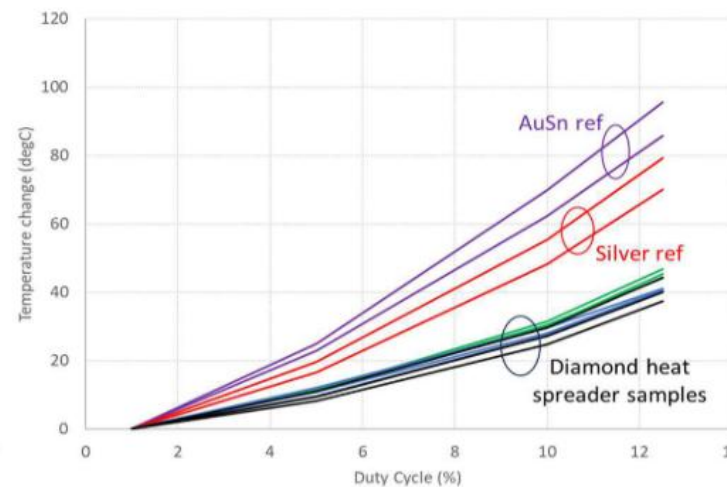
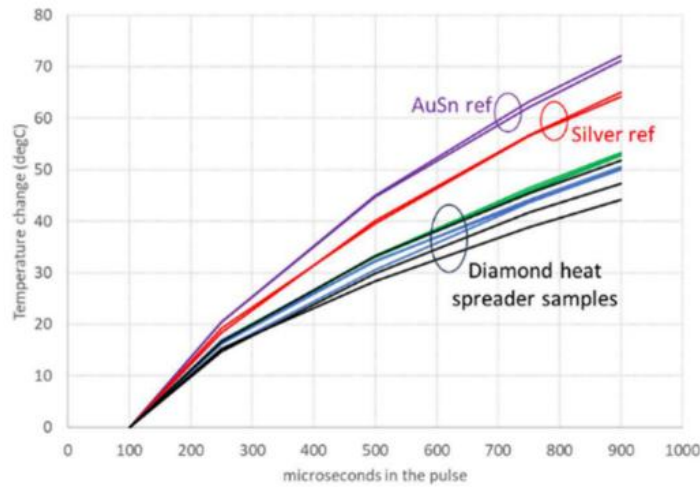
Thickness Ag layer: $\approx 30 \mu\text{m}$

$TC_{\text{AG layer}} \approx 100 \text{ W/m-K}$



Left: MMIC-on-diamond-on-MoCu cold plate. **Right:** Temperature of CuMo cold plate with 1 ms pulses and 10% duty cycle.

Introduction of diamond heat spreader decreases temperature of MoCu cold plate by almost 30%.



MMIC temperature change vs. **Left:** time in pulse and **Right:** pulse duration.

Purple: AuSn reference.

Red: Ag-sintered reference.

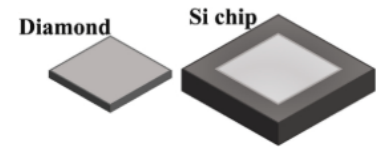
Green: diamond 1000 W/m-K, 500 μm .

Blue: diamond 2200 W/m-K, 300 μm .

Black: diamond 2200 W/m-K, 500 μm .

- Integration of diamond heat spreader:
 - 20-30% reduction in MMIC temperature;**
 - $\approx 30\%$ reduction of carrier/package thermal resistance;**
 - increase of RF signal pulse width** by a factor of **30-100**, while maintaining the same reliability.
- Difference between diamond heat spreaders only becomes significant at high junction temperatures.
- Lowest quality diamond provides significant performance improvement!**

Pressure-assisted nano-Ag Sintering, Diamond & TTVs



Ar plasma activation of 27×28 mm² diamond and Si chips.



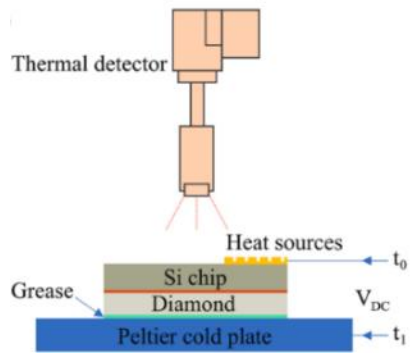
Deposition of 20/100 nm Cr/Au on 27×28 mm² diamond and Si chips.



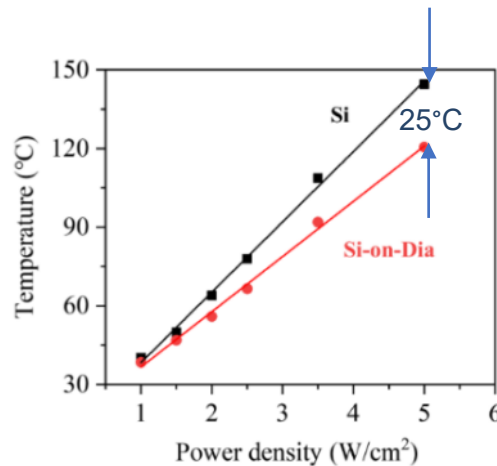
Printing of 40 µm of Ag sinter paste and pre-drying @160°C, 30 min.



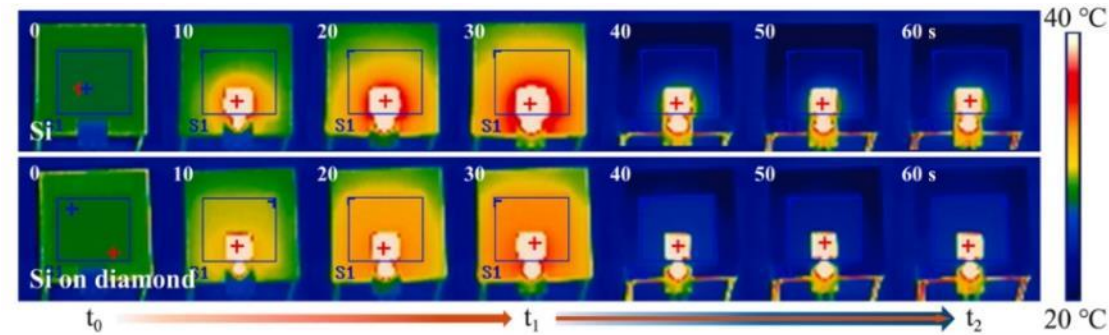
Sintering @200°C, 30 min, 2-10 MPa.



Left: Thermal measurements setup.



Right: Surface temperature vs. power density.



Evolution of surface temperature of **top: Si** and **bottom: Si/diamond** chips by IR imaging.

- ☞ TBR between **428-769 m²·K/GW** depending on sintering pressure.
- ☞ The PCD heat spreader decreases the hotspot temperature by **25°C @5W/cm²** and increases in-plate temperature uniformity.

Processor chip

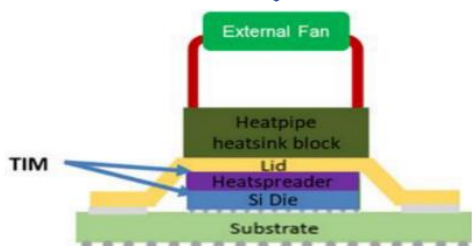
Thinning down of CPU chip.



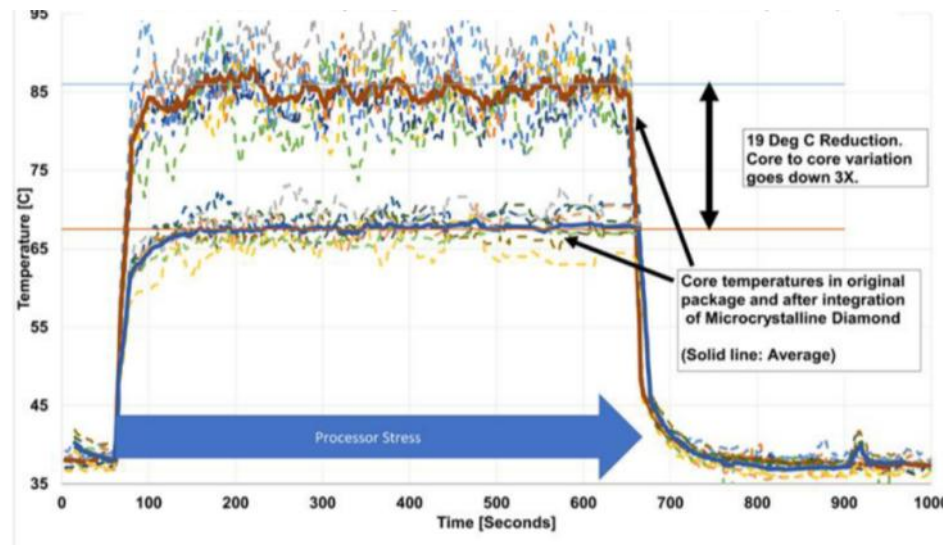
Processor chip

PCD

Bonding of chip and diamond using Ga-based liquid metal TIM.



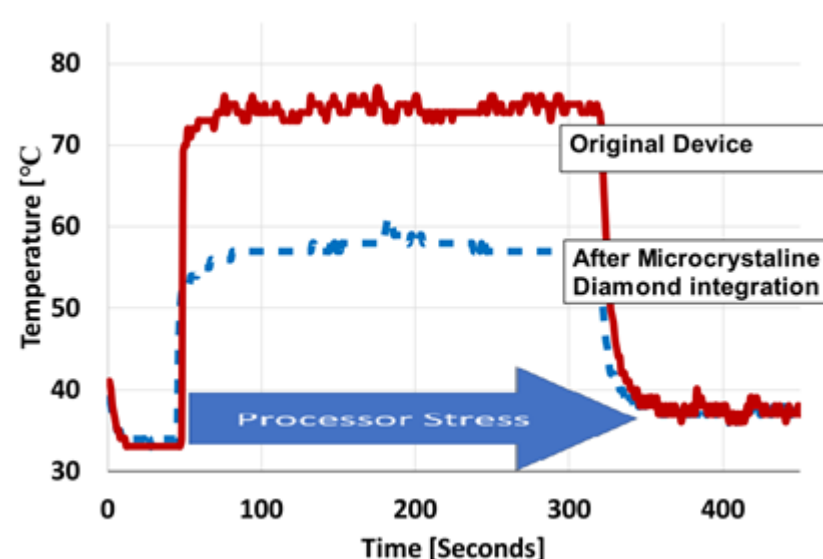
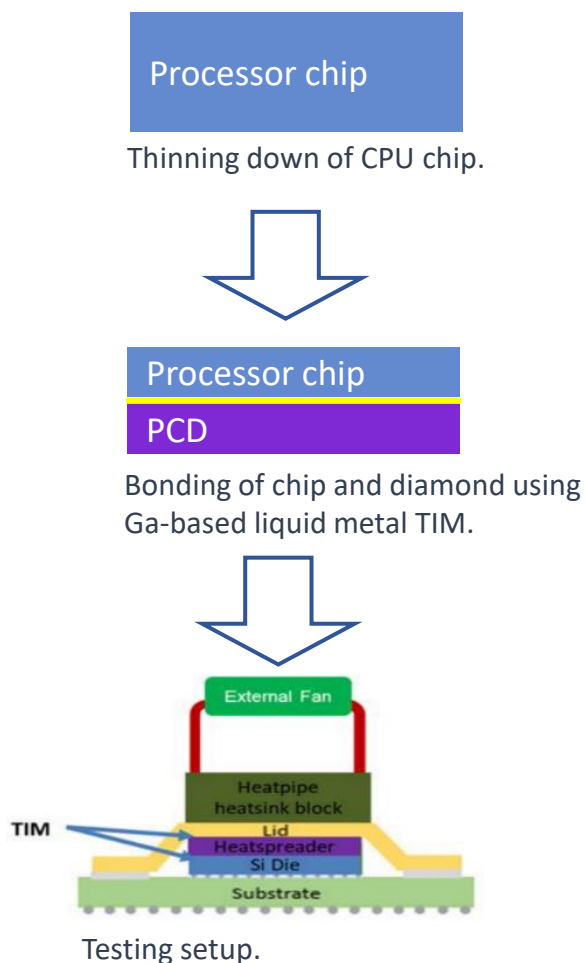
Testing setup.



Intel Gen 11 (8 core 14 nm).

- ➡ **85% increase** in junction-to-case thermal conductance.
- ➡ **8 core 14 nm processor:**
 - ➡ **15°C temperature reduction** at full stress;
 - ➡ reduction of temperature spread from **4.8 to 1.2°C**;
 - ➡ **5% increase** in core operation power.

Liquid Metal TIM, Diamond Heat Spreaders & CPUs



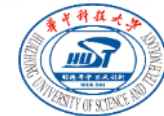
AMD Ryzen 5900 (12 core 7 nm).

- 12 core 7 nm processor:
- 17°C temperature reduction;
- Identical overclocking from 3 to 5.6 GHz of all cores with:
 - processor + diamond in **standard cooling system**;
 - custom **600\$ 200 W water-based cooling system**.

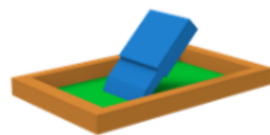
2. Integrating Diamond & Chips

b. Diamond Boards

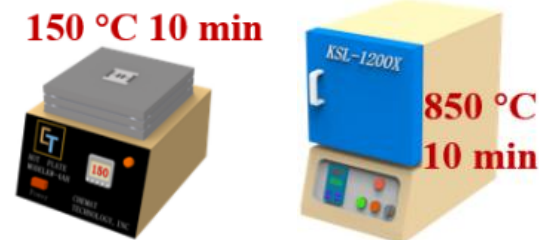
Diamond Boards & Deep UV LEDs



Diamond + Al_2O_3 boards.



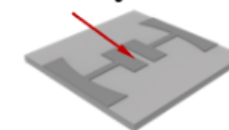
Screen-printing of Ag paste.



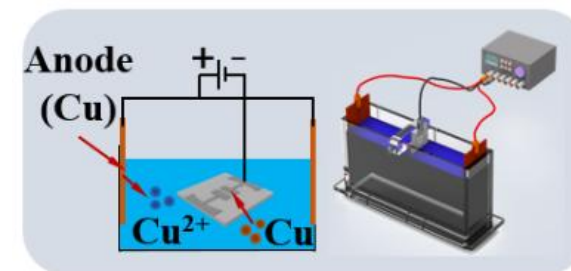
Drying and sintering of Ag paste.



Silver layer



Board with Ag seed layer.



Cu electroplating .



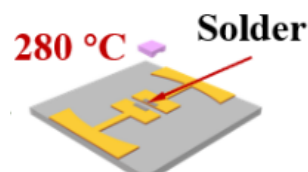
Au electroless plating.



Gold layer



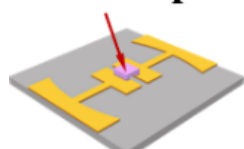
PCTF diamond / Al_2O_3 boards.



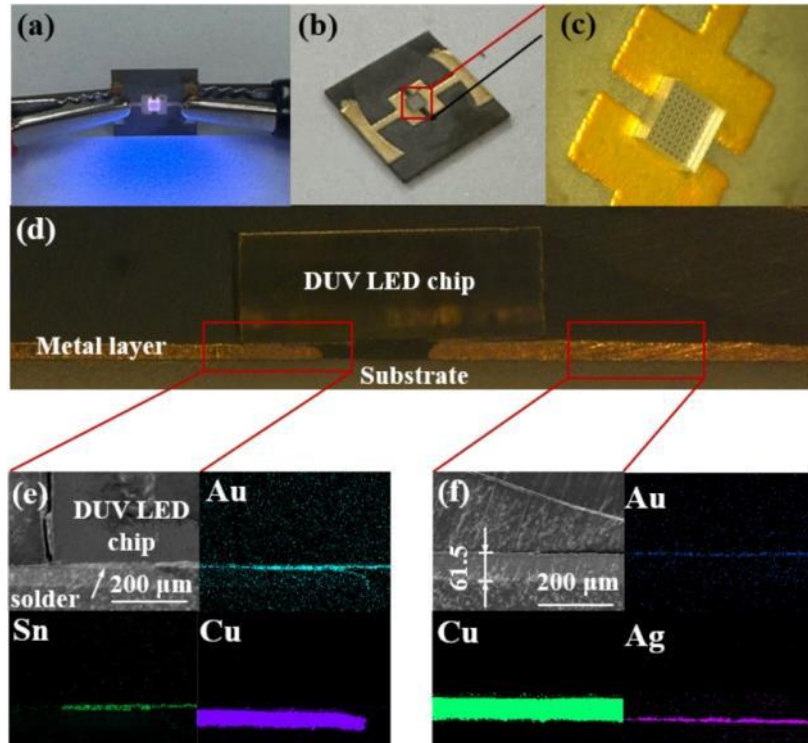
AuSn eutectic soldering of DUV LED @280°C.



DUV Chip



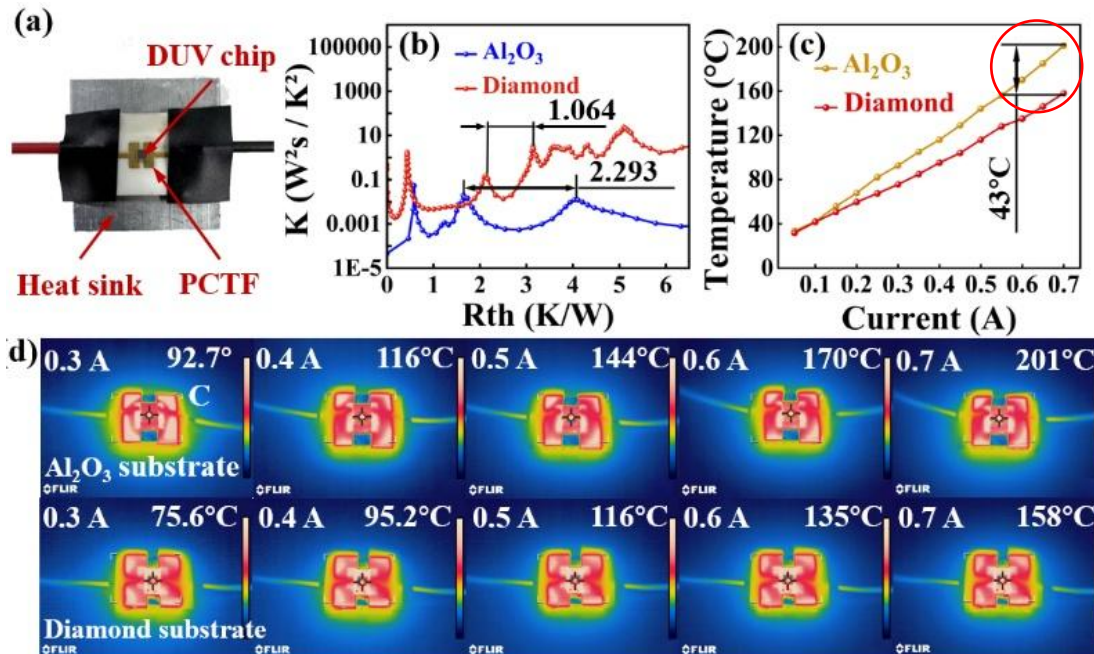
DUV LED on diamond / Al_2O_3 boards



(a-c) Photos of LED chip on PCTF-diamond board.
(d) Cross-section view and (e,f) SEM images and EDS mapping of LED chip on PCTF-diamond board.

- Total thickness of metallization layer: 61.5 μm (2.6/54.4/4.5 μm Ag/Cu/Au);
- Robust bonding between the PCTF-diamond substrate and LED chip without any voids.
- **Thermal resistance of PCTF-diamond board is 53.6% lower** than that of PCTF- Al_2O_3 board (1.064 against 2.293 K/W, respectively).

Diamond Boards & Deep UV LEDs



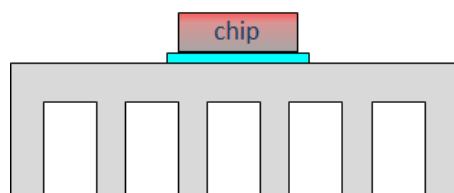
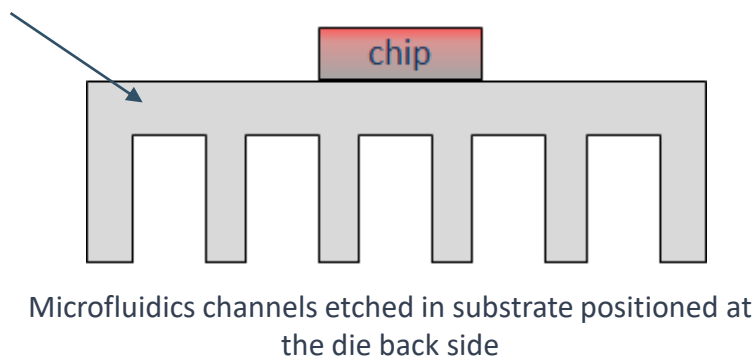
(a) PCTF board mounted on heat sink.
(b) Differential thermal resistance, (c) junction temperature and
(d) surface temperature of LED chips on PCTF-diamond and Al_2O_3 boards.

- 0.7 A $\rightarrow$ surface temperature is $43^{\circ}C$ lower ($158^{\circ}C$ against $201^{\circ}C$);
- 20.3% increase in light output power;
- 14.2% improvement in conversion efficiency.

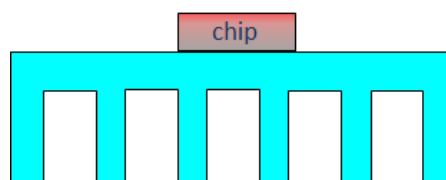
Thick Cu-on-Ag metallization enables excellent heat spreading and robust adhesion, but at the cost of high Ag paste sintering temperature and potential stress from thick metal layers.

3. Liquid Cooling with Diamond

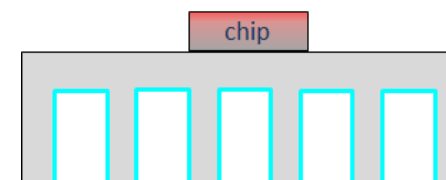
Microchannels



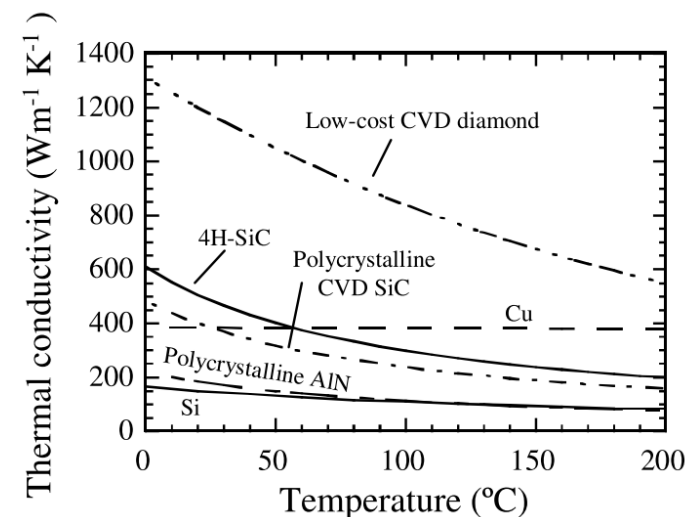
1. Diamond heat spreader



2. Diamond microchannels

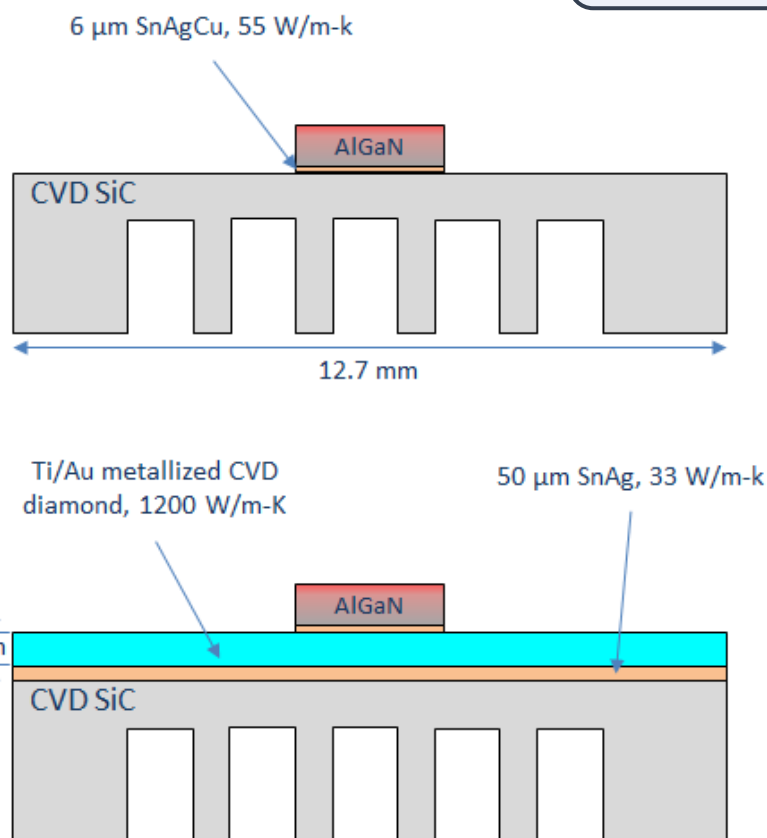


3. Diamond films



Diamond Heat Spreader & SiC Microchannels

Diamond heat spreaders improve the heat transfer coefficient between the heated chip and the microchannel cooler.



Integration of **400 μm -thick 1200 W/m-K** diamond heat spreader with CVD SiC microchannel using 50 μm -thick solder (33 W/m-K) & water as working fluid:

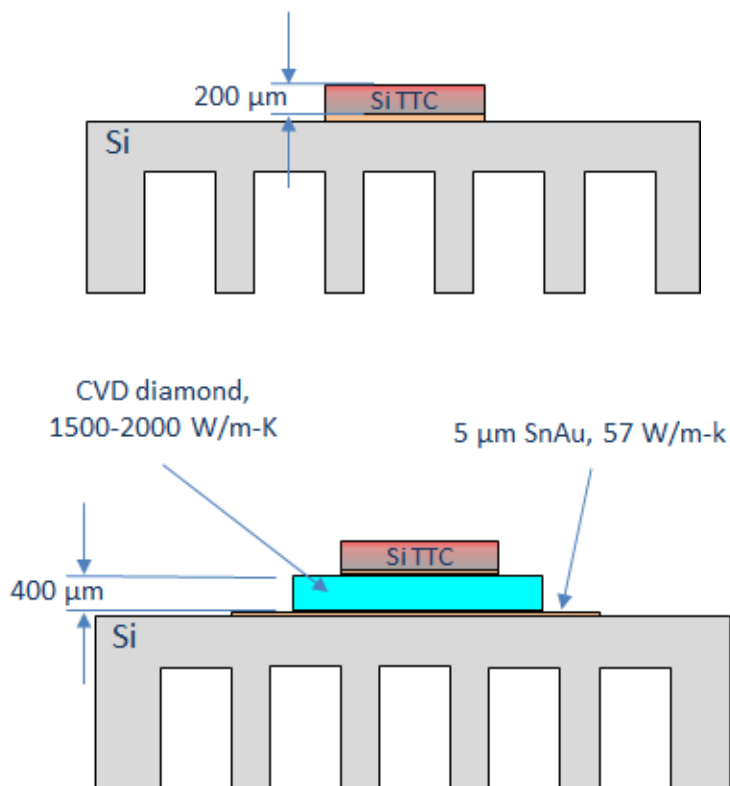
☞ **Temperature rise $\approx 30\%$ lower** than for SiC alone.

4–5 kW/cm² heat fluxes can be handled maintaining **temperatures $< 120^\circ\text{C}$** using:

☞ **3.8 l/min** (SiC);

☞ **0.72 l/min** (diamond-on-SiC).

Diamond heat spreaders improve the heat transfer coefficient between the heated chip and the microchannel cooler.



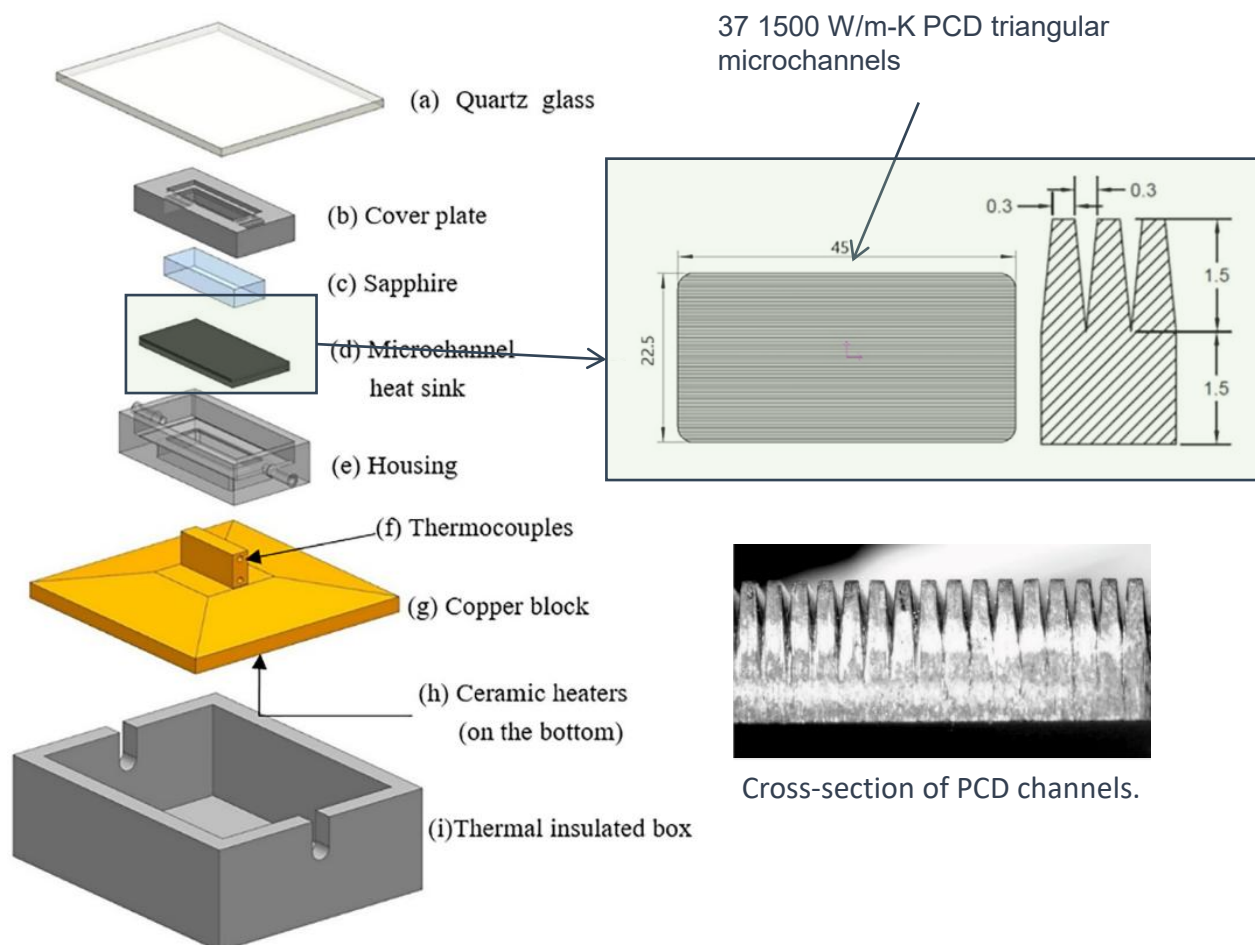
Integration of **400 μm-thick 2000 W/m-K** diamond heat spreader with Si microchannel using 5 μm-thick solder (57 W/m-K) :

- ➡ Hotspot **temperature reduction** by $\approx 5.7\%$ ($54\text{ W} \rightarrow 5\text{ kW/cm}^2$) and $\approx 26.1\%$ ($70\text{ W} \rightarrow 6.5\text{ kW/cm}^2$).
- ➡ $\approx 43\%$ **heating power increase** for 180°C hotspot temperature.
- ➡ **Reduction** of centre/edge hotspot **temperature variation** from 8°C (w/o) to 2°C (with diamond).

Replacing diamond (**2000 W/m-K**) with diamond (**1500 W/m-K**):

- ➡ Maximum hotspot temperature rise $< 2\%$.

Diamond Microchannels & Flow-Boiling Cooling

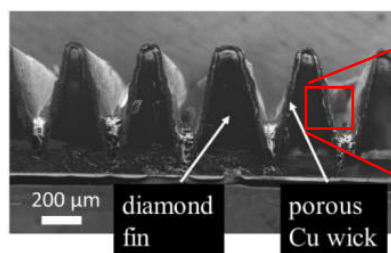


Test setup. Dimensions in mm.

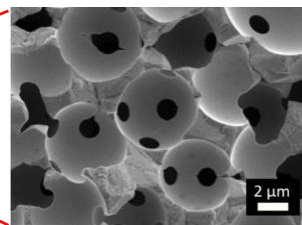
Flow-boiling cooling using ammonia as working fluid.

- ➡ This architecture manages a central hotspot with **267 W/cm²** heat flux while maintaining the heat source temperature at **53.3°C** for a mass flux of **320 kg/m²s**.

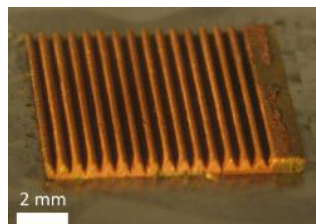
How can we improve the heat transfer coefficient between the diamond microchannel and the coolant?



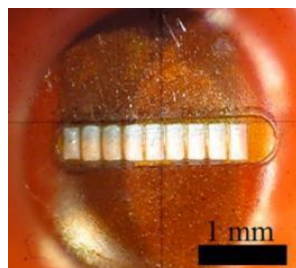
PCD heat spreaders.



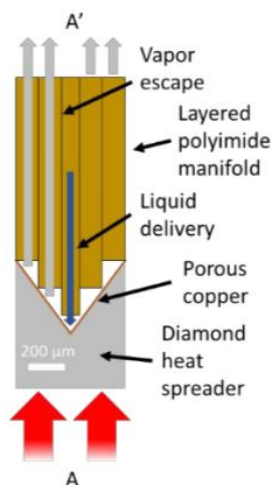
Fine-featured porous Cu.



Cu-covered diamond microchannels.



ePTFE phase separation membranes (white).



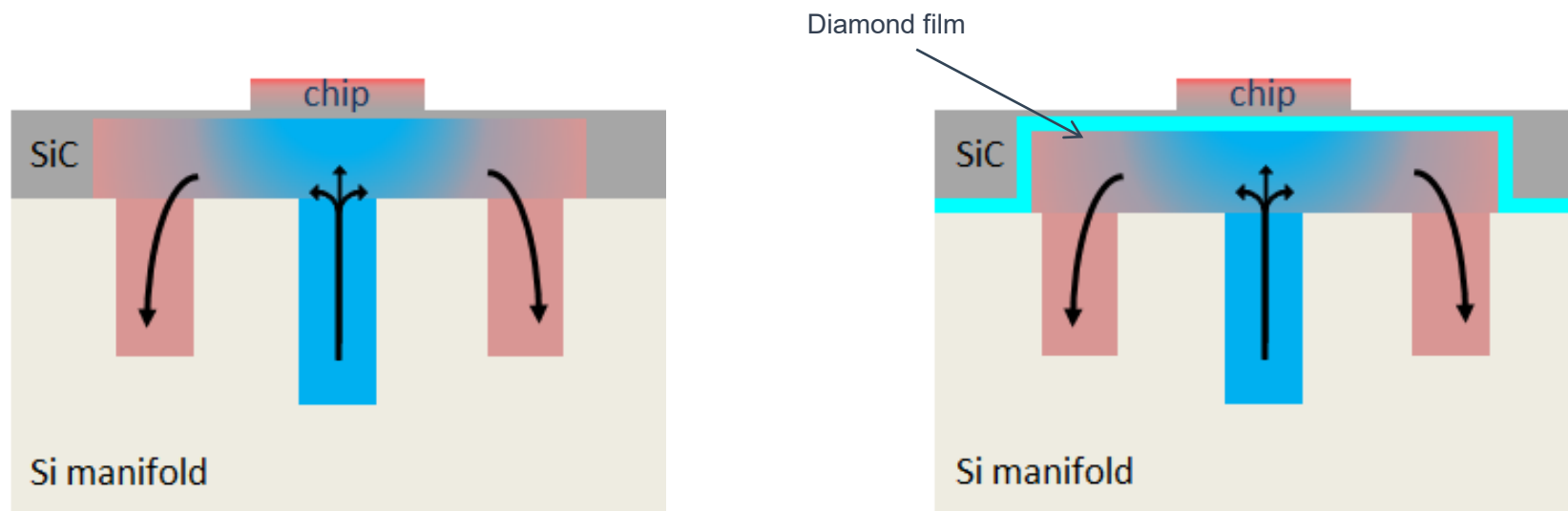
Cross-section of single heat sink channel and manifold.

VOLUMETRIC FLOW RATE (ml/s)	CRITICAL HEAT FLUX (W/cm ²)
3.08	≈1342
0.96	≈824

Dissipation of heat fluxes **>1300 W/cm²** at the heated surface by combining:

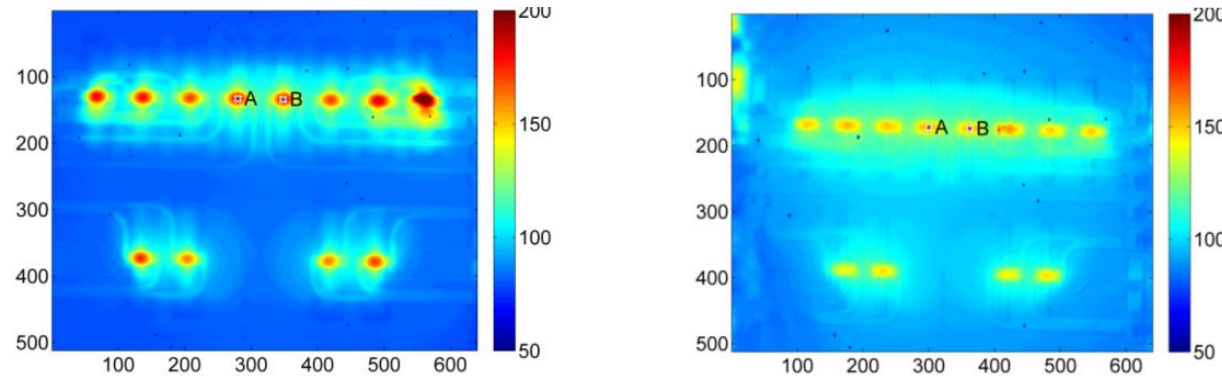
- Heat spreading by diamond;
- Boiling heat transfer on fine-featured porous copper;
- Uniform liquid distribution via 3D microfluidic manifolding.

How can we increase the performance of impingement cooling with diamond?



- ➡ Etching microchannels below die;
- ➡ Diamond CVD inside the etched cavities;
- ➡ Coolant supplied to the chip via Si.

How can we increase the performance of impingement cooling with diamond?

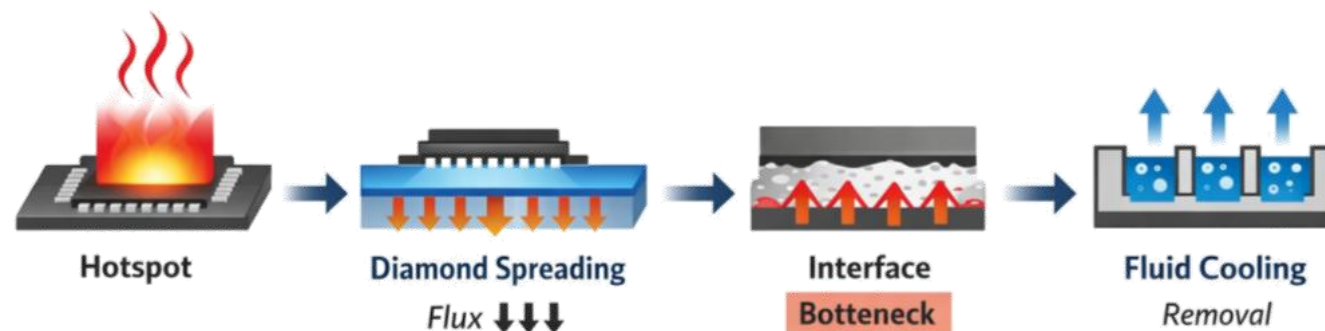


IR images of dies for 45 W heat input. **Left:** TDV12XL / H-Channel, Flow = 4.1 g/s.

Right: TDV12 / Straight Channel, Flow = 2.3 g/s.

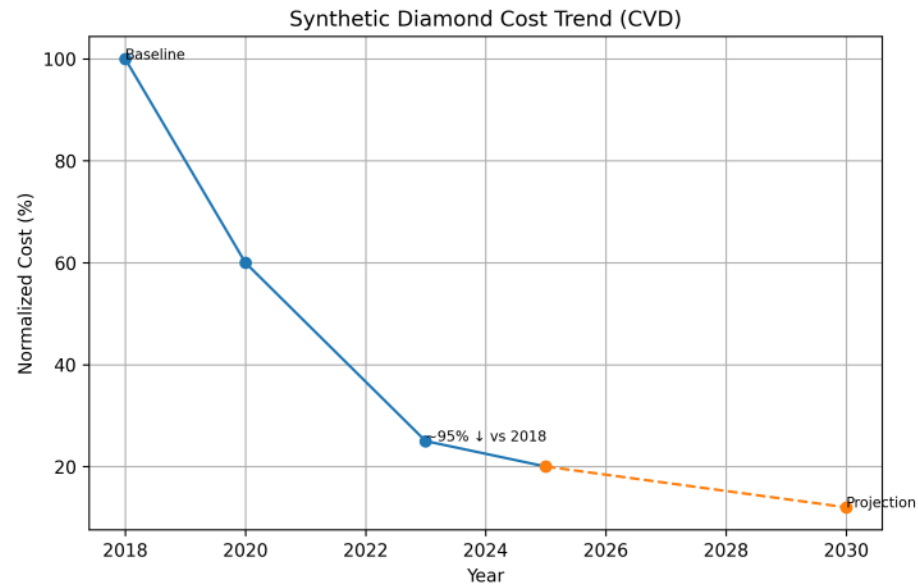
Baseline performance measurements, 1 MPa pressure drop, PGW
@70°C, maximum temperature <200°C:

- ➡ TDV12XL → larger footprint, H-shaped microchannel, **526 W/cm²**;
- ➡ TDV12 → smaller footprint, rectangular microchannel, **680 W/cm²**.
- ➡ Estimated **≈4× increase** in **RF output** power of GaN chips.



- ➡ Integrating diamond heat spreaders between chip and microchannel cooler spreads the heat from local hotspots, improves thermal uniformity and reduces peak heat flux seen by coolant by up to $\approx 85\%$.
- ➡ Diamond microchannels enable management of heat fluxes in the kW/cm^2 range.
- ➡ Diamond thin films extend the limits of microchannel coolers.
- ➡ Interfaces become the bottleneck with TIMs strongly impacting performance.

5. Challenges & Mitigation Strategies



Evolution of synthetic diamond cost since 2018. Future trend shown as projection in orange dashed line.

- ➡ Synthetic diamond cost has decreased up to $\approx 95\%$ since 2018 in some segments;
- ➡ Prices scale down with manufacturing capability;
- ➡ Improvement in reactors efficiency reduced per-carat production cost by 44%.

Cost is still a limiting factor!



Reduce post-processing

Polishing can dominate the cost →
roughness-tolerant bonding



SCD vs. PCD rationale

SCD may bring incremental
benefit only



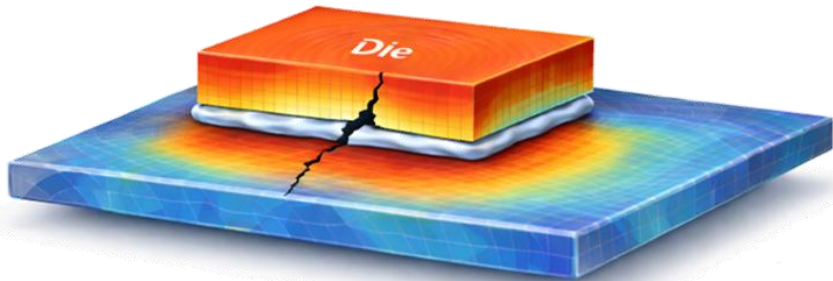
Avoid over-specification

Don't over-spec TC, thickness,
area



Model first

Resort to FEM whenever
possible to minimize TC and
footprint



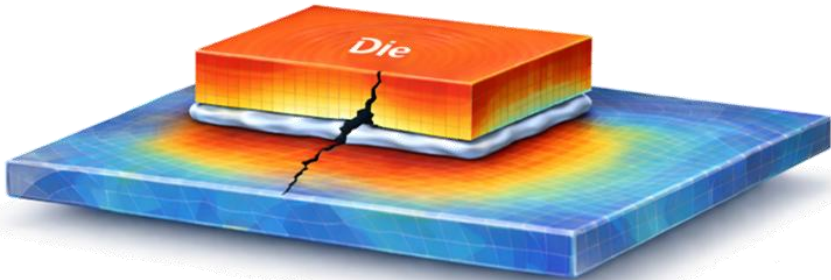
1. Diamond's intrinsic properties (low CTE, high Young Modulus) may affect assembly reliability.
2. CTE mismatch between diamond heat spreader and chip, combined with high lattice stiffness, generates significant thermomechanical stress during thermal cycling.
3. Thermal stresses scale with planar dimensions (length and width), so CTE mismatch is especially critical for large-area chips and heat spreaders.
4. For chips on crystalline substrates (e.g., GaAs, InP), excessive tensile stress can lead to substrate fracture when the assembly exceeds the chip's tensile fracture load.

https://eps.ieee.org/images/files/enews/EDMS_Diamond_Thermal_Interface.pdf



Soft, low-temperature solders (In, Bi alloys):

- ☞ Suitable for large chips on diamond.
- ☞ Low Young's modulus and creep behavior help relieve strain during thermal cycling.



Hard, high-temperature solders (AuSn, AuGe; 280–356°C):

- ☞ High stiffness and higher CTE ($\approx 13\text{--}16 \times 10^{-6}/\text{K}$) reduce transfer of tensile load to brittle semiconductor substrates.



CTE-tailored laminates:

- ☞ Adjust CTE by adding Cu or Al layers to metallization stack.
- ☞ Use Cu–Invar–Cu or Cu–Mo–Cu stacks to tune the overall expansion of the multilayer.

Improving Thermal Management in 3D packaging via Bulk and Interfacial Heat Transport



❖ Joana Mendes – Diamond heat spreaders and related applications

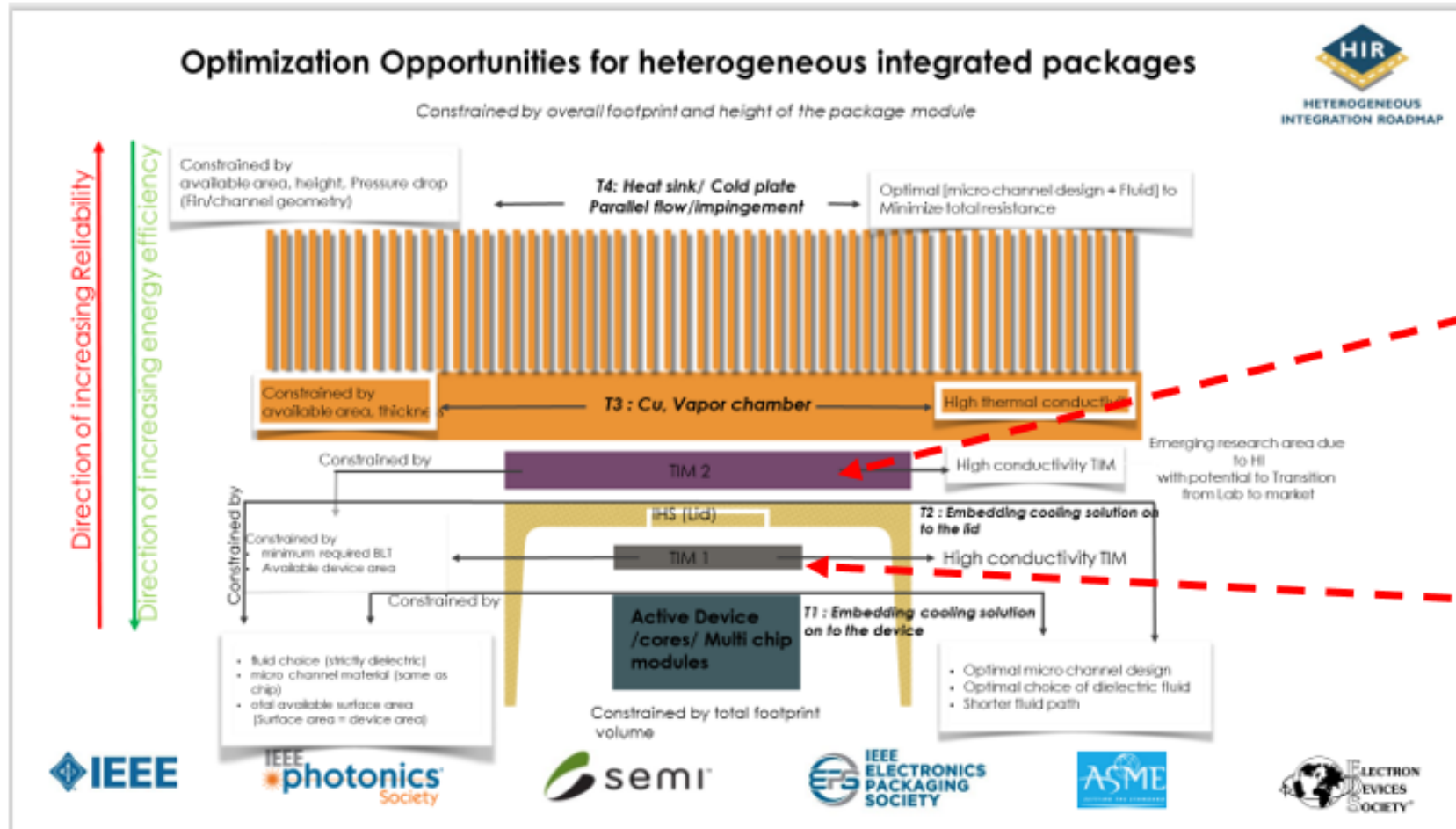
- Diamond: What & Why?
- Integrating Diamond in Advanced Packages
- Liquid Cooling with Diamond
- Challenges & Mitigation Strategies



❖ Christo Bojkov – Thermal Interface Materials Review

- TIM definitions, TIM1/TIM 1.5/TIM2 used cases
- Material performance vs requirements
- Application criteria, Metrology and Reliability
- Future products roadmaps: 2025-2030

Power Dissipation is the Greatest Challenge Facing Modern Electron Devices



TIM2 – Elastomers, Thermal grease, limited to $20+W/mK$ with most used cases closer to $5 W/m-K$

TIM 1 (TIM 1.5) - Die-attach materials (Sintered metals, LT Solders, PC materials Thermally Matched Composites are $60-110W/m-K$

TIM Category and Use Case

TIM Category	Material Type	TIM1	TIM1.5	TIM2	Typical Thermal Conductivity (W/m-K)	Notes
Thermal Greases	Silicone / Non-silicone with ceramic fillers	Common in mobile SoCs, reworkable	Not ideal for direct-die unless pressure-controlled	Widely used	~0.5 – 12	Easy application, good wetting, risk of pump-out
Phase Change Materials (PCMs)	Wax/polymer matrix with ceramic fillers	Good for smooth lids	Limited use (may not fully wet uneven dies)	Moderate power interfaces	~2 – 6	Activates ~45–65°C, better than grease under pressure
Metal Foils / Preforms	Indium, Indium Alloys	For flat, large dies (GPU/FPGA)	Excellent for direct coldplate contact	Requires uniform contact area	~60 – 90	High conductivity, zero pump-out, may creep
Liquid Metals	Gallium based alloys	Containment needed and no Al	High-end GPU w/ Ni surface	Containment needed and no Al	~15 – 38	Best conductivity, needs encapsulation
Graphite Sheets	Pyrolytic or expanded graphite	Poor Z-axis conduction	Layered stack (e.g. graphite + grease)	Excellent for lateral spreading	~5 – 15 (Z-axis)	Used in stack-ups with PCM/grease
Carbon Nanotubes (CNTs)	Vertically aligned CNT arrays	Experimental	R&D direct-die cooling	High cost, immature	~10 – 300+	Potential breakthrough in direct TIM1.5
Hybrid TIM Stacks	Any combo (e.g., indium + PCM)	Emerging best practice	Highly effective on warped dies	Helps compensate gaps	blended (based on components above)	Best for large or high-warpage die sizes



Cooling the Future:
TIM Strategies for High-Density AI and HPC Platforms

Dr. Jie Geng
R&D Manager – TIM Group/ Indium Corporation
INEMI Project Manager: Masahiro Tsuruya

Date of webinar: November 25, 2025

Hybrid Nanocomposite Thermal Interface Materials: The Thermal Conductivity and the Packing Density

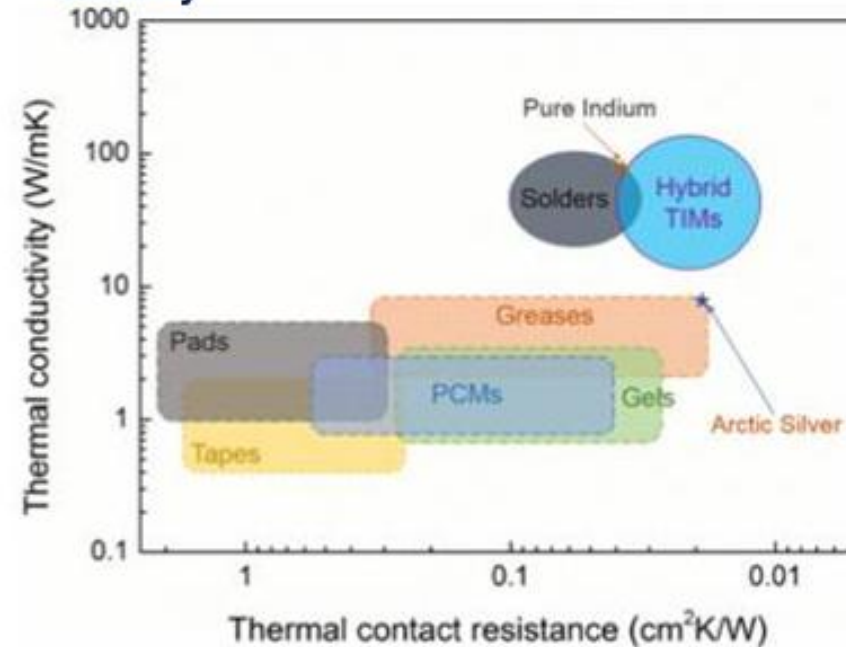


Fig. 8 Comparative mapping of thermal properties (k and R_c) of various TIMs. The novel hybrid TIMs in this study is shown in the upper-right corner, with k 's comparable to those of high-end solder TIMs, and R_c 's as low as those of the best thermal greases.

<https://www.researchgate.net/publication/335882126> Hybrid Nanocomposite Thermal Interface Materials The Thermal Conductivity and the Packing Density

We have investigated a novel hybrid nanocomposite thermal interface material (TIM) that consists of silver nanoparticles (AgNPs), silver nanoflakes (AgNFs), and copper microparticles (CuMPs). Continuous metallic network form while AgNPs and AgNFs fuse to join bigger CuMPs upon hot compression, resulting in superior thermal and mechanical performances. The assembly temperature is as low as 125 C due to the size effect of silver nanoparticulates. The thermal conductivity, k , of the hybrid nanocomposite TIMs is found to be in the range of 15-140 W/mK, exceeding best-performing commercial thermal greases, while comparable to high-end solder TIMs. The dependence of k on the solid packing density and the volume fraction of voids is discussed through comparing to model predictions.

Chapter 20: Thermal

For updates, visit <http://eps.ieee.org/hir>

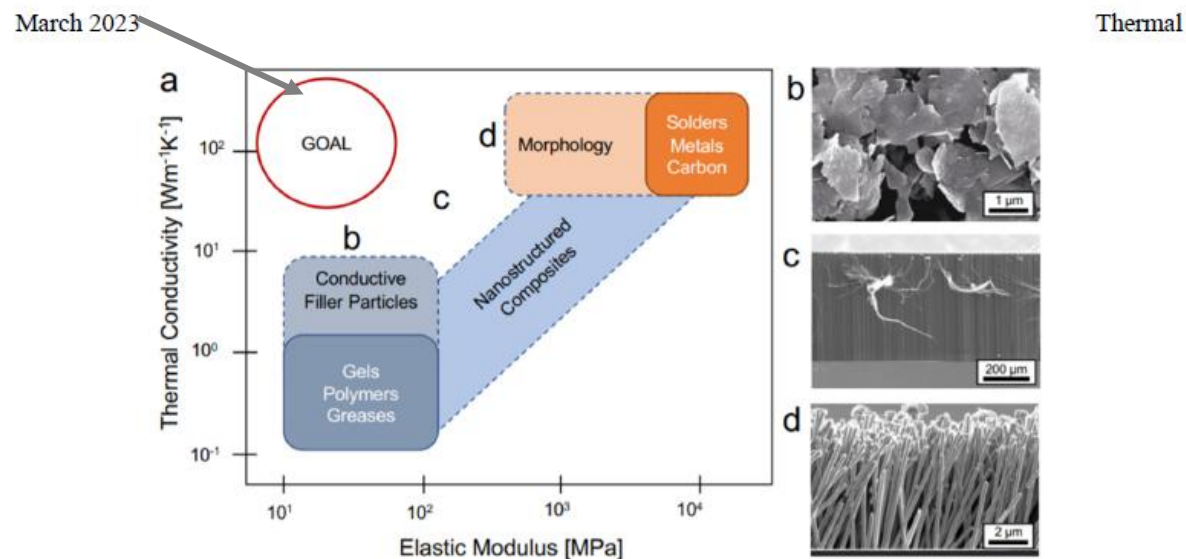


Figure 29 (a) Two common strategies can be employed to create high-performance TIM composites [27], (b) an example of graphene-polymer composite [28], (c) vertically grown nanotubes [29-30], (d) vertically electrodeposited nanowires [27, 32].

First strategy

is to begin with an intrinsically soft material and add fillers to increase the thermal conductivity, such as an example of **graphene-polymer composite** in Figure 29 (b).

The method of manufacture would be to begin with an intrinsically soft material, such as a polymer, and add conductive fillers (e.g., metal nanoparticles, **carbon nanoparticles, and graphene nanomaterials**) to increase the effective thermal conductivity by creating a conduction network.

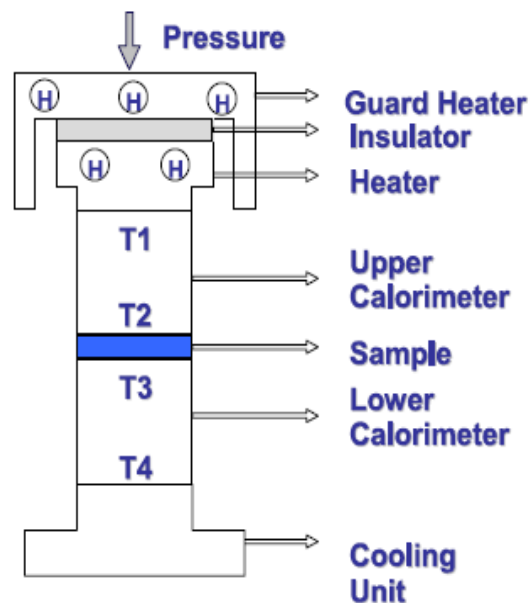
Second strategy

is to form a nanostructure from an intrinsically conductive material into a mechanically compliant morphology, such as Figure 29 (c) **vertically grown nanotubes** and (d) **vertically electrodeposited nanowires**. The fabrication process would be to build the nanostructured conductive material (e.g., **metals and graphite**) into a mechanically compliant morphology. Aligned arrays of continuous, conductive elements improve the effective thermal conductivity by providing **out-of-plane** heat transfer pathways.

Recent approaches have focused on synthesizing **Carbon nanotubes (CNTs)** into vertically aligned arrays. However, the CNT arrays show lower thermal conductivity values (of 10-50 W/m-K) than theoretical estimates, due to the **material's uncontrollable morphology during the growth process**, nanotube-nanotube contact resistances, and defects

“God made the bulk; the surface was invented by the devil.” said W. Pauli, recipient of the Nobel Prize in Physics in 1945 [14]. However,

- ASTM D5470 is a convenient, standardized tool to measure and compare performance of TIMs
- Measured **thermal impedance** at a given pressure is determined by:
 - Bulk thermal conductivity, and
 - Bond line thickness (BLT), and
 - Contact resistance at the interfaces
- Limitations:
 - In-situ reliability measurements
 - Caution when comparing published test results from one tester to another, one lab to another ...
 - ... particularly for thin bond-line, very low impedance measurements
 - Caution when translating lab test results to real world applications



Principles of Laser Flash Method

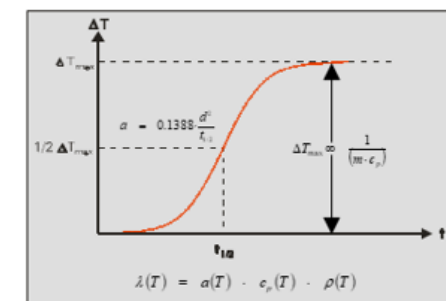
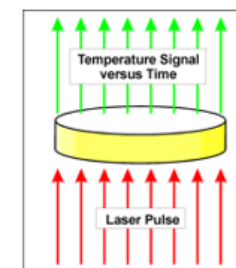
Thermal diffusivity, α is a measure of how quickly heat diffuses through a material.

$$\alpha = \frac{k}{\rho C_p}$$

k : Thermal Conductivity; ρ : Mass Density; C_p : Heat Capacity.
 α is a key material thermal property needed for accurate simulations and design.

In Laser Flash method, front face of a thin sample is heated by a single energy pulse from a laser source. Temperature rise on the back face is measured using an IR detector as a function of time. Comparison of the measurement with an analytical model (Parker, *et al.*, 1961) is carried out to determine thermal diffusivity.

Further, it is known that peak temperature rise in this measurement is proportional to heat capacity. Therefore, by comparison of the signal measured for a test sample with a standard sample of known heat capacity, one may determine heat capacity of the test sample. The equation above can then be used to determine thermal conductivity.



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 The University of Texas at Arlington, USA



<https://roadmap.inemi.org/ir/thermal-interface-materials>

Approaches to address Needs, Gaps and Challenges

Table 2 considers approaches to address the above needs and challenges. The evolution of these is projected out over a 10-year timeframe using technology readiness levels (TRLs).

In-table color key	Range of Technology Readiness Levels	Description
2	TRL: 1 to 4	Levels involving research
6	TRL: 5 to 7	Levels involving development
9	TRL: 8 to 9	Levels involving deployment

TECHNOLOGY ISSUE	POTENTIAL SOLUTIONS	EXPECTED TRL LEVEL*			
		TODAY (2024)	3 YEARS (2027)	5 YEARS (2029)	10 YEARS (2034)
Thermal Interface Materials					
TIMs ISSUE #1: Addressing voiding to reduce thermal impedance/ resistance in solder TIMs	Development of novel materials and processes	4	6	7	8
TIMs ISSUE #2: Voiding in other TIMs (non-metal TIMs) (e.g., thermal greases, gels, pads, TC adhesives) (Voiding is more of an issue with adhesives.)	Development of novel materials and processes	2	4	6	7
TIMs ISSUE #3: Bleeding of TIM (gel and pad type materials- silicones and urethanes) (TIM 2 and TIM 0 materials)	Development of novel materials and processes	2	4	6	7
TIMs ISSUE #4: TIM Pump-out/bleed-out/dry-out	Development of novel materials and processes	4	6	7	8



<https://roadmap.inemi.org/ir/thermal-interface-materials>

Approaches to address Needs, Gaps and Challenges

Table 2 considers approaches to address the above needs and challenges. The evolution of these is projected out over a 10-year timeframe using [technology readiness levels \(TRLs\)](#).

In-table color key	Range of Technology Readiness Levels	Description
2	TRL: 1 to 4	Levels involving research
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9	TRL: 8 to 9	Levels involving deployment

Conclusions

1. Addressing voiding to reduce thermal impedance/resistance in solder TIMs
2. Addressing voiding in other TIMs (non-metal TIMs) (e.g., thermal greases, gels, pads, TC adhesives) (Voiding is more of an issue with adhesives.)
3. Bleeding of TIMs (e.g., gel and pad type materials- silicones and urethanes) (TIM 2 and TIM 0 materials)
4. TIM pump-out/bleed-out/dry-out

TECHNOLOGY ISSUE	POTENTIAL SOLUTIONS	EXPECTED TRL LEVEL*			
		TODAY (2024)	3 YEARS (2027)	5 YEARS (2029)	10 YEARS (2034)
Thermal Interface Materials	Development of stable materials (no filler separation)	2	3	4	5
	Development of stable materials (No viscosity changes)	2	3	4	5
TIMs ISSUE #5: Material Stability (Non-solder TIMs)	Development of agreed upon inspection methods	3	4	5	7
	Development of methodology for high-volume manufacturing	3	4	5	7
	Standardization of Inspection	3	4	5	7
TIMs ISSUE #6: Inspection of TIMs	PnP/insertion process standard/guidelines	2	3	5	7



TIM evaluation and reliability

Test Method	Standard	Primay TIM Type
Bulk thermal conductivity	ASTM D-5470 (30, 85 °C)	All
Shelf-life	-40 to +35 °C typical	All
Drop-shock	JESD22-B104C	TIM1, TIM1.5
Reflow resistance	3, 4 or 5x reflow up to 260 °C	TIM1 (BGA)
Thermal shock	JESD22-A106B	TIM1
Thermal cycling	JESD22-A104E	TIM1, TIM1.5
HAST	JESD22-A118	TIM1, TIM1.5
HTOL	JESD22-A108C	TIM1, TIM1.5
Power cycling	Up to 1000 W/cm ²	TIM1.5
Vibration	JESD22-B103B	TIM1, TIM1.5



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Date of webinar: November 25, 2025

5.5 Device qualification requirements

Table 1 — Device qualification tests

Stress	Ref.	Abb.	Conditions	Requirements	
				# Lots / SS per lot	Duration / Accept
High Temperature Operating Life	JESD22-A108, JESD85	HTOL	$T_j \geq 125^\circ\text{C}$ $V_{cc} \geq V_{ccmax}$	3 Lots / 77 units	1000 hrs / 0 Fail
Early Life Failure Rate	JESD22-A108, JESD74	ELFR	$T_j \geq 125^\circ\text{C}$ $V_{cc} \geq V_{ccmax}$	See ELFR Table	$48 \leq t \leq 168$ hrs
Low Temperature Operating Life	JESD22-A108	LTOL	$T_j \leq 50^\circ\text{C}$ $V_{cc} \geq V_{ccmax}$	1 Lot / 32 units	1000 hrs / 0 Fail
High Temperature Storage Life	JESD22-A103	HTSL	$T_a \geq 150^\circ\text{C}$	3 Lots / 25 units	1000 hrs / 0 Fail
Non-Volatile Memory Cycling Endurance	JESD22-A117	NVCE	25°C and $85^\circ\text{C} \geq T_j \geq 55^\circ\text{C}$	3 Lots / 77 units	Up to Spec. Max Cycles per note (e) / 0 Fails
Data Retention for Non-Volatile Memory: High Temperature	JESD22-A117	HTDR	Option 1: $T_j = 100^\circ\text{C}$	3 Lots / 39 units	Cycles per NVCE ($\geq 55^\circ\text{C}$) / 96 and 1000 hrs / 0 Fail / note (f)
			Option 2: $T_j \geq 125^\circ\text{C}$		Cycles per NVCE ($\geq 55^\circ\text{C}$) / 10 and 100 hrs / 0 Fail / note (f)
Non-Volatile Memory Low-Temperature Retention and Read Disturb	JESD22-A117	LTDR	$T_a = 25^\circ\text{C}$	3 Lots / 38 units	Cycles per NVCE (25°C) / 500 hrs / 0 Fail / note (g)
Latch-Up	JESD78	LU	Class I or Class II	1 Lot / 3 units	0 Fail
Electrical Parameter Assessment	JESD86	ED	Datasheet	3 Lots / 10 units	Ta per datasheet
Human Body Model ESD	JS-001	ESD-HBM	$T_a = 25^\circ\text{C}$	3 units	Classification
Charged Device Model ESD	JESD22-C101	ESD-CDM	$T_a = 25^\circ\text{C}$	3 units	Classification
Accelerated Soft Error Testing	JESD89-2, JESD89-3	ASER	$T_a = 25^\circ\text{C}$	3 units	Classification
"OR" System Soft Error Testing	JESD89-1	SSER	$T_a = 25^\circ\text{C}$	Minimum of 1E+06 Device Hrs or 10 fails.	Classification

Stress	Ref.	Abb.	Conditions	Requirements	
				# Lots/SS per lot	Duration/Accept
Temperature Cycling	JESD22-A104	TC	-55°C to $+125^\circ\text{C}$ or alternatives with temperature justification	3 Lots / 25 units	700 cycles / 0 Fail
Bond Pull Strength ³	M2011	BPS	Characterization	1 lot / 30 bonds / 5 units	$Ppk \geq 1.66$ or $Cpk \geq 1.33$
Bond Shear ³	JESD22-B116	BS	Characterization	1 lot / 30 bonds / 5 units	$Ppk \geq 1.66$ or $Cpk \geq 1.33$
Solderability	M2003 JESD22-B102	SD	Characterization	3 lots / 22 leads	0
Solderball Shear	JESD22-B117	SBS	Characterization	5 units	10 balls per unit
Mechanical Shock ¹	JESD22-B104 M2002	MS	Y1 plane only, 5 pulses, 0.5 ms duration, 1500 g peak acceleration	3 lots / 39 units	TEST after CA
Vibration Variable Frequency ¹	JESD22-B103 M2007	VVF	20 Hz to 2 kHz (log variation) in > 4 minutes, 4X in each orientation, 50g peak acceleration	Sequence from MS	TEST after CA
Constant Acceleration ¹	M2001	CA	Y1 plane only, 30 kg force <40 pin packages, 20 kg for > 40 pins.	Sequence from VVF	Test at room temp. pre & post -stress
Gross /Fine Leak	JESD22-A109 M1014	GFL	Any fine test followed by gross test. May also be performed at the beginning of the mechanical sequence before mechanical shock test		
External Visual		EV			1
Physical Dimensions		PD		1 lot / 30 units	2
Lead Integrity		LI		45 leads; min of 5 units	1
Lid Torque		LT		1 lot / 5 units	1
Internal Water Vapor	MIL-STD 883 M1018	IWVC	Residual Gas Analysis of Package Cavity Water Vapor Content	3 lots / 1 unit ea.	Characterization
Tin Whisker Acceptance	JESD22-A121	WSR	Characterization per JESD201	See JESD201	See JESD201, Based on Appropriate Classification

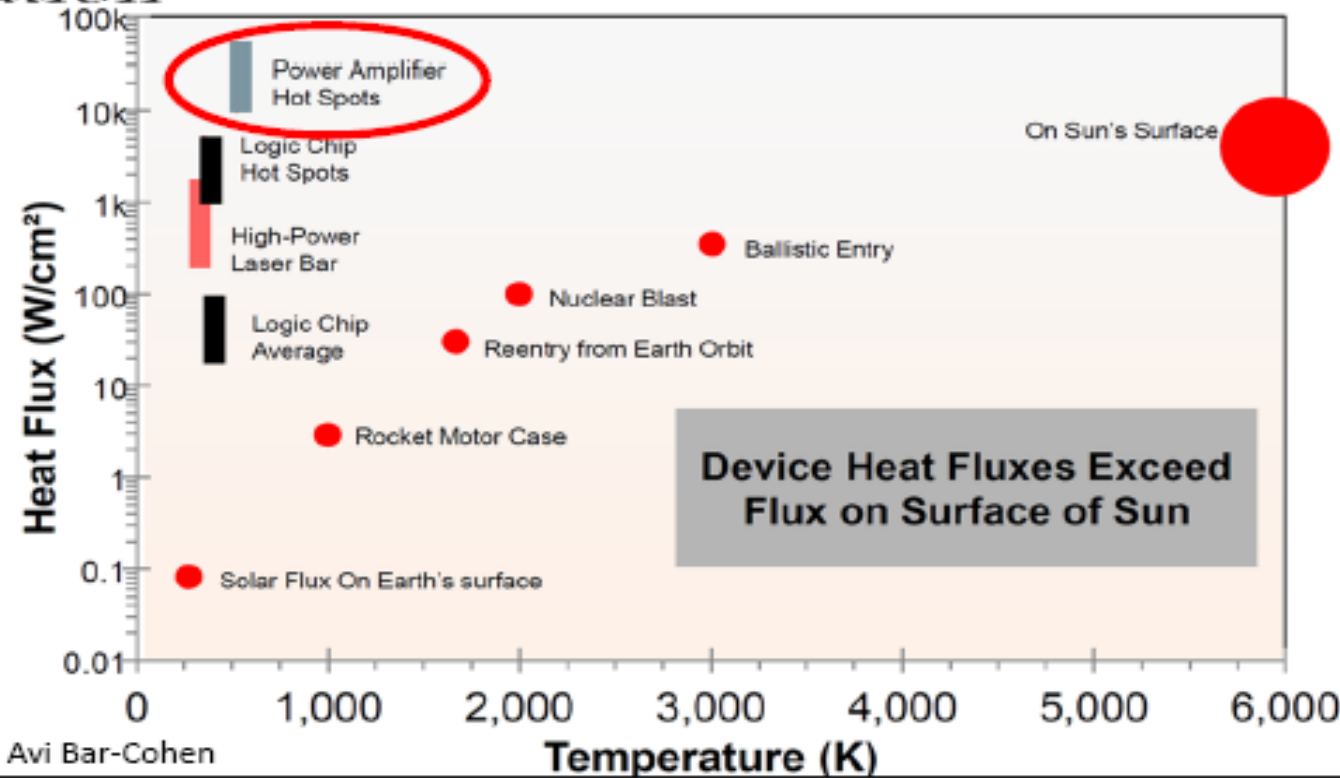
¹ Based upon manufacturer specification or applicable procurement documents.

² Reference applicable JEDEC spec, supplier specification, or procurement document for significant dimensions and tolerances.

³ $Ppk = \frac{\bar{x} - LSL}{3\sigma}$, $\frac{USL - \bar{x}}{3\sigma} \geq 1.66$. Process capability data may be substituted for Ppk with data on more than 30 lots with the requirement that $Cpk \geq 1.33$.

The thermal requirements on packaging are becoming more demanding

Thermal Management Reaching Limits of Imagination



Source: Raytheon, Avi Bar-Cohen





The thermal requirements on packaging are becoming more demanding

Material Requirements³

Thermal Requirements³

Power Electronics/ Electrification Packaging Material Requirements			
Attributes	Current	5 years	10-15 years
Packaging platforms	Laminate & LF based (QFN, LGA, BGA, SIP) Power QFN, specialized package (TO)	Laminate & LF based (QFN, LGA, BGA, SIP) Flip chip/ (HD) FOWLP	Laminate & LF based (QFN, LGA, BGA, SIP) Contact-less package (example: EM energy transfer) Flip chip/ (HD) FOWLP/PLP
Pkg Dimensions	2x2 to 7x7mm	1x1 to 2x2 mm	Chip Scale
Device Material	Si	GaN, SiC	GaN, SiC
Max Junction Temperature	175C	200C	200C and beyond
Max Voltage	1300V	>2000V	TBD
Interconnect/via material/surface finish	WB- Au wire, Cu wire, Multiple Cu vias, Cu Pillar, OSP, ENIG, ENEPIG, Electrolytic NiAu	WB- Cu wire, OSP, SOP, ENIG, ENEPIG, Electrolytic NiAu, Cu Pillar interconnect, Thicker Cu-via/ Larger surface area (clips)	Cu Pillar, OSP, SOP, ENIG, ENEPIG, Electrolytic NiAu New Materials (graphite, etc)
Die attach materials	Epoxy, Solder (Leadfree & Leaded) Sintering Adhesive (Pb-free)	Sintering Adhesive (Pb-free) Diamond and Graphite loaded materials	TLPS (Transient Liquid Phase Sintering) New Materials (graphite, etc.)

Diamond and Graphite loaded materials

Table 3: Thermal Management Requirements. (Green: Solution available for manufacturing. Yellow: Additional development work needed. Red: Significant development effort needed for HVM. White: Information only)

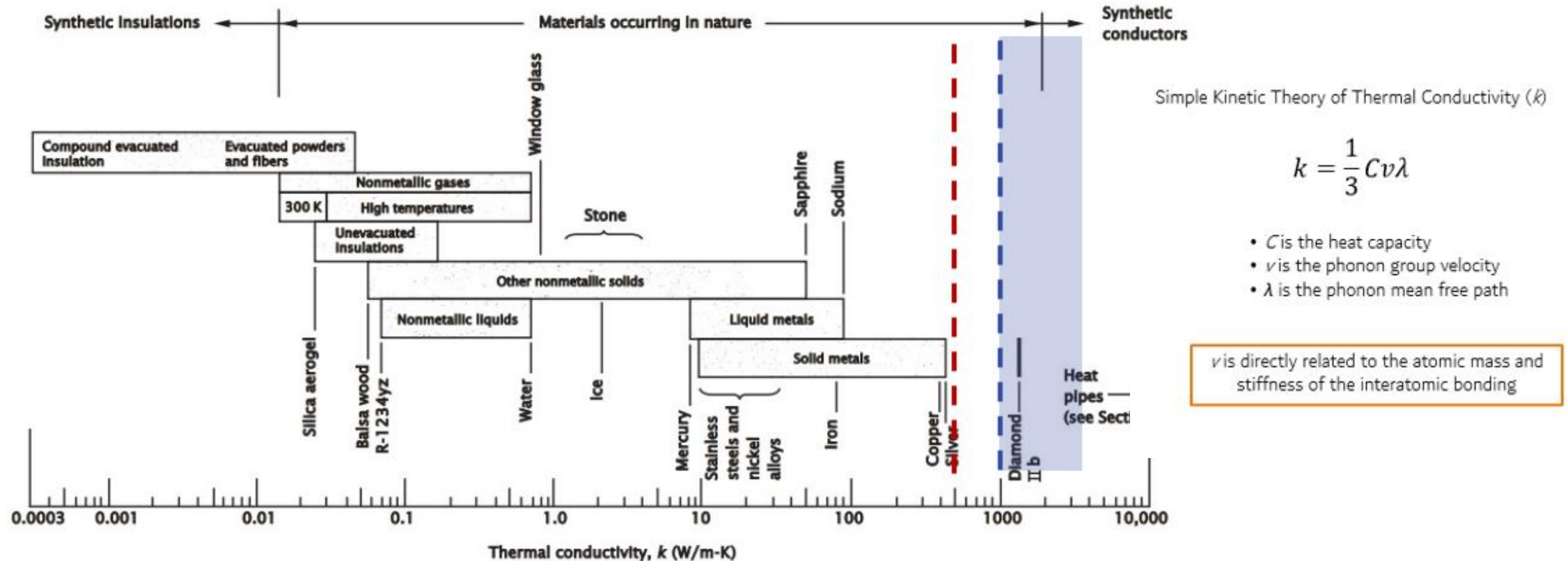
Thermal Management			
Ingredients	>2023	>2028	2033 and +
Thermal Interface Materials (TIMs)	Thermal interface materials with low thermal resistance and high resilience to package and board level assembly techniques (50% or greater reduction especially in effective thermal resistance under reliability conditions)		
Heat Spreaders	High conductivity (2x or greater than copper), low-cost materials for interfacing which are capable of being cost effectively manufactured into integrated heat spreaders on the package	High conductivity spreaders for integration within a 3D stack which are process compatible. Thermal conductivities ≥ 3000 W/m/K with a thickness of 50mm to 200mm	

Thermal conductivities ≥ 3000 W/m/K with a thickness of 50mm to 200mm

3. National Institute of Standards and Technologies. Microelectronic and Advanced Packaging Technologies Roadmap. Interim Edition 2023.



Metallic packaging is fundamentally limited to $k \sim 10^2$ W/mK and few materials can tap into the 10^3 W/mK range.



G. Chen. Nanoscale Energy Transport and Conversion. Oxford University Press 2005.

Chapter 15: Materials and Emerging Research Materials



NANOSCALE AND MICROSACLE THERMOPHYSICAL ENGINEERING
<http://dx.doi.org/10.1080/15567265.2017.1296910>



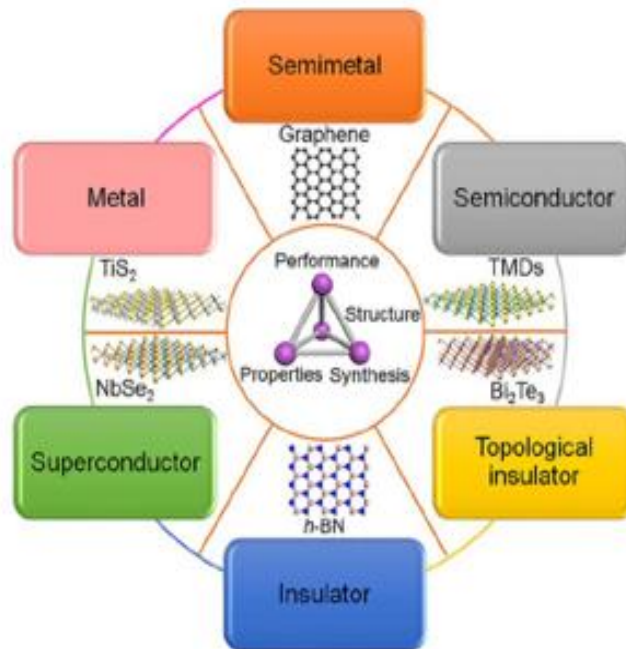
Enhanced Thermal Conduction Through Nanostructured Interfaces

Woosung Park^a, Aditya Sood^{a,b}, Joonsuk Park^b, Mehdi Asheghi^a, Robert Sinclair^b, and Kenneth E. Goodson^a

^aDepartment of Mechanical Engineering, Stanford University, Stanford, California, USA; ^bDepartment of Materials Science and Engineering, Stanford University, Stanford, California, USA

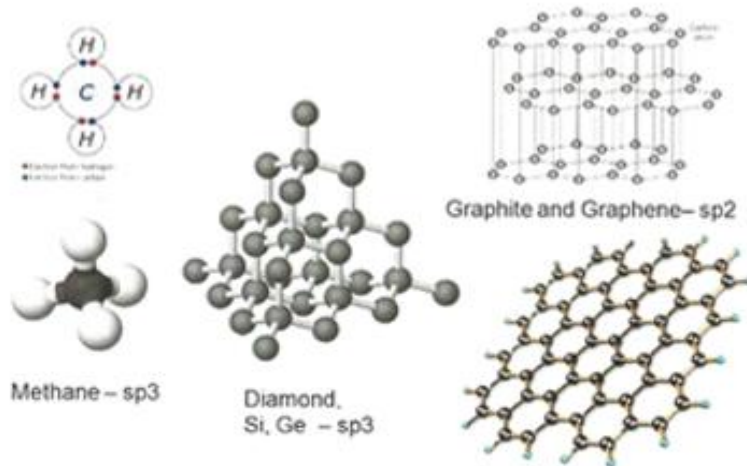
“ Interfaces strongly influence thermal transport in nanostructured systems and have become a primary impediment to thermal management in many applications such as nanoelectronics energy conversion devices and nano-photonics. Much research has targeted an improved understanding of the impact on the thermal interfacial resistance of the **phonon density-of-states** mismatch near interfacial defects such as vacancies and dislocations interface roughness **phonon inelastic scattering** and **electron-phonon interactions** among other factors. Current approaches to enhancing interfacial thermal transport rely primarily on improving interface quality, accomplished by reducing **surface roughness and mitigating near-interfacial defects or through the introduction of vibrational and lattice-matching interlayers**. While the specifics vary, the unifying theme among existing approaches is that they involve planar interfaces, where the heat flux vector is everywhere parallel to the surface normal. In order to push the limits with planar interfaces, new approaches are required that can enhance thermal transport beyond what is currently possible”

2D Class Of Materials Can Support Many Device Types



Why are carbon materials (graphene, graphite, carbon nanotubes, diamond) seemingly alone on many roadmaps for advanced passive/conductive thermal packaging?

Covalent Structures



Carbon has electrically insulating and conducting forms

$$\omega = \sqrt{\frac{k}{m}}$$



From mechanics, the vibrational frequency (ω) of a harmonic oscillator is related to the atomic mass and stiffness of the interatomic potential.

Carbon has light atoms and stiff bonds

$$k = \sum_{\text{modes}} c v \lambda$$

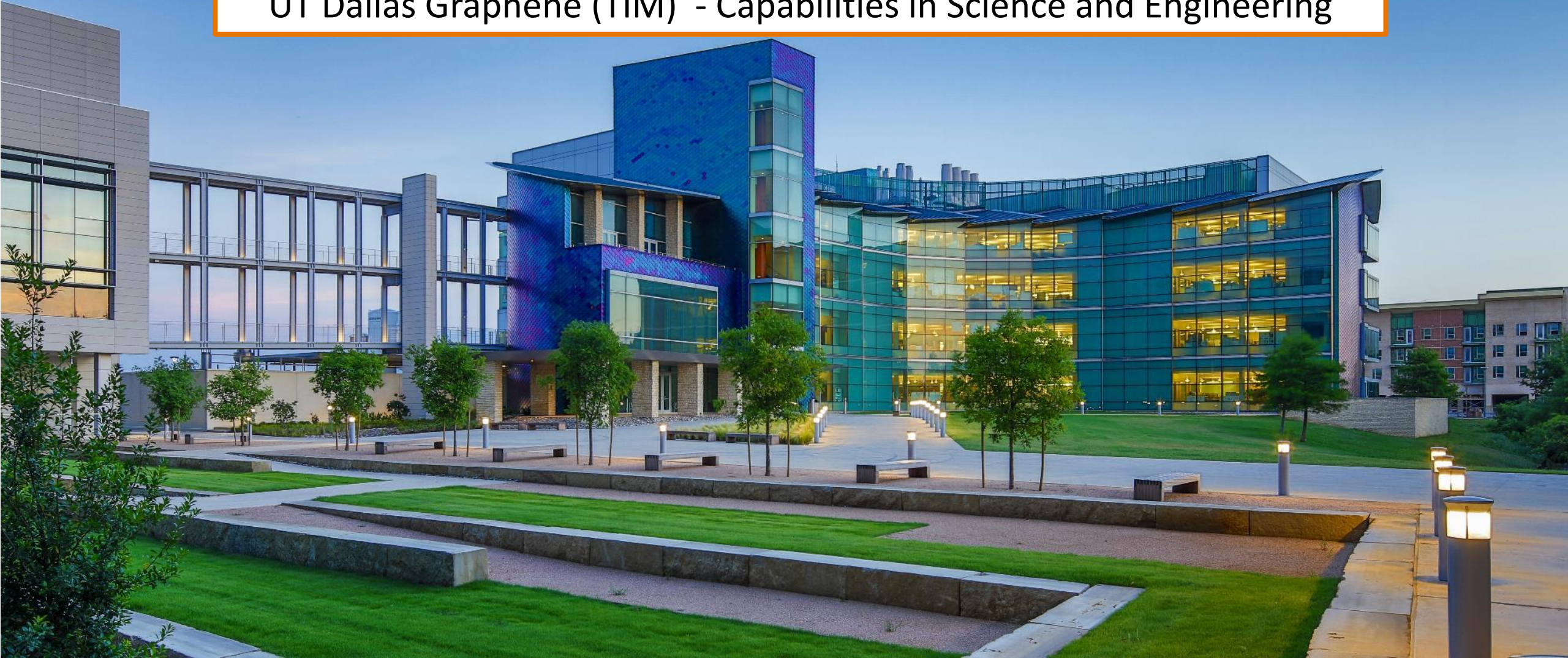
Heat Capacity Phonon Mean-Free Path

From kinetic theory, the thermal conductivity is related to the group velocity ($v \propto \omega$) of the phonons.

Carbon has high thermal conductivity

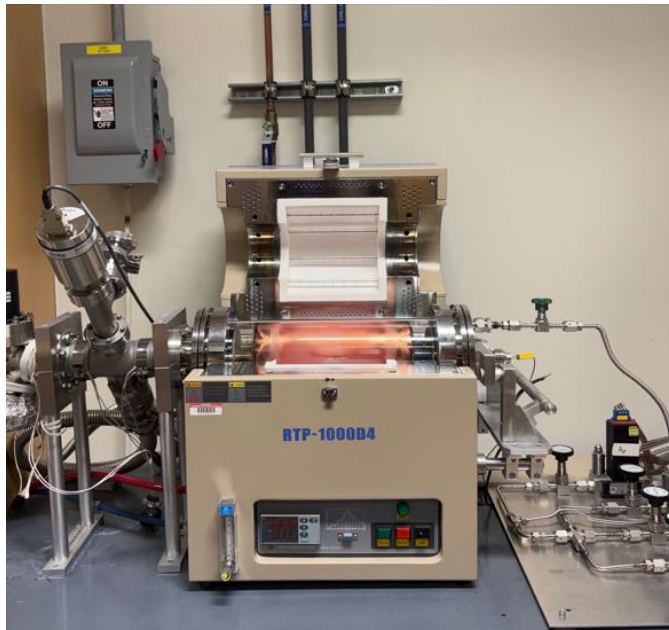
Many synthetic conductors, like heat pipes or microfluidics, may not be compatible with highly integrated systems.
For example, back-end-of-the-line compatibility for monolithic 3D integration.

UT Dallas Graphene (TIM) - Capabilities in Science and Engineering

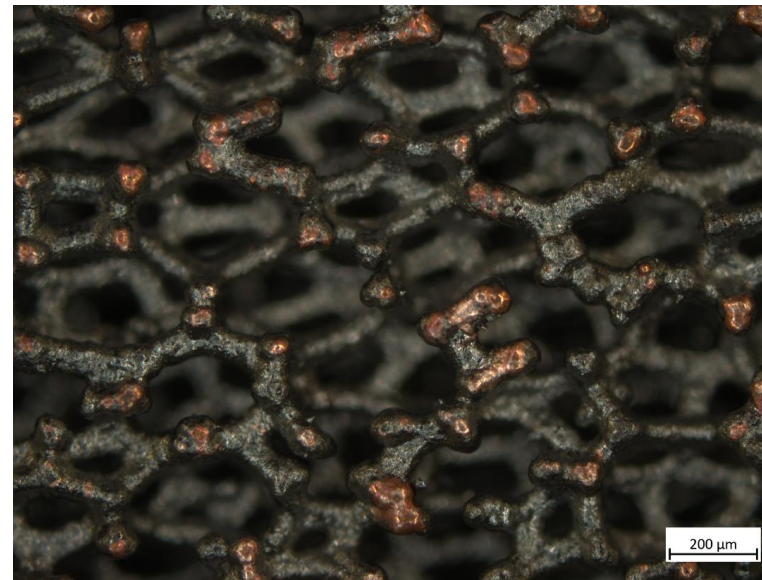


Graphene and graphite can be grown directly on 3D metal templates.

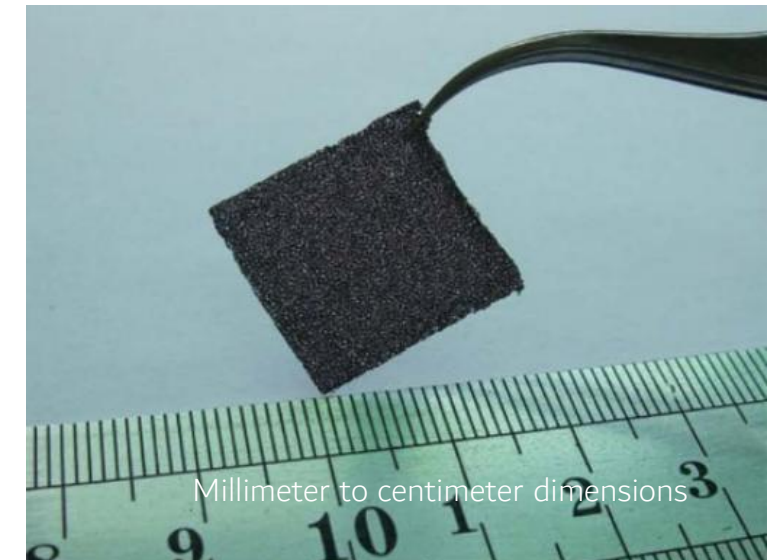
Chemical Vapor Deposition



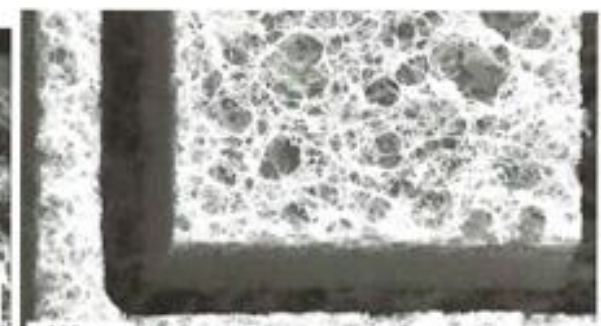
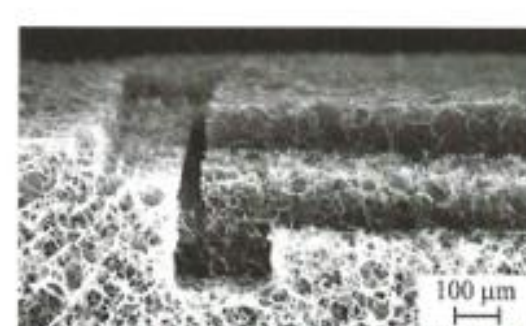
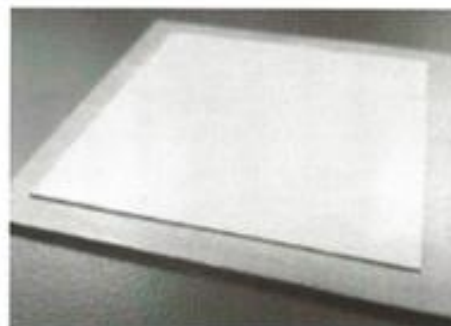
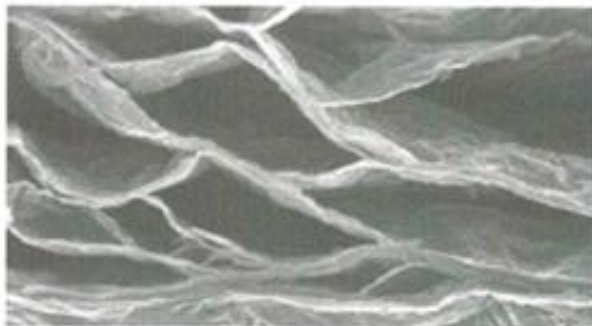
Microscopic Image



Macroscopic Image



Flakes, sheets, foams

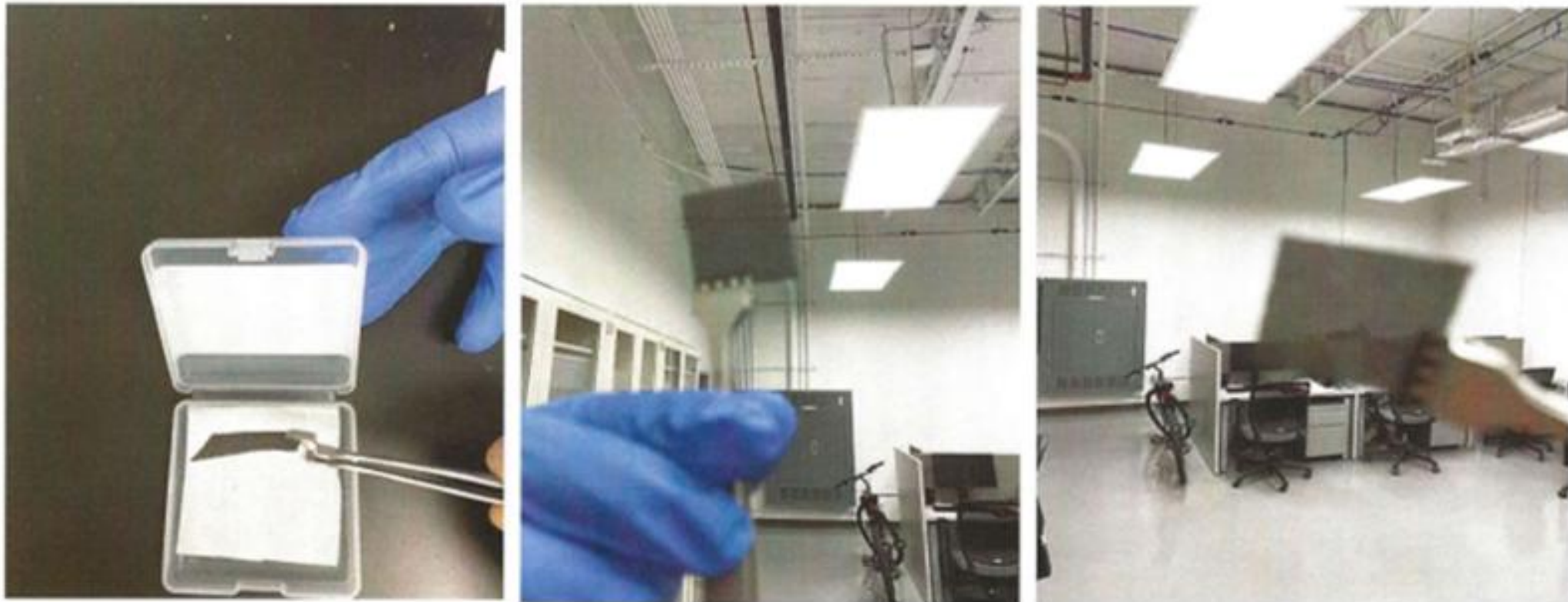


Advanced Thermal Interface Materials: Assembly and Integration for System in Package

Kevin Brenner
Southern Methodist University
Department of Electrical and Computer Engineering

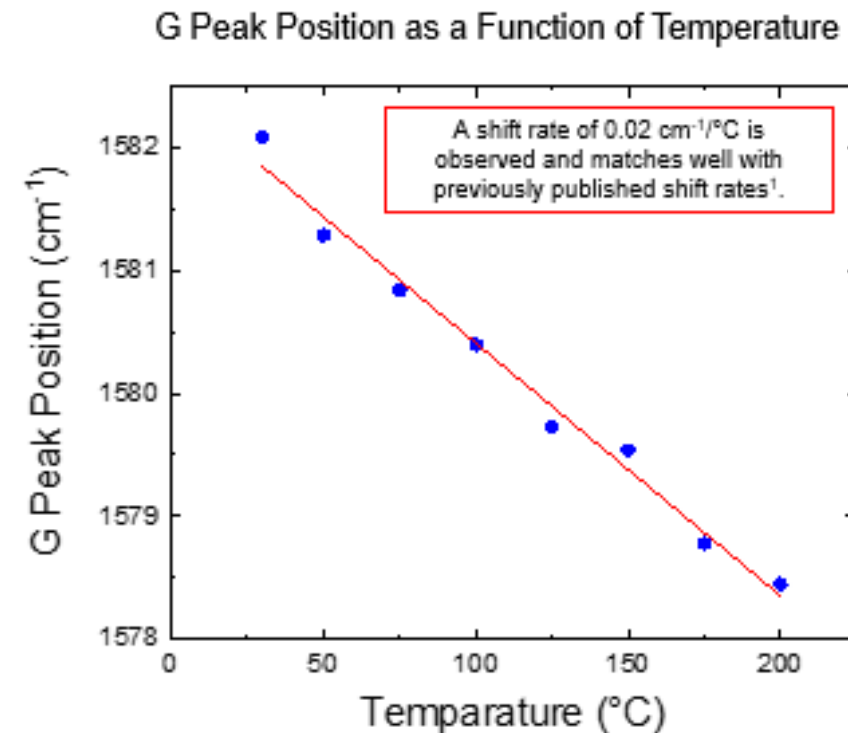
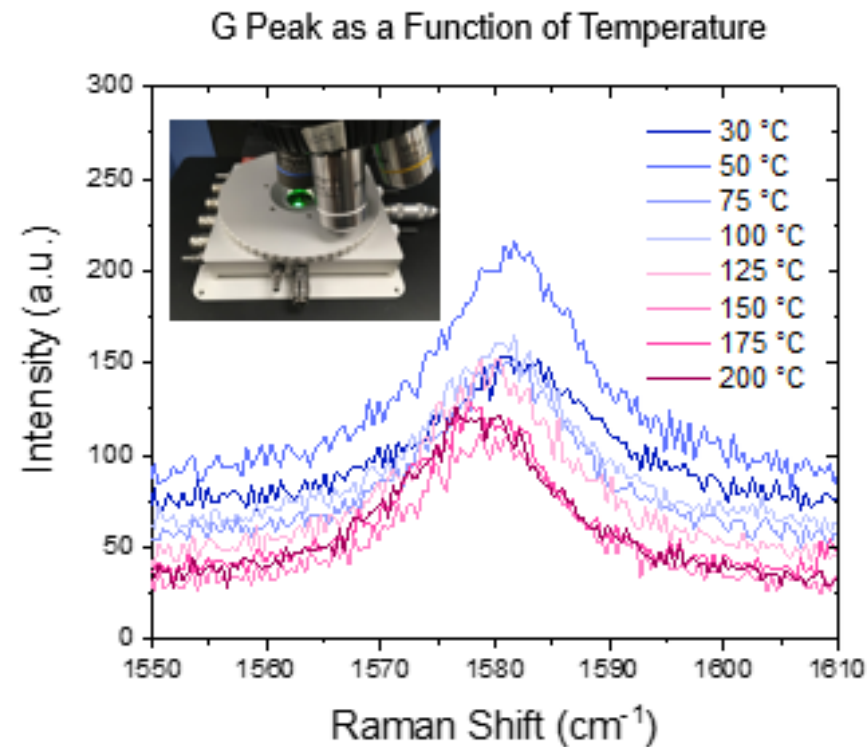
Graphene for Packaging Applications on High-Power/High-Frequency Products

(Metallic foams coated with Graphene – no X-Y size restrictions)



The Raman laser is now a simultaneous **heater**, **thermometer**, and **characterizer** of structural/chemical details!

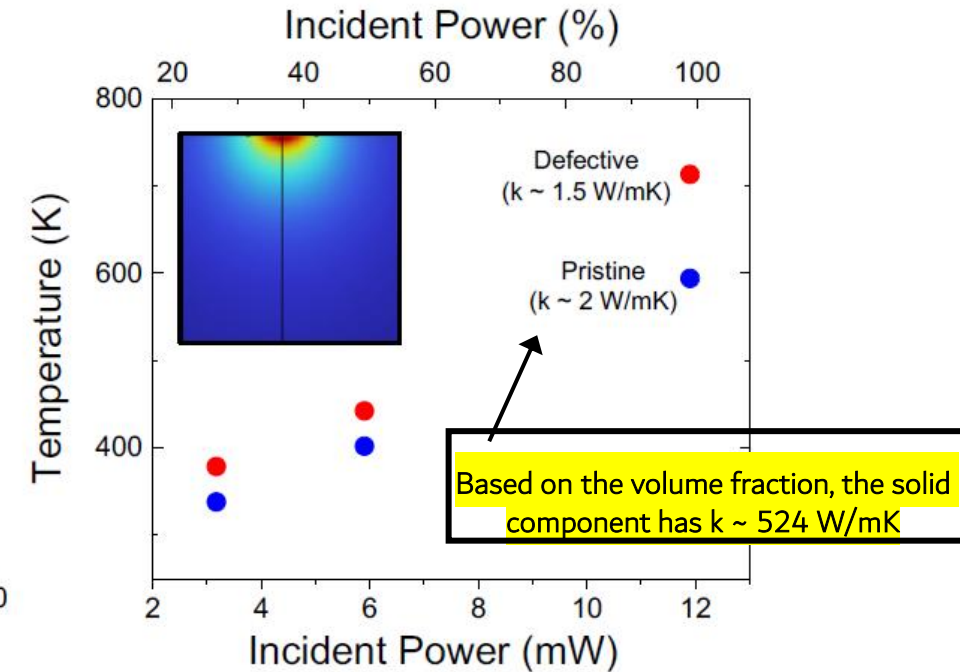
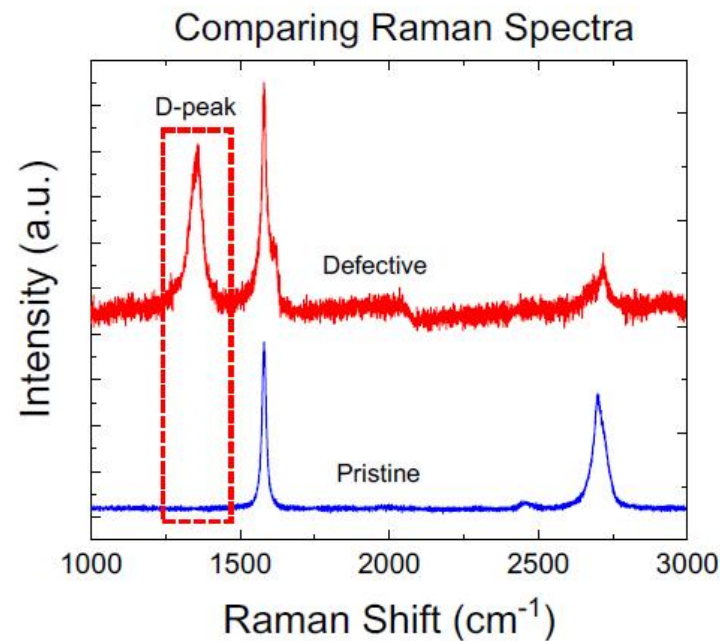
All measurements show the peak position at room temperature (blue) and heated (red). The heated temperature is determined by the shift between blue and red peaks. The calibration for the peak shift versus temperature is shown below.



1. I. Calizo, et al., "Temperature Dependence of the Raman Spectra of Graphene and Graphene Multilayers." Nano Letters 2007.

The thermal conductivity and material quality can be **simultaneously characterized** for carbon-based TIMs.

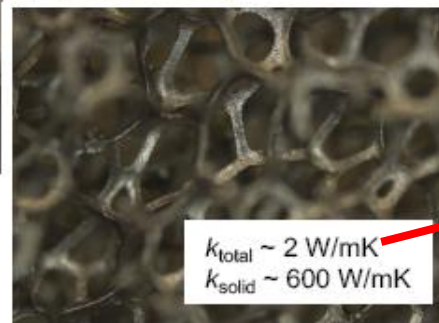
Graphite-Metal Composite



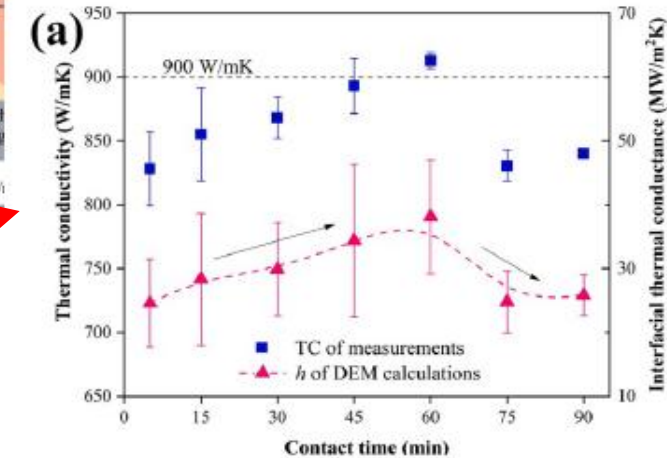
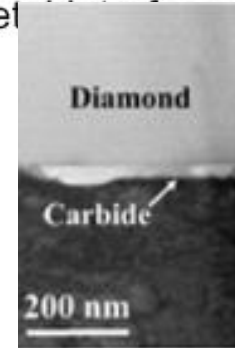
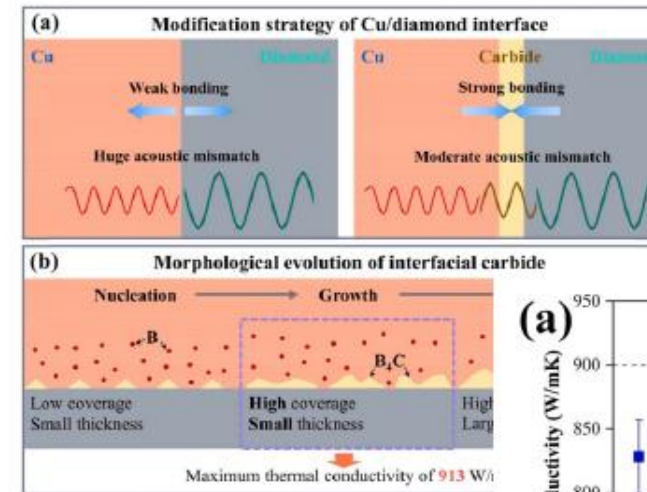
Raman spectroscopy is one of the few metrologies that can uncover the underlying nature of changes in thermal conductivity. For example, correlating it with a wide range of material properties (defects, strain, etc.)

There are a variety of promising avenues for carbon-based thermal packaging.

Graphene/Graphite Grown Directly on Metals Templated Growth?



Successful Engineering of Carbon-Metal Interfaces can be controlled?



7. M. Pettes, et al., "Thermal Transport in Three-Dimensional Foam Architectures of Few-Layer Graphene and Ultrathin Graphite." Nano Letters 2012.

8. Y. Zhang, et al. Manipulating in-situ discrete carbide interlayer to achieve high thermal conductivity in Cu-B/diamond composites. Materials Today Communications 2022.

Solving the Dispersion Problem by Functionalization



AMINATED GRAPHENE-FILLED GLASS FIBER COMPOSITES FOR ENHANCED MECHANICAL PROPERTIES

A. Ning Bian^a, B. Ashutosh Shrivastava^b, C. Gabriel More-Torres^c, D. Runyu Zhang^a, E. Samsuddin Mahmood^d, F. Duck J Yang^d, G. Hongbing Lu^{a(*)}

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^d GrapheneTX Inc., 619 Mogonye Lane, Elgin, TX 78621, United States

(*)Hongbing.lu@utdallas.edu

Acknowledge the support: NSF 2219347 and from GrapheneTX Inc.



Powder*



Masterbatch



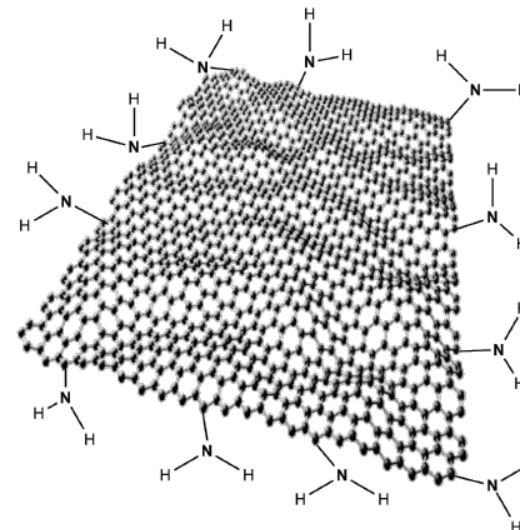
Liquid dispersion



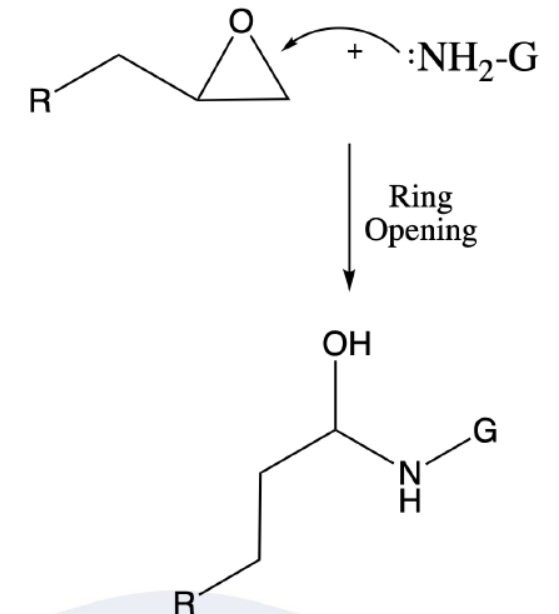
P. Coating/Paint



Aminated Graphene



The amine groups on graphene generate repulsion with the amine groups in the hardener solution



Amine (NH_2 -) groups in graphene react with epoxy groups to form strong covalent bonds

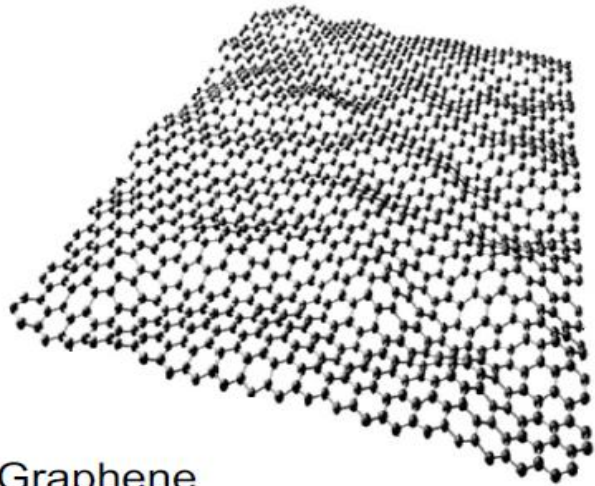
Slide N° 6



ICEM20
Porto, 2-7 July 2023

20th International Conference on
EXPERIMENTAL MECHANICS

Graphene or Graphite



Graphene

Less than 10 atomic layers

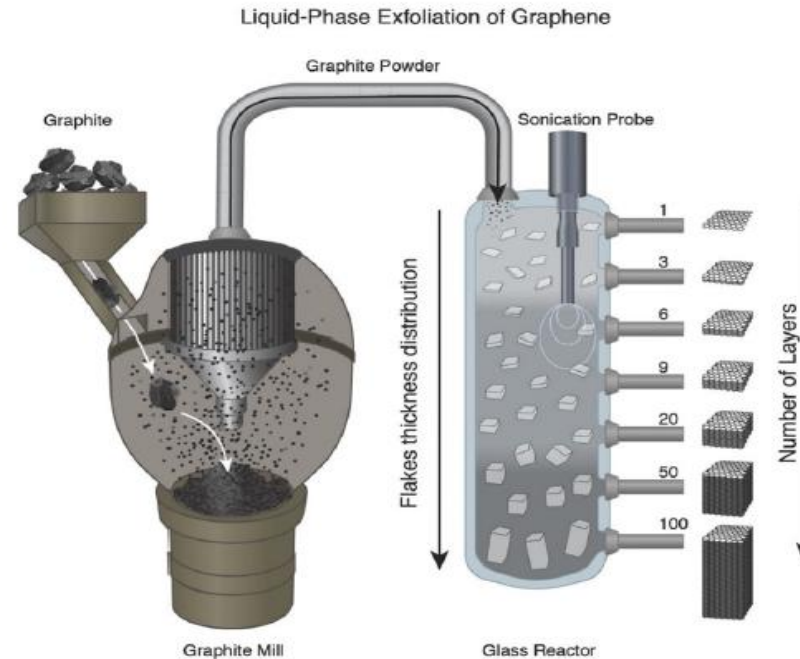
Tensile Strength: 130 GPa

Surface area: 2630 m²/g

Thermal conductivity:

3000 Wm⁻¹K⁻¹

Lightweight: 0.77 mg/m²



Most commercially available graphene products are graphite or graphene derivatives, e.g., GO, rGO, rather than graphene.

Adv. Mater. 2018, 30, 1803784

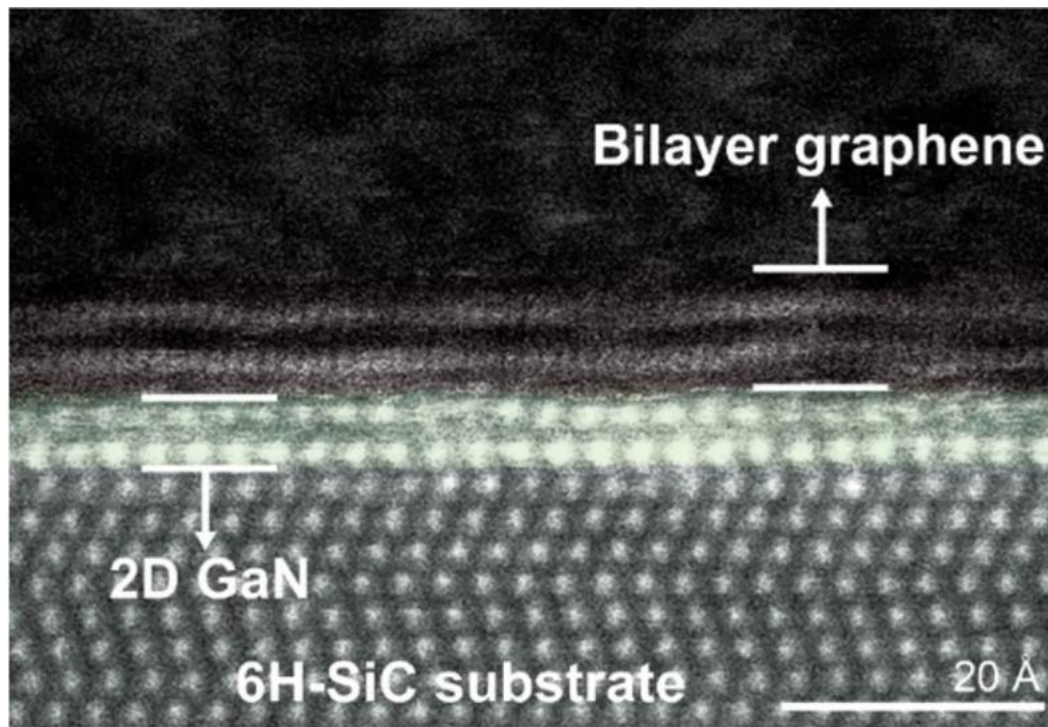
Nature 562, 502-503 (2018)

Slide Nº 5

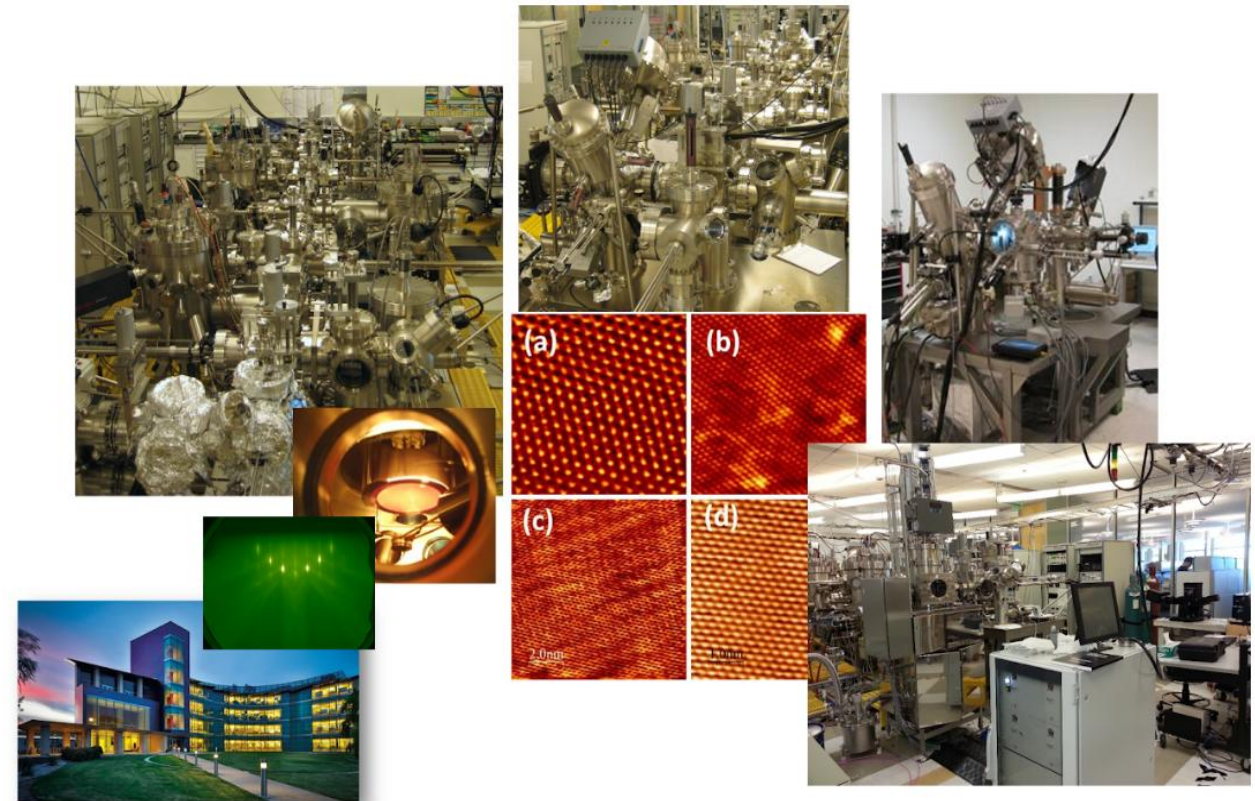
- US Patent 11,111,150 B2
- US Patent Application 18/701,465
- US Patent 12,065,762
- US Patent 12,006,594
- US Patent 10,435,821
- US Patent 12,421,631 B2
- Additional applications are in process of filling

UT Dallas (TIM) Capabilities in Science and Engineering

- ❖ Create large scale (area) dimensional TIM (sq. inches) for BLD 1 mil to 10 mil on metallic mesh
- ❖ Provide compression capability of TIM to accommodate for large die and substrate warpage due to CTE
- ❖ Provide 600+ (W/mK) foams for X-Y-Z dimensional thermal conductivity
- ❖ Provide Metallic mesh and Graphitic foams impregnable with Epoxy materials for die attach
- ❖ Provide Graphitic interface functionalization for Graphene wetting with Polymers (Epoxy and Molding compounds)
- ❖ Top and Bottom of TIM metallization options available for die back-side to substrate metallurgical interface
- ❖ Laser patterning of Graphene foam for die to die 3D stacking for MCM applications.
- ❖ Non-destructive Thermal conductivity and Quality determined for TIM via micro-Raman spectroscopy



Welcome to the Addou Lab



Wallace Group

<https://sites.google.com/view/robert-m-wallace/home>

<https://sites.google.com/view/robert-m-wallace/home/recent-research>



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Cpbojkov@outlook.com

For further discussion, please reach out to us. We are happy to exchange ideas, answer questions, and explore potential collaborations.