

Cu-Cu Hybrid Bonding and Glass Packaging

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- Introduction
- Cu-Cu Hybrid Bonding
- Glass Packaging
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Advanced Packaging in Artificial Intelligence (AI) Era

In the past

The performance has been driven by Moore's Law. Today, 2nm is in high volume manufacturing.

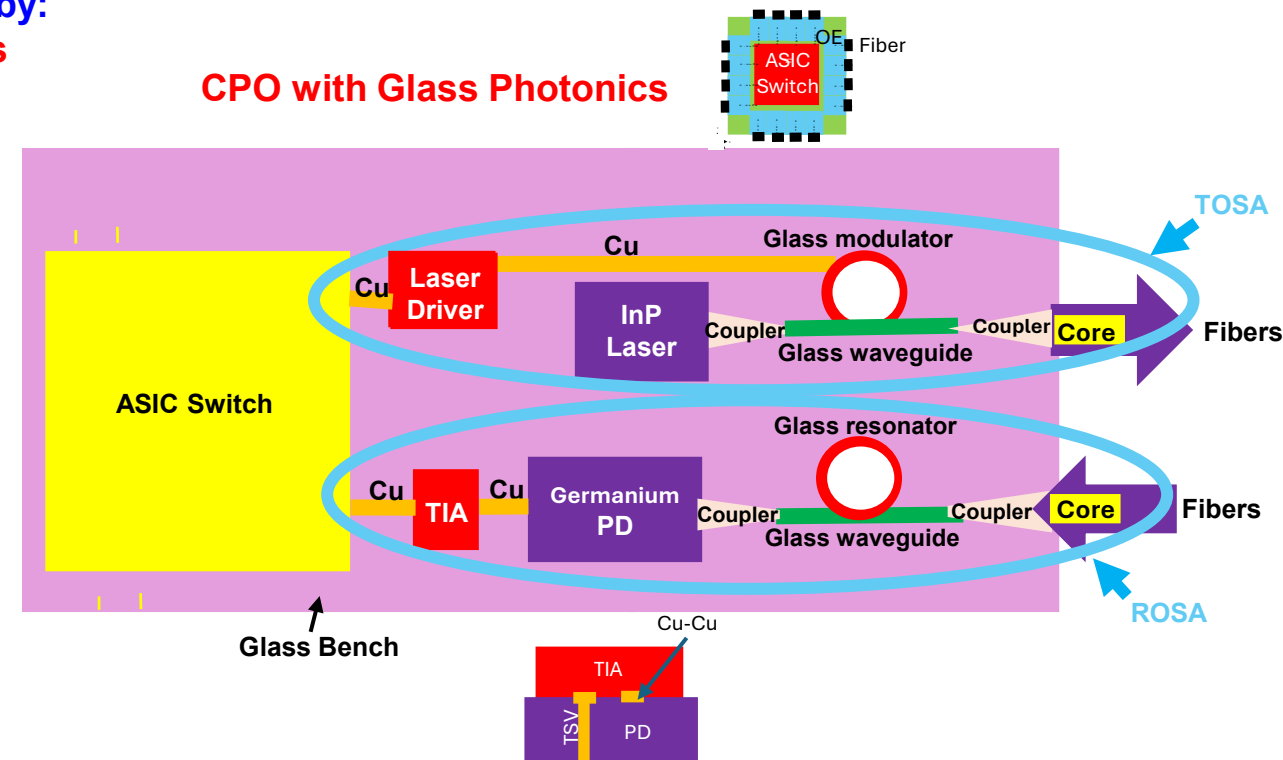
Now and the future

The performance is not only driven by purely Moore's Law but also by:

- how the chips are partitioned and split into smaller chiplets
- how the chiplets are stacked
- how the chiplets are interconnected
- how the chiplets are cooled
- how the chiplets are packaged

The methods, among others, are:

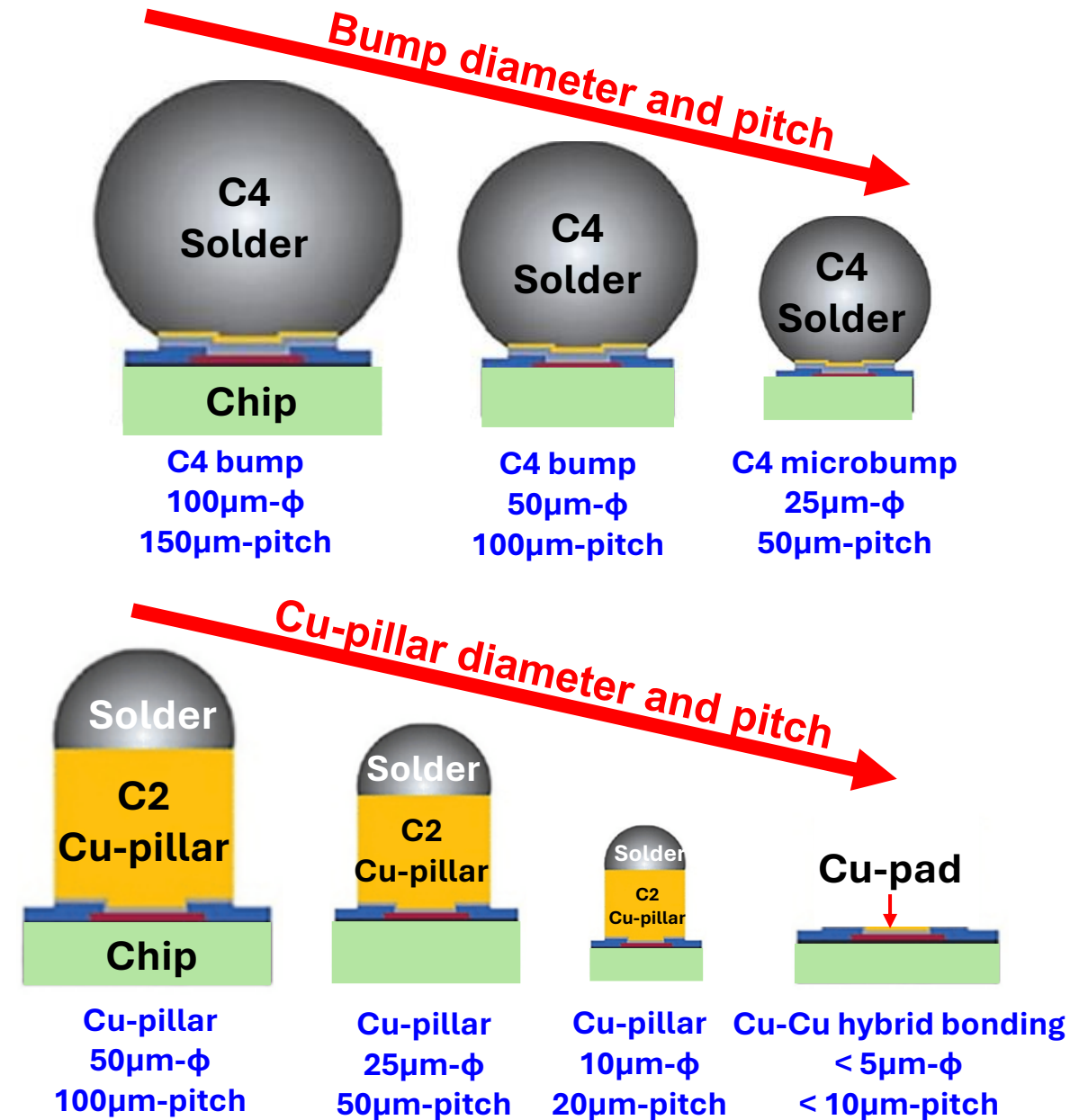
- Chiplets heterogeneous integration [1, 2, 3, 4, 5, 7]
- Bridges connecting chiplets [1, 2, 3, 4]
- FOWLP/FOPLP, TCB, Cu-Cu hybrid bonding [1, 2, 3, 4, 5, 8]
- Panel-level packaging [1, 8]
- Glass packaging [1, 2]
- Co-packaged optics with Si/Glass photonics [1, 2]
- Efficient power delivery
- Superior thermal management [2]
- Innovative materials and processes [1 - 10]
- etc.



- [1] Lau, J. H., and K. N. Chiang, *Hybrid Bonding, Glass, and AI-Assisted Simulation for Chiplets Heterogeneous Integration*, (547 pages), Springer, 2026.
- [2] Lau, J. H., and X. Fan, *Hybrid Bonding and Thermal Management for Chiplets and Heterogeneous Integration*, (645 pages), Springer, April 2025.
- [3] Lau, J. H., *Flip Chip, Hybrid Bonding, Fan-In, and Fan-Out Technology*, (501 pages), Springer, 2024.
- [4] Lau, J. H., *Chiplet Design and Heterogeneous Integration Packaging*, (525 pages), Springer, 2023.
- [5] Lau, J. H., *Semiconductor Advanced Packaging*, (498 pages), Springer, 2021.
- [6] Lau, J. H., and N. C. Lee, *Assembly and Reliability of Lead-Free Solder Joints*, (527 pages), Springer, 2020.
- [7] Lau, J. H., *Heterogeneous Integrations*, (367 pages), Springer, 2019.
- [8] Lau, J. H., *Fan-Out Wafer-Level Packaging*, (303 pages), Springer, 2018.
- [9] Lau, J. H., *3D IC Integration and Packaging*, (458 pages), McGraw-Hill, 2016.
- [10] Lau, J. H., *Through-Silicon Via (TSV) for 3D Integration*, (487 pages), McGraw-Hill, New York, 2013.

**Hybrid Bonding is one of the
Flip Chip Bumpless
Assembly Technologies**

Trends in Flip Chip Interconnects



The Origin of Cu-Cu Hybrid Bonding

- Between 2000 and 2001, Fountain, Engquist, Tong, and several others founded **Ziptronic**.
 - **ZiBond** (a direct oxide to oxide bonding that involves wafer-to-wafer processing at low temperatures to initiate high bond strengths).
 - Between 2004 and 2005, based on their ZiBond technology, Ziptronic combined the dielectric bond with embedded metal to simultaneously bond wafers and form the interconnects at low temperature, so called **direct bond interconnect (DBI)**. Today, we called it **Cu-Cu Hybrid Bonding**.
 - The breakthrough (**chance**) for Ziptronic DBI technology came in the spring of **2015** when **Sony**, already using its “**Zibond**” oxide to oxide bonding technology, extended its license to include **DBI**.
 - The rest is history – **Sony shipped their Cu-Cu hybrid bonding product in 2015.**
-

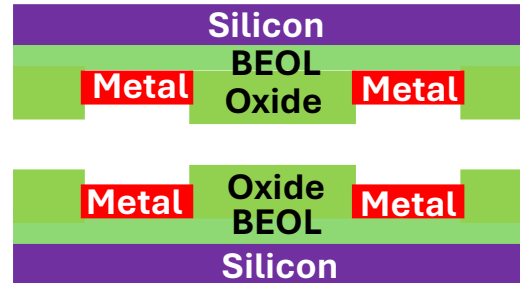
Patents:

- Q. Tong, et al., “Method for low temperature bonding and bonded structure,” U.S. Patent 6902987, Jun. 7, 2005, filed on Feb. 16, 2000.
- Q. Tong, et al., “Method for low temperature bonding and bonded structure,” U.S. Patent 7387944, Jun. 17, 2008, filed on Aug. 9, 2004.
- Q. Tong, et al., “Method for room temperature metal direct bonding,” US Patent 6962835, Nov. 8, 2005, filed on Feb. 7, 2003.
- Q. Tong, et al., “Room temperature metal direct bonding,” US Patent 7602070, Oct. 13, 2009, filed on Mar. 22, 2005.

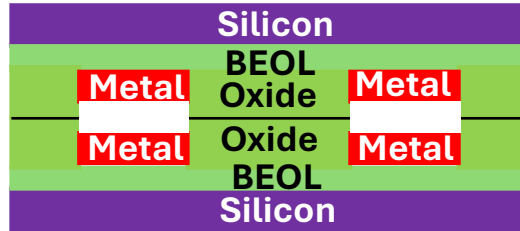
- **Cu-Cu Hybrid Bonding is an Old Technology.**
- **It has been in High-Volume Manufacturing (HVM) since 2016.**

Brief Fundamental (Key Process Steps) of Hybrid Bonding

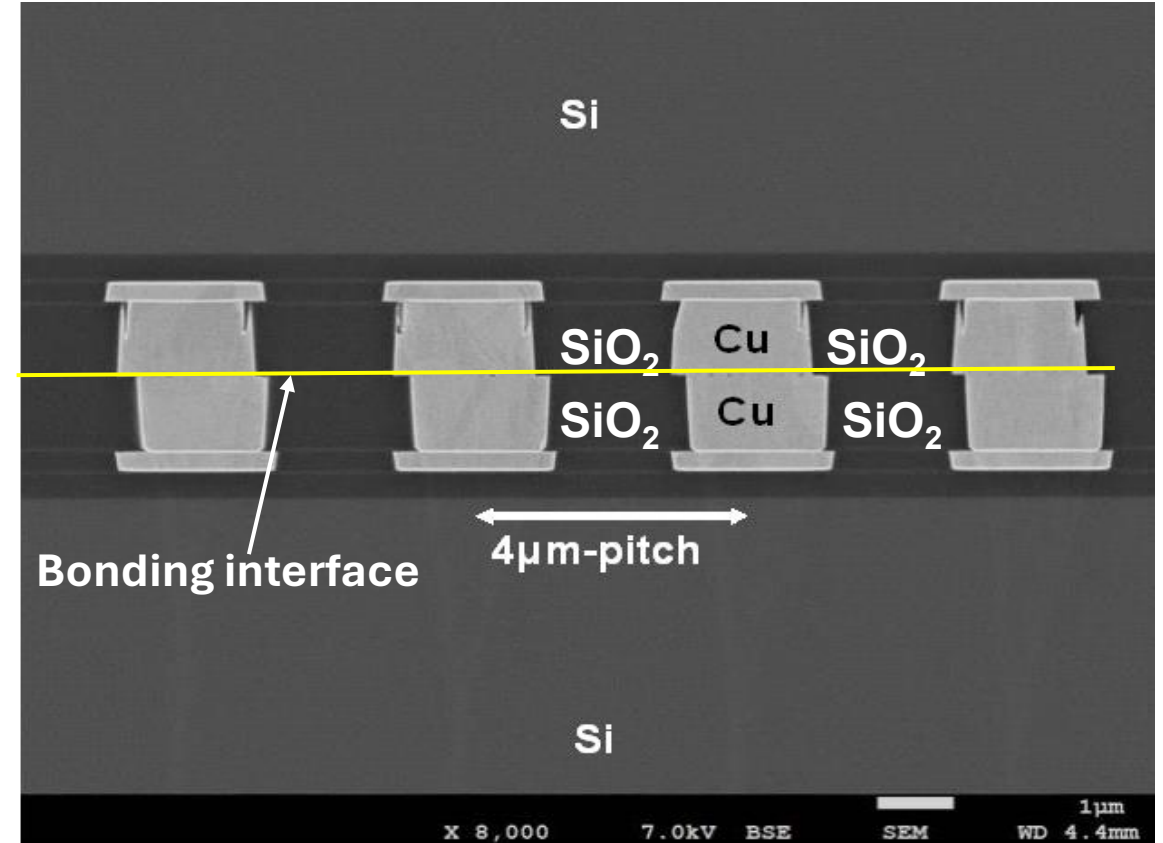
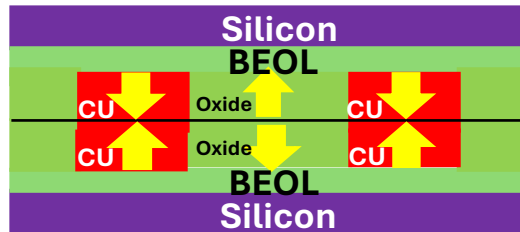
Metal (Cu) recess = 3nm
Plasma surface Activation



Oxide to Oxide Initial Bond
at Room Temperature
(ZiBond)



Metal to Metal Diffusion
Bond at Annealing (e.g.,
200°C for 1h)
(DBI)

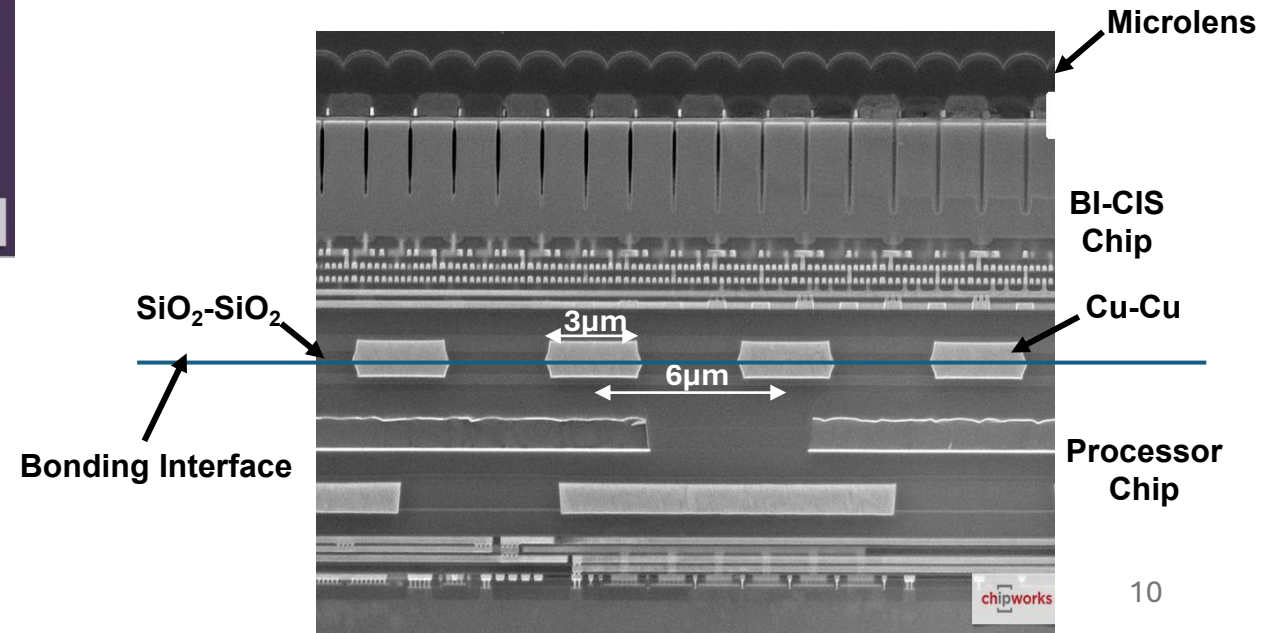
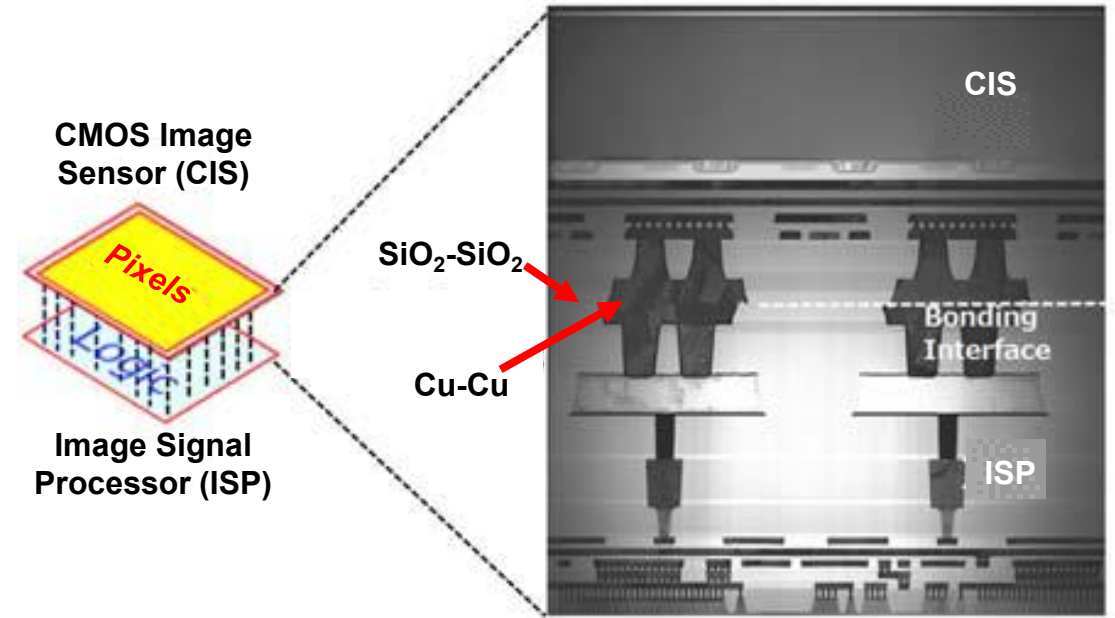
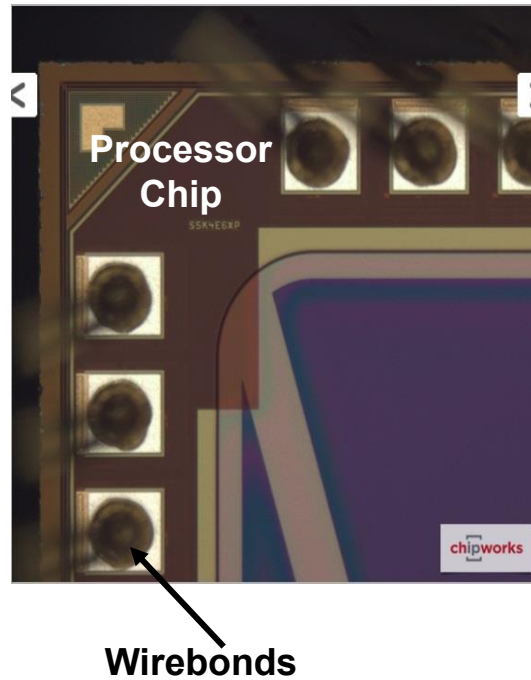
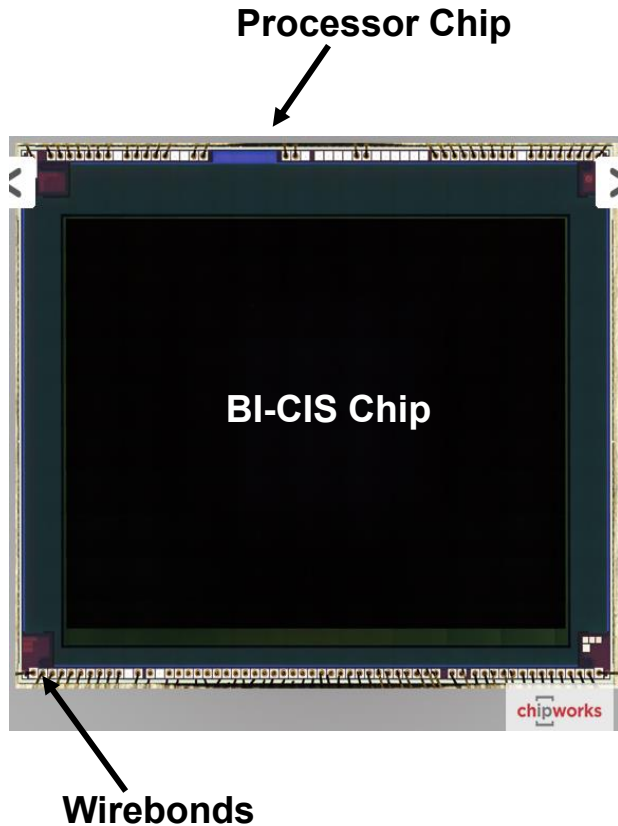


- Lau, J. H., “State of the Art and Outlooks of Cu–Cu Hybrid Bonding”, *IEEE Transactions on CPMT*, Vol. 15, No. 12, Dec. 2025, pp. 2575-2613.
- Lau, J. H., “Current Advances and Outlooks in Hybrid Bonding”, *IEEE Transactions on CPMT*, Vol. 15, No. 4, April 2025, pp. 651-681.
- Lau, J. H., “State of the art of Cu-Cu Hybrid Bonding”, *IEEE Transactions on CPMT*, Vol. 14, No. 3, March 2024, pp. 376-396.
- Lau, J. H., “Recent Advances and Trends in Cu-Cu Hybrid Bonding”, *IEEE Transactions on CPMT*, Vol. 13, No. 3, March 2023, pp. 399-425.
- Lau, J. H., “Recent Advances and Trends in Advanced Packaging”, *IEEE Transactions on CPMT*, Vol. 12, No. 2, February 2022, pp. 228-252.

HVM and to be in HVM Products with Hybrid Bonding

1. Sony's CIS with WoW
2. Sony's CIS with WoWoW
3. OMNIVISION's CIS
4. Samsung's CIS
5. AMD's 3D V-Cache
6. Graphcore's IPU
7. Jasminer's ASIC Miner
8. AMD's MI300A (3.5D IC Integration)
9. Samsung's SAINT (3.5D IC Integration)
10. Broadcom's XDSiP (3.5D IC Integration)
11. Apple's M5 Pro and M5 Max (GPU and CPU)
12. NVIDIA's Rubin
13. Intel's Clearwater Forest
14. Samsung's HBM
15. SK Hynix's HBM
16. Micron's HBM
17. YMTC's 3D NAND Flash
18. Kioxia-Western Digital's 3D NAND Flash
19. Samsung's 10th-Gen (V10) NAND
20. SK Hynix's 10th-Gen (V10) NAND
21. Apple's iPhones sell in China (YMTC's 3D NAND Flash)

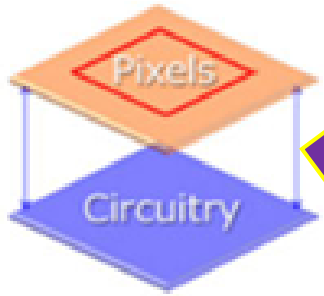
Sony's CMOS Image Sensor (CIS) with Hybrid Bonding (WoW)



Shipped in 2016

Sony's WoWoW Cu-Cu Hybrid Bonding

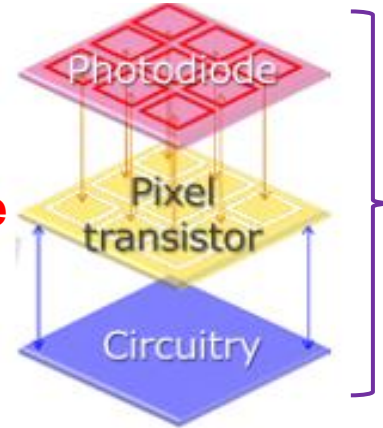
Stacked CIS



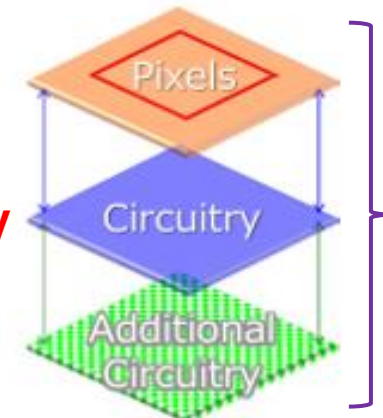
2015

3-wafer Stacked CIS

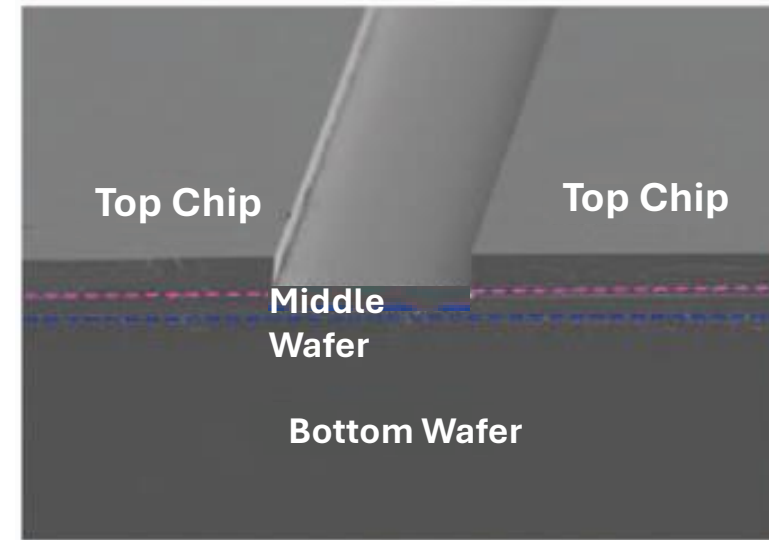
High
Performance



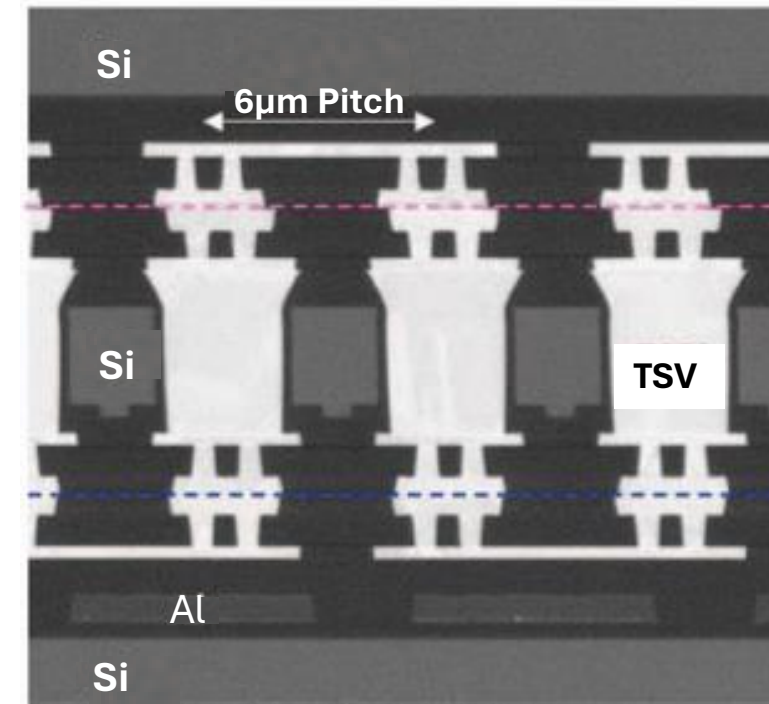
Multi-
Functionality



To be shipped in 2026

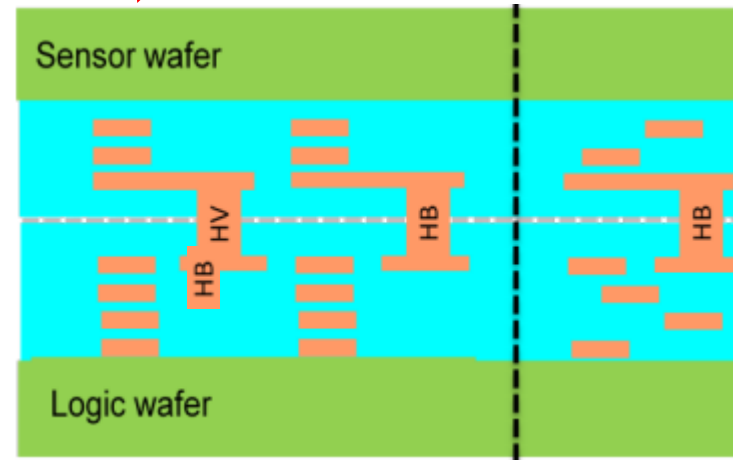
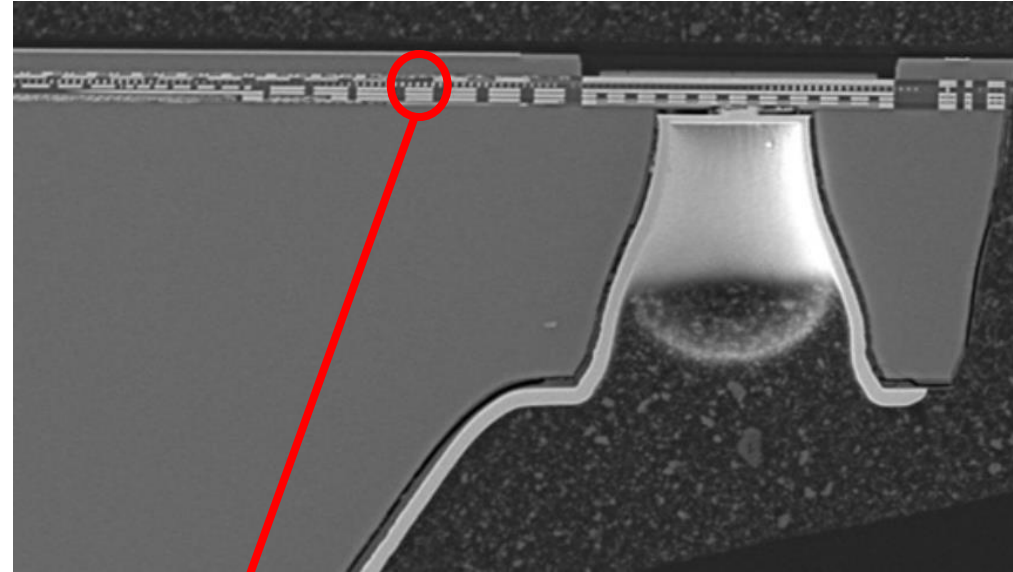
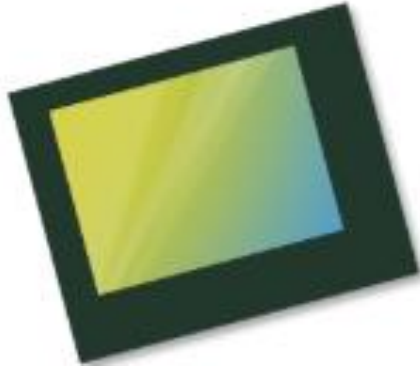


F2B
F2F
WoW



Top Chip
F2B
CoW
Middle Wafer
F2F
WoW
Bottom Wafer

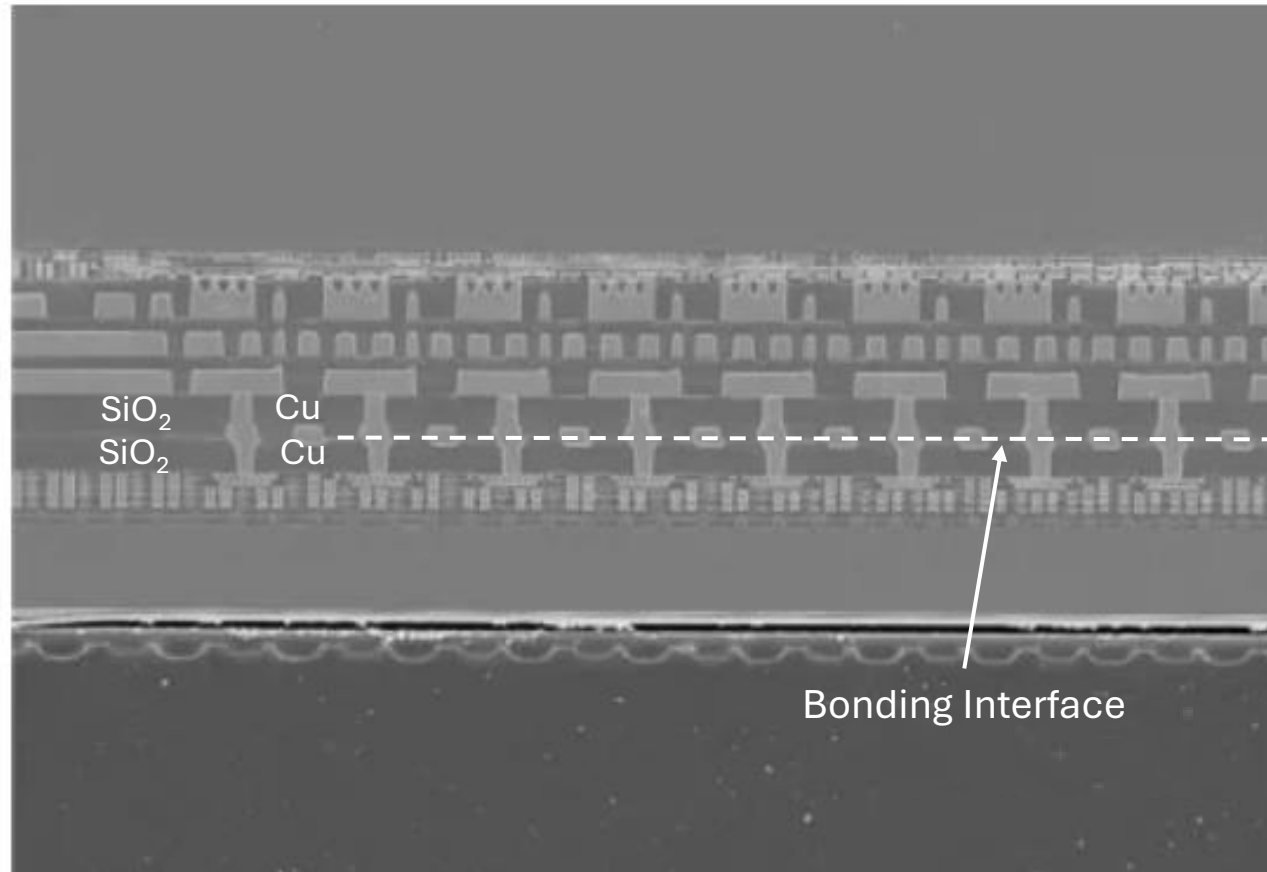
OMNIVISION OX05B1S Sensor



Unlike traditional sensors that use Through-Silicon Vias (TSVs) at the periphery, **OMNIVISION OX05B1S** uses direct copper-to-copper (**Cu-Cu**) connections. This "bumpless" bonding allows for a higher interconnect density and significantly smaller pixel sizes

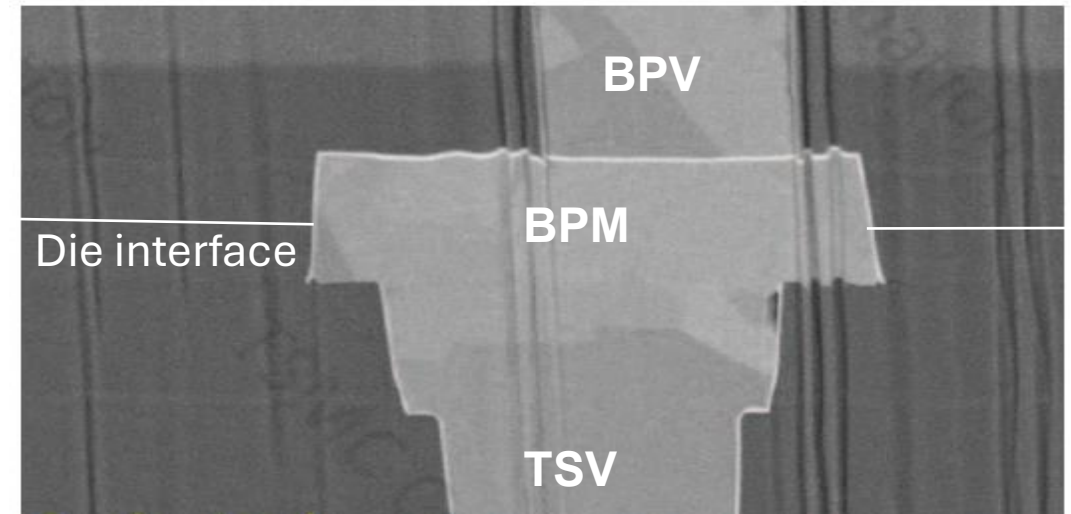
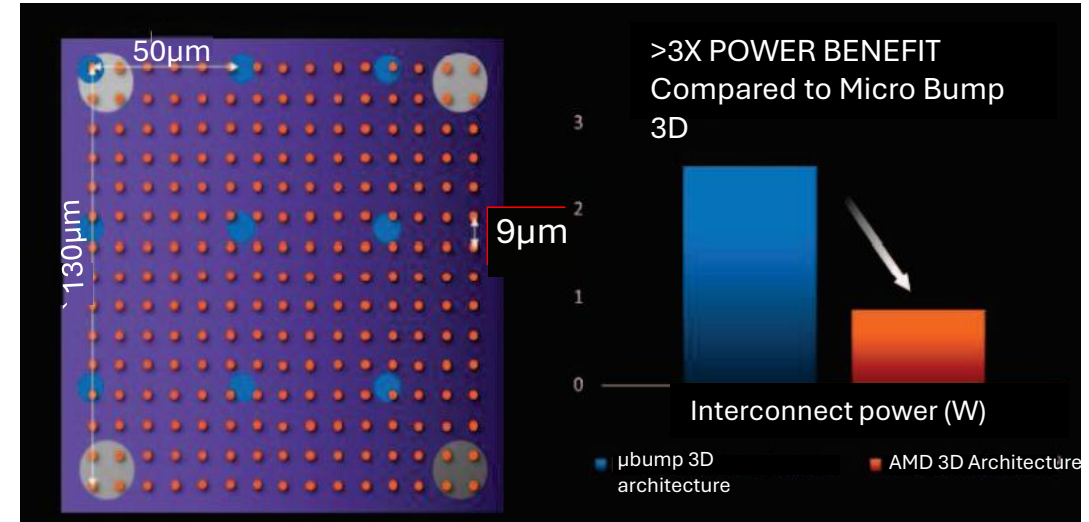
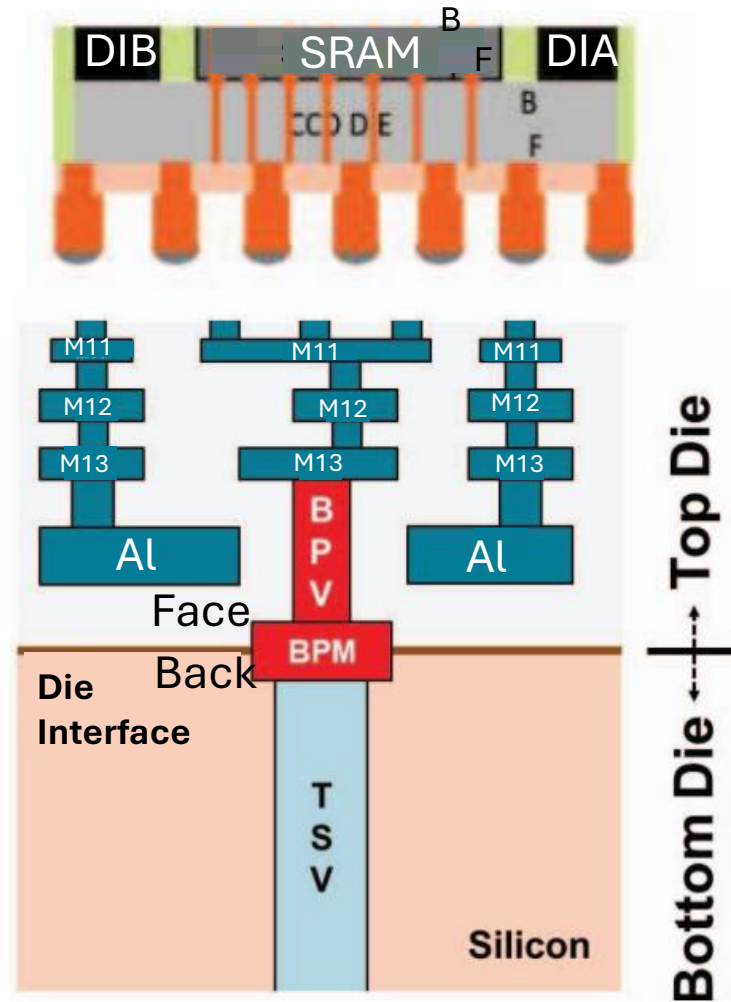
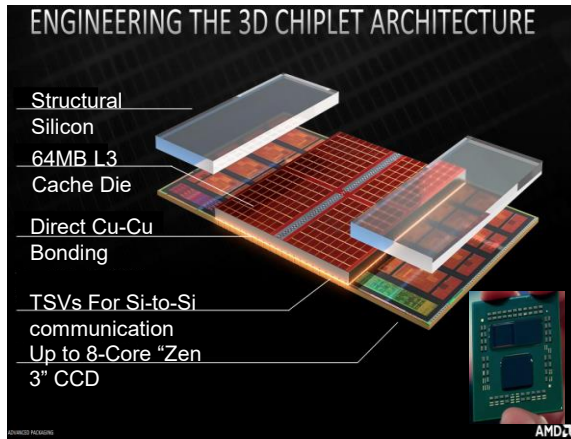
Shipped in 2023

Samsung GM5 imager (for Google Pixel 7 Pro)



June 2025

AMD's 3D V-cache with Hybrid Bonding: SRAM (Face)-to-CCD (Back) (CoW)

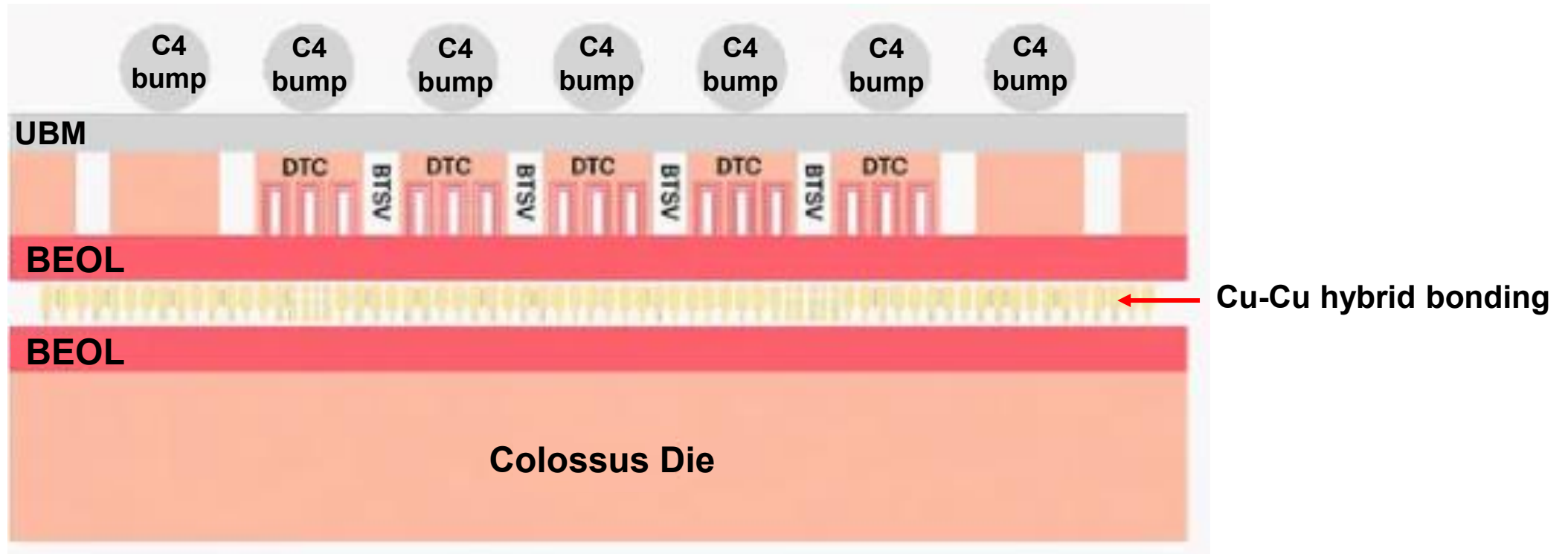


Agarwal, R., P. Cheng, P. Shah, B. Wilkerson, R. Swaminathan, J. Wu, and C. Mandalapu, "3D Packaging for Heterogeneous Integration", *IEEE/ECTC Proceedings*, May 2022, pp. 1103-1107.

BPM (bond pad metal)
BPV (bond pad via)
TSV (through-silicon via)

Shipped in April 2022

Graphcore's IPU (Intelligence Processing Unit) Processor

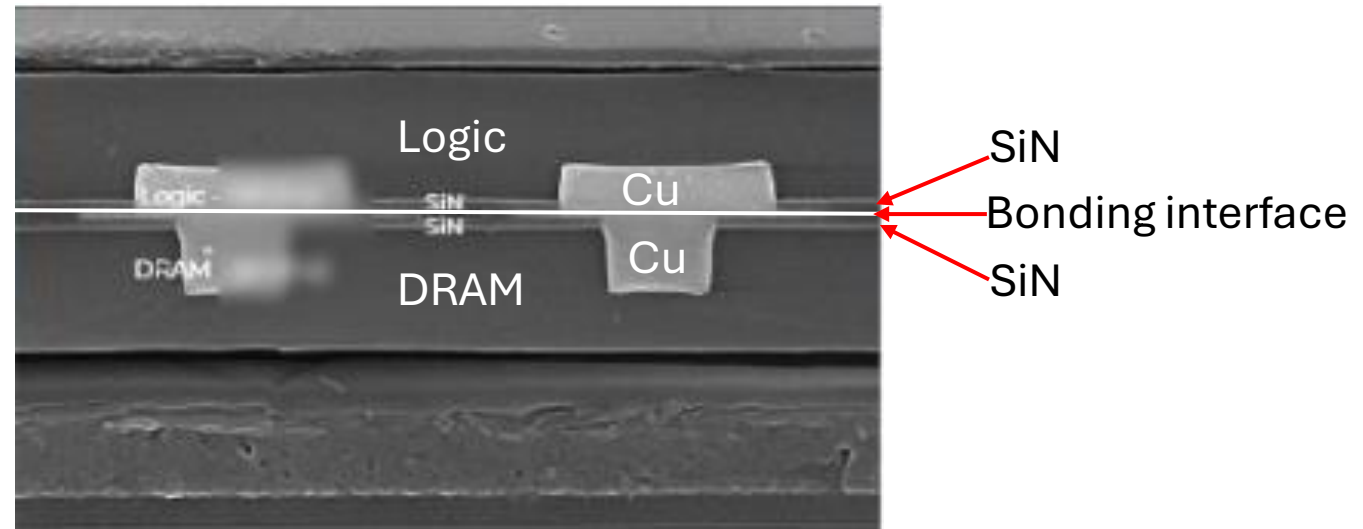


Moore, S., "Graphcore uses TSMC 3D Chip Tech to Speed AI by 40%", *IEEE Spectrum*, March 3, 2022.

Shipped in February 2022

Jasminer's ASIC miner designed for high-efficiency, quiet, and small-scale mining of Ethereum Classic (ETC) and other Ethash-based algorithms (Cu-Cu Hybrid Bonding)

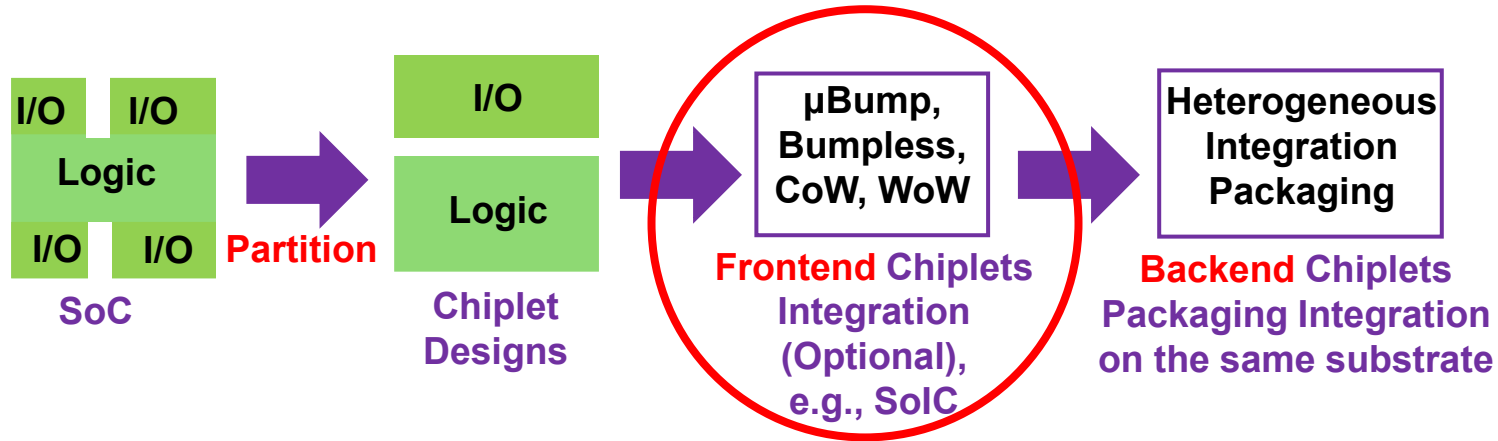
JASMINER X4-QZ 5GB



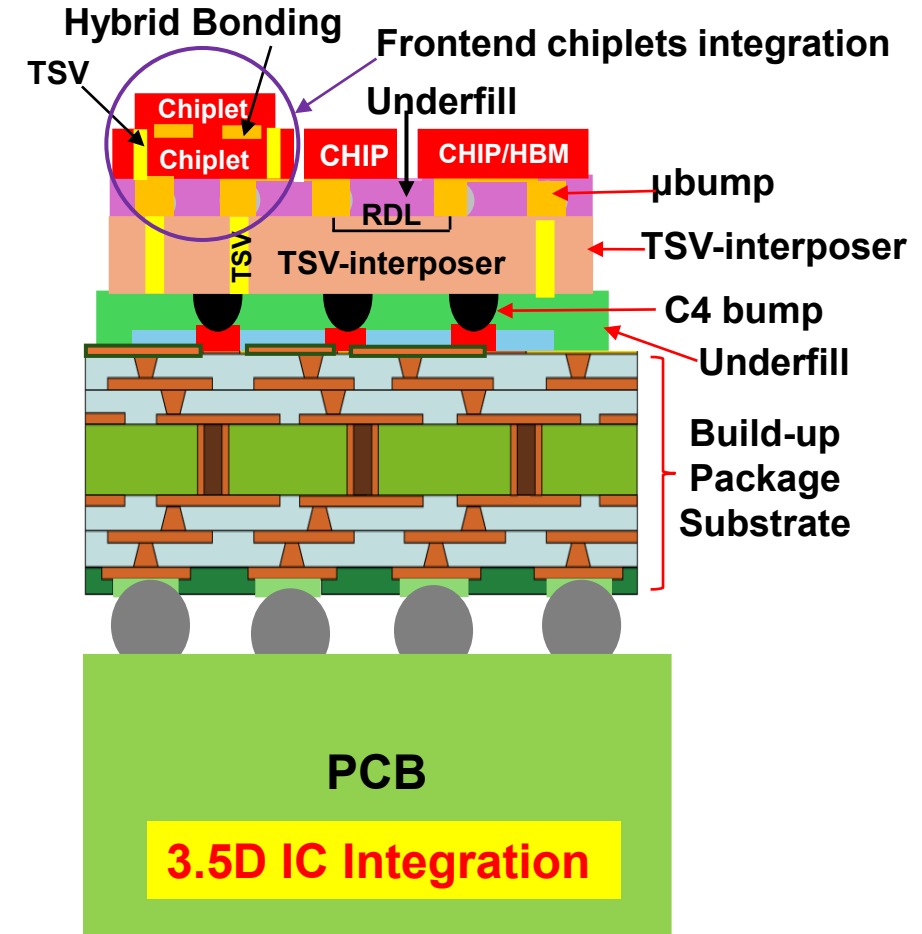
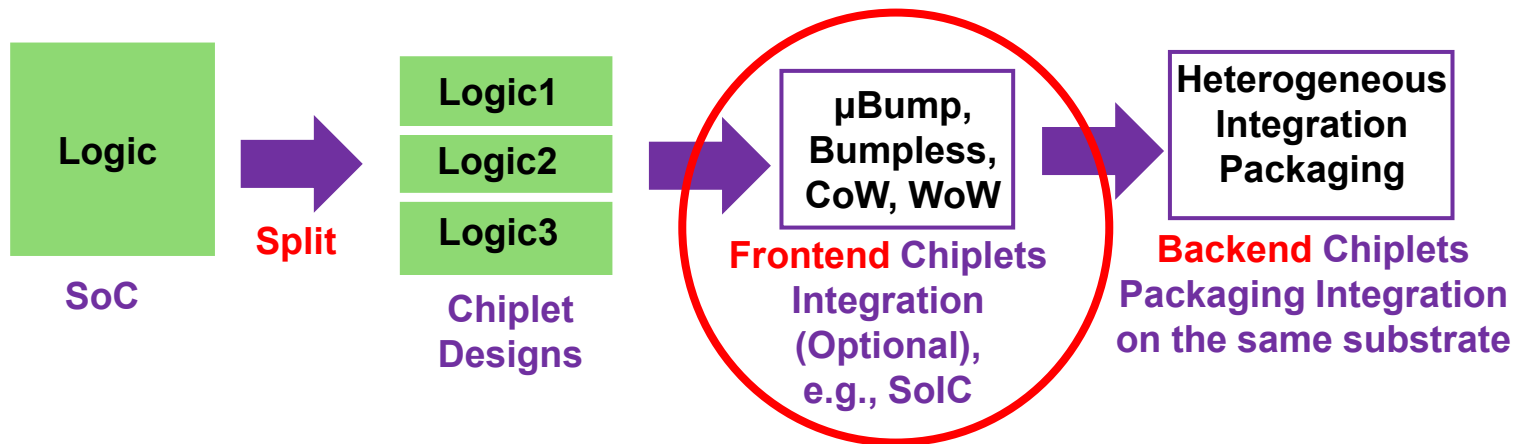
- The base model (Jasminer X4-Q (Standard)) was released in **June 2022** featuring a hash rate of 1040 MH/s at 480W.
- A follow-up variant (Jasminer X4-Q-Z) with a hash rate of 840 MH/s and lower power consumption (380W) was launched in **December 2022**.
- Another iteration (Jasminer X4-QZ) was released in **March 2023** to further optimize efficiency for home mining environments.

Unimicron's 3.5D IC Heterogeneous Integration

Chip partition and integration (Driven by cost and technology optimization)

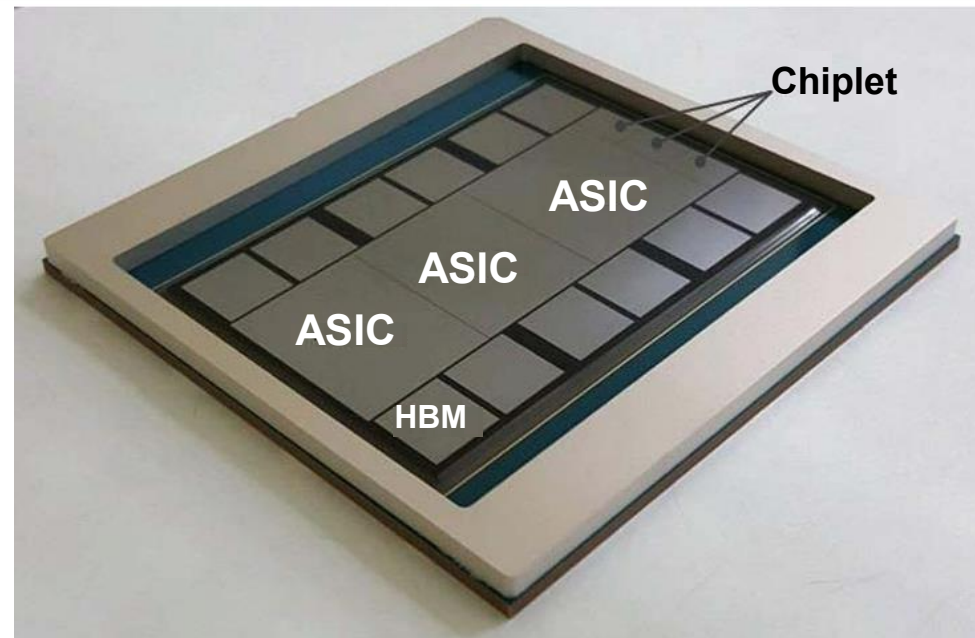
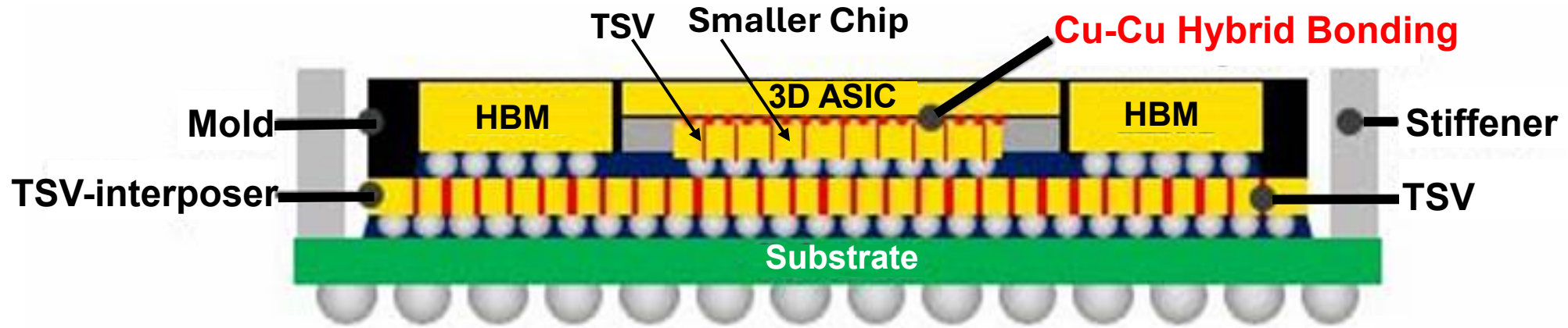


Chip split and integration (Driven by cost and yield)



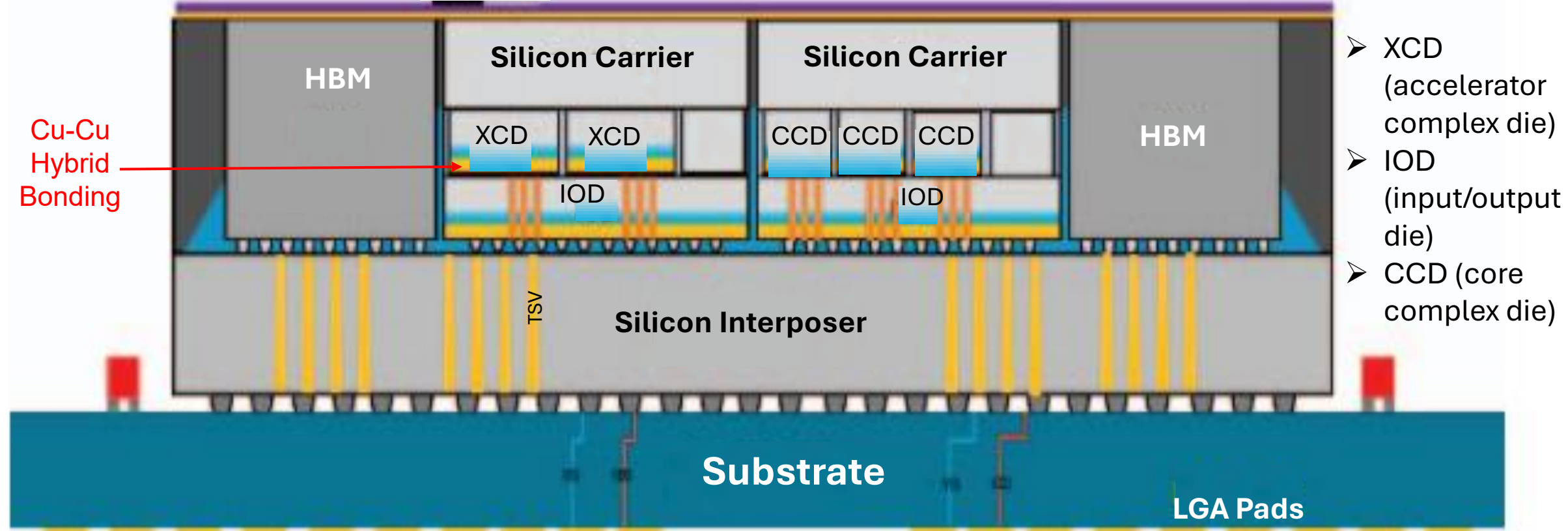
- Smaller Package Size
- Better Electrical Performance

Samsung's 3.5D IC Heterogeneous Integration

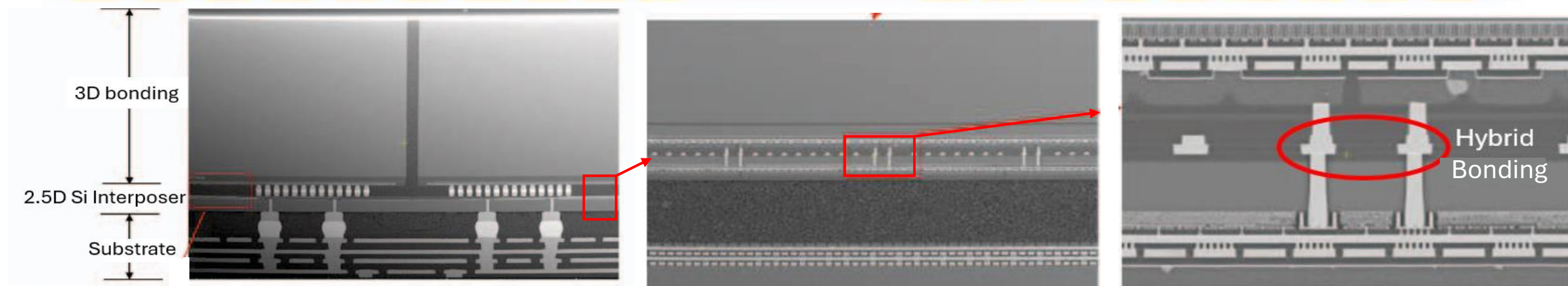


I. Lee, et al., "Extremely Large 3.5D Heterogeneous Integration for the Next-Generation Packaging Technology", *IEEE/ECTC Proceedings*, June 2023, pp. 893-898.

AMD's MI300A 3.5D IC Heterogeneous Integration with Hybrid Bonding

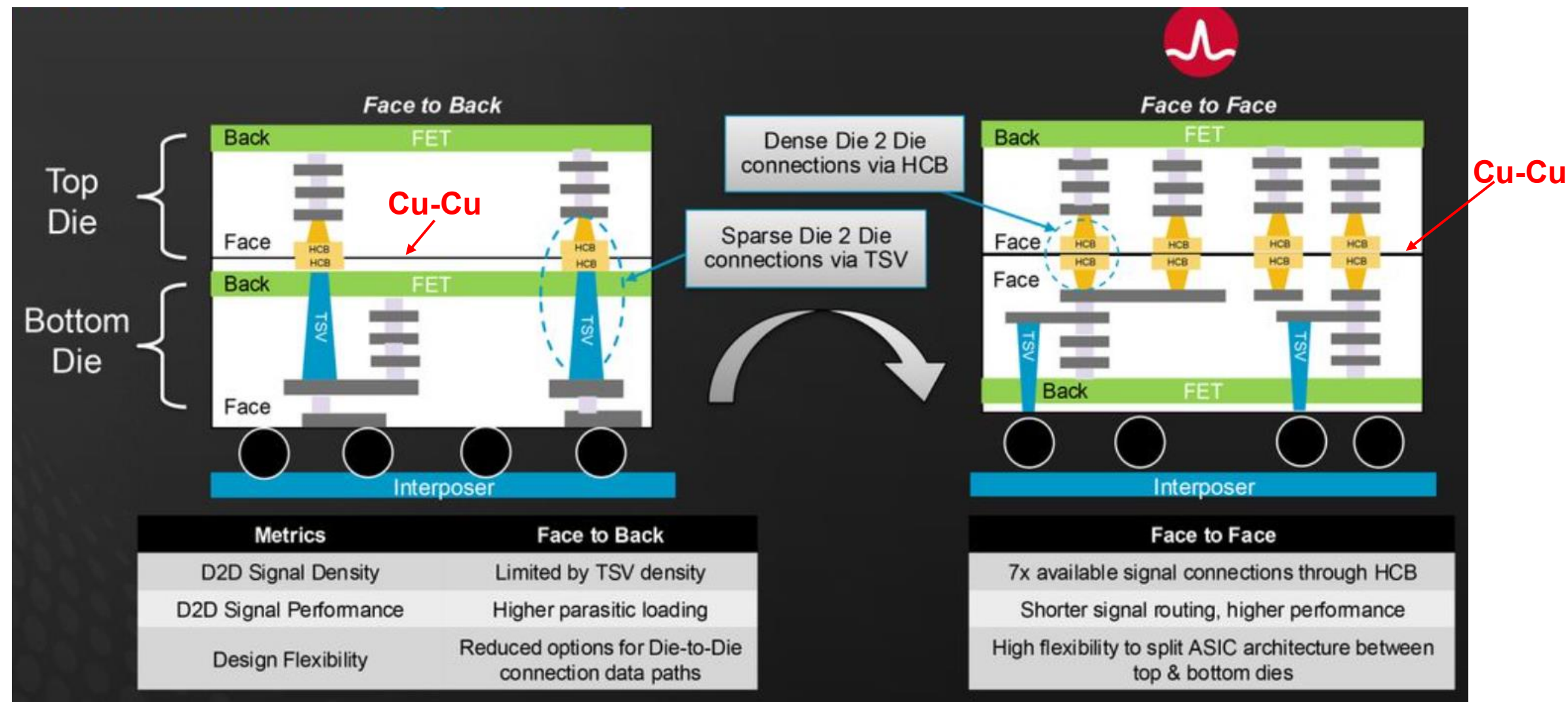


- XCD (accelerator complex die)
- IOD (input/output die)
- CCD (core complex die)



Broadcom's 3.5D IC Heterogeneous Integration with Hybrid Bonding

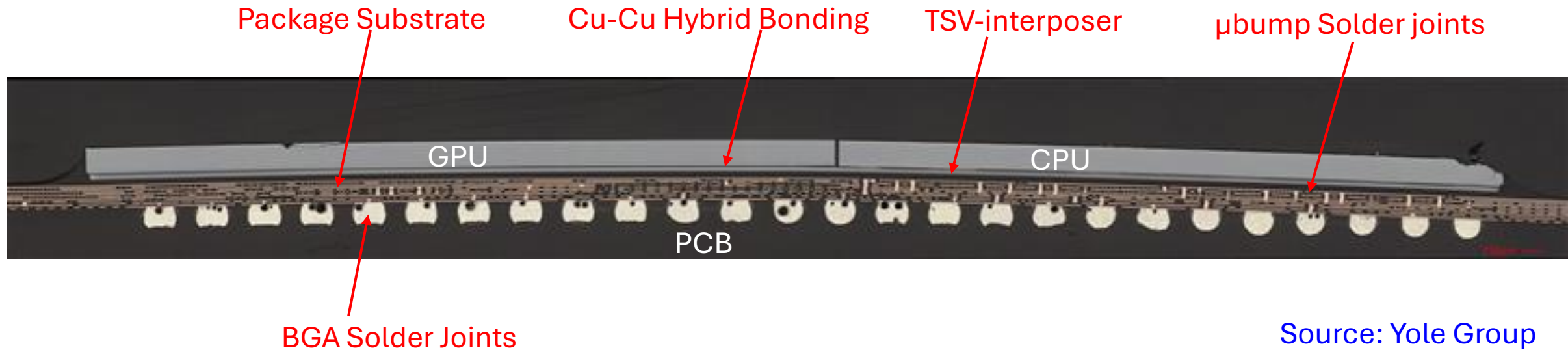
3.5D eXtreme Dimension System in Package (XDSiP)



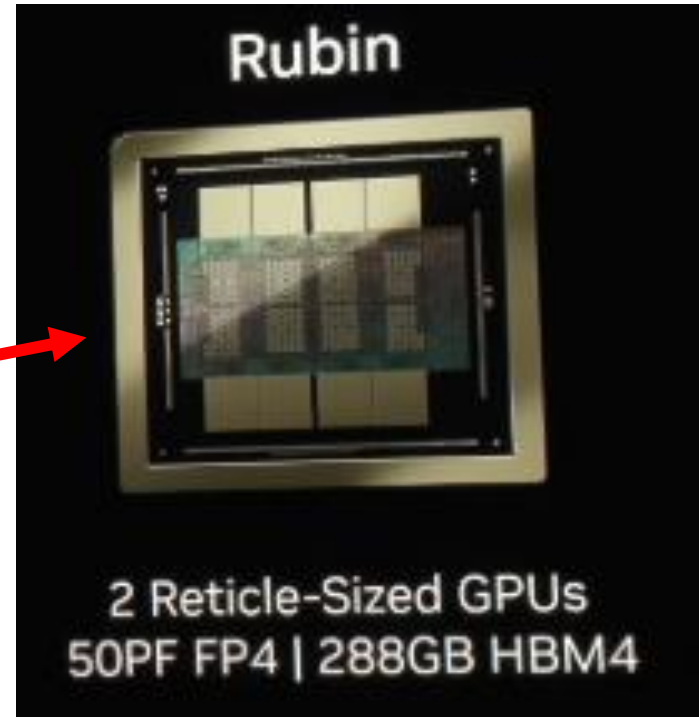
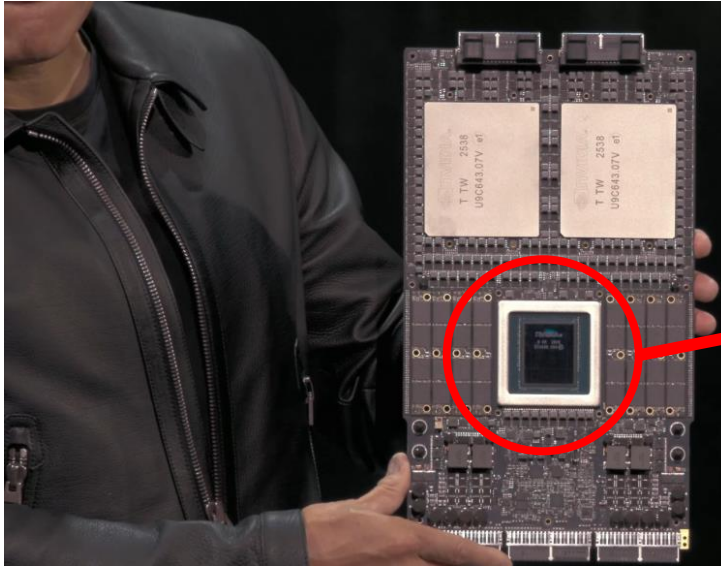
Shipped to Fujitsu in February 2026

Apple's M5 Pro Packaging

The CPU and GPU are Cu-Cu Hybrid Bonding to a TSV-Interposer

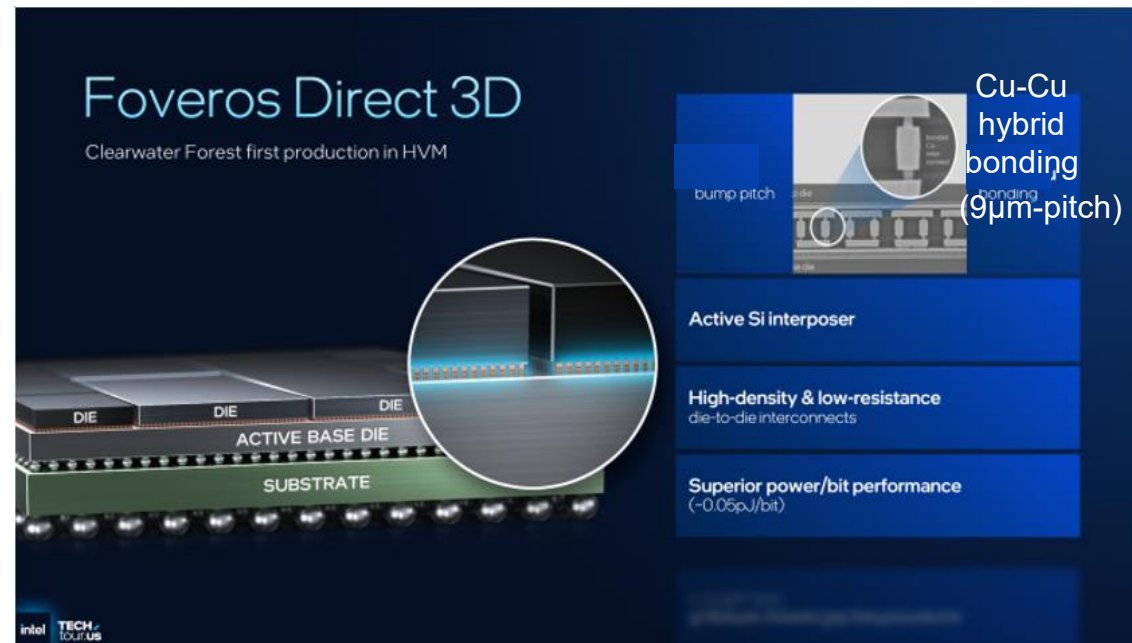


NVIDIA's Rubin

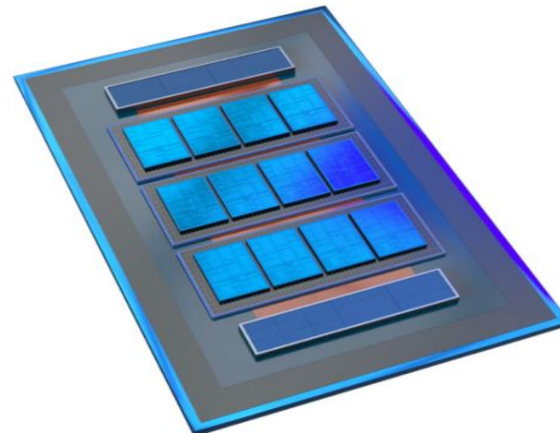


NVIDIA is scheduled to begin shipping the **Rubin** architecture, which utilizes **hybrid bonding** technology, in the **second half of 2026**.

Intel's Hybrid Bonding (Foveros Direct 3D)



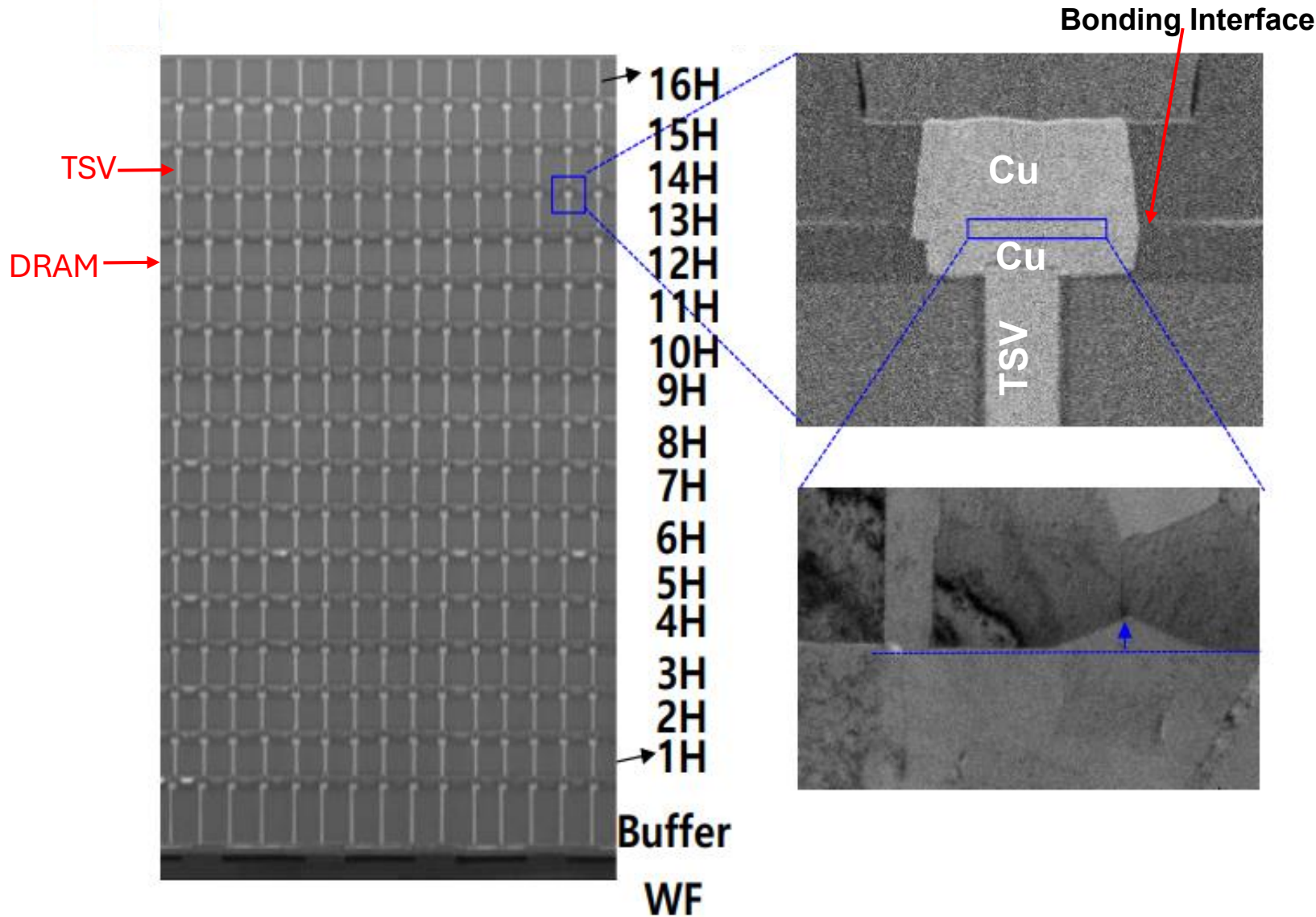
Intel's Clearwater Forest with Hybrid Bonding



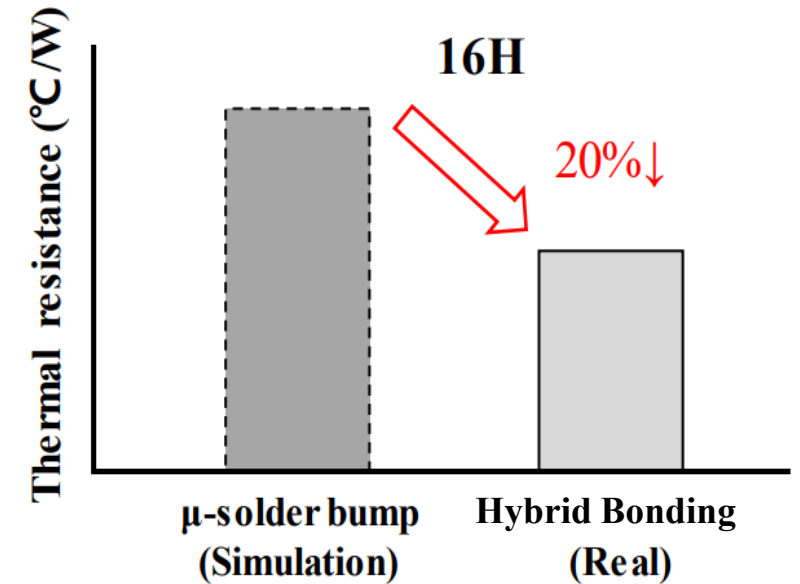
Intel's Clearwater Forest uses Intel's Foveros Direct 3D (hybrid bonding) at 9um-pitch technology. Volume production is scheduled for the first half of 2026.

Samsung's HBM with Hybrid Bonding

HBM Stack with Hybrid Bonding

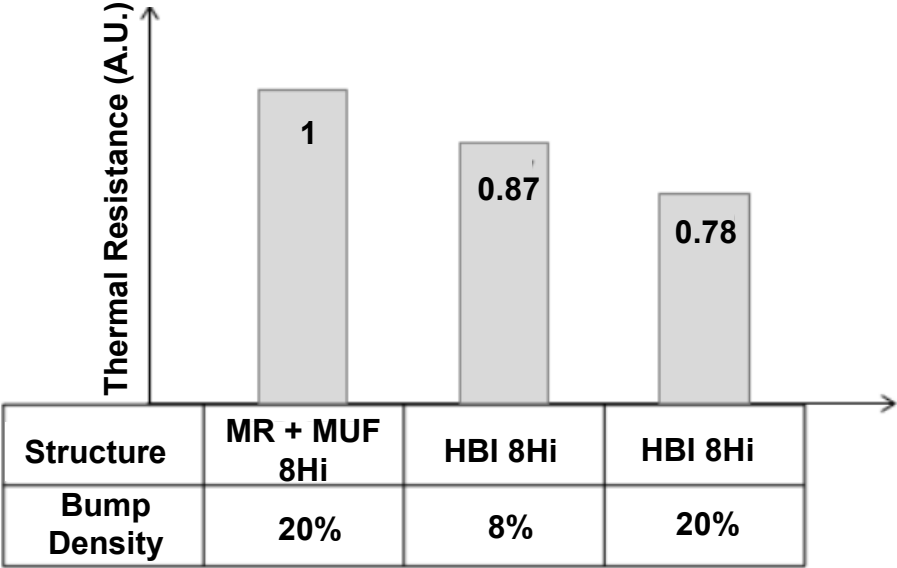
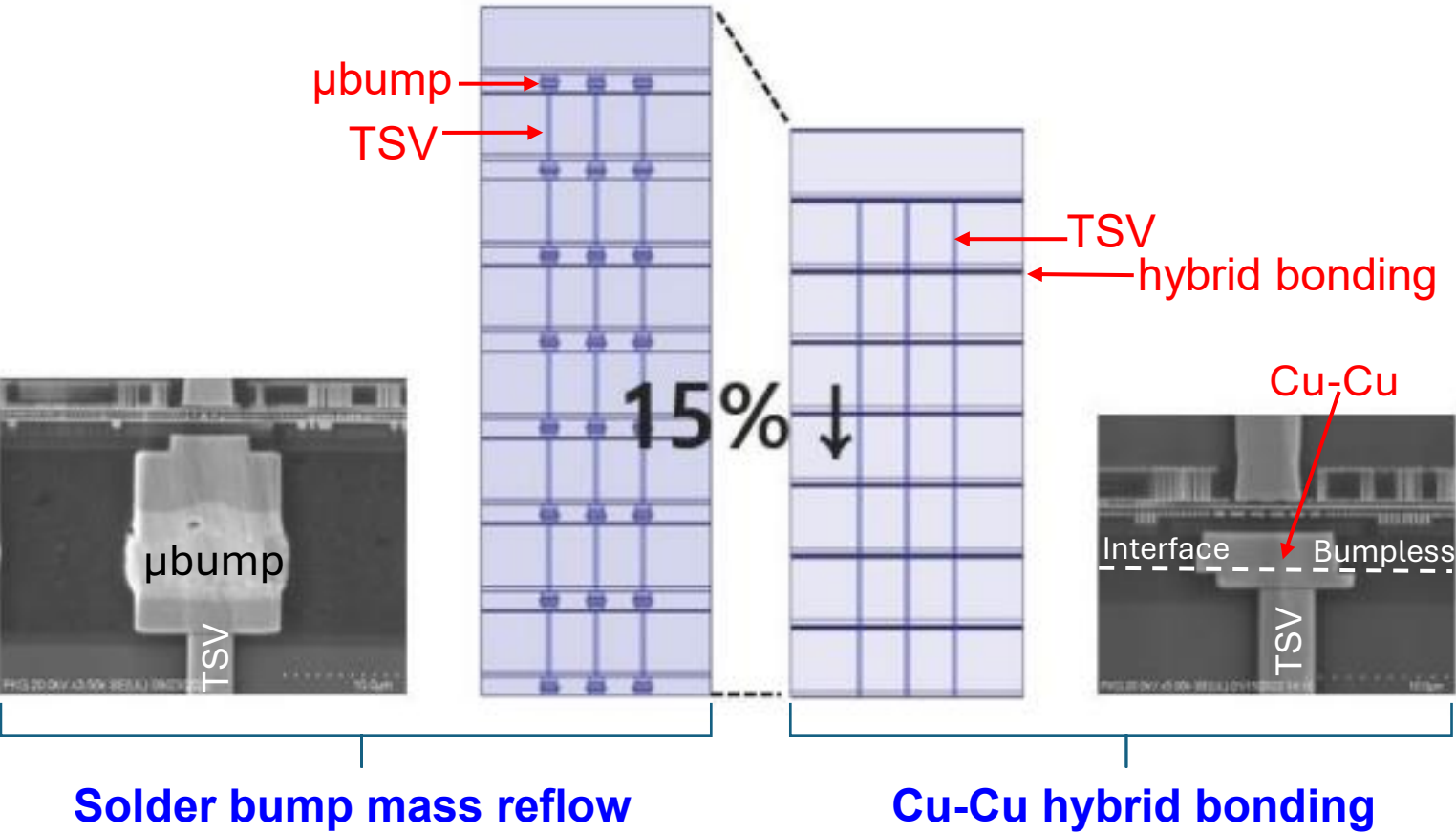


Thermal Resistance of HBM Stack with Hybrid Bonding



Shipped in 2026

SK Hynix's HBM with Hybrid Bonding

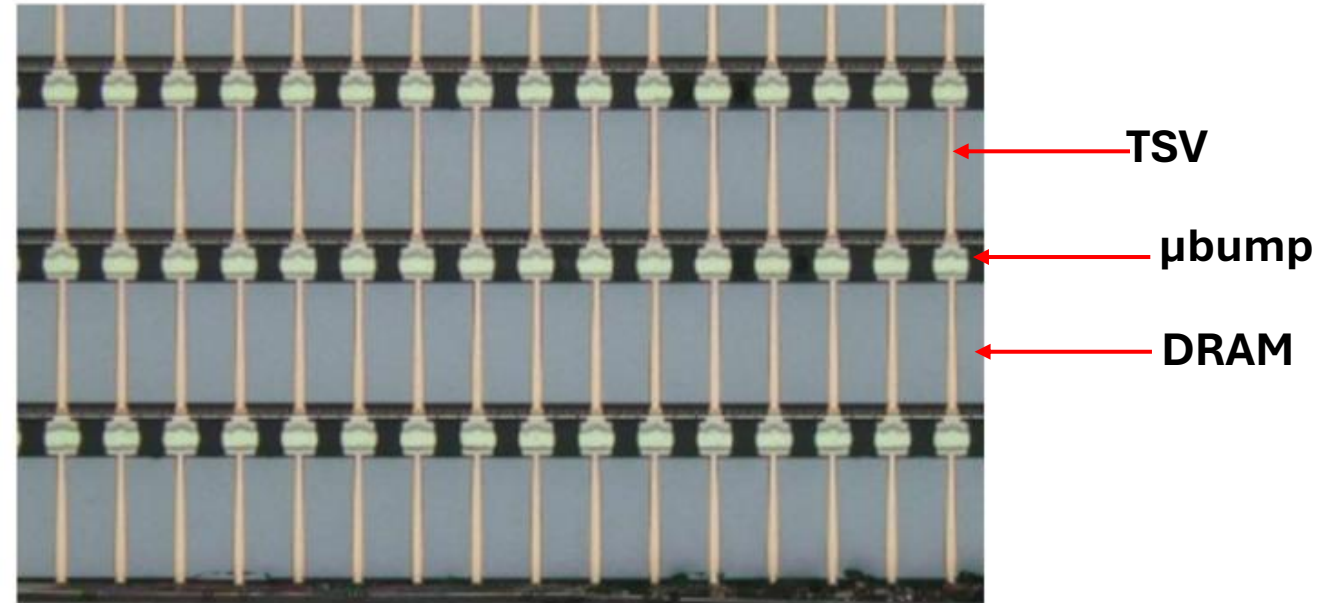


Thermal Performance

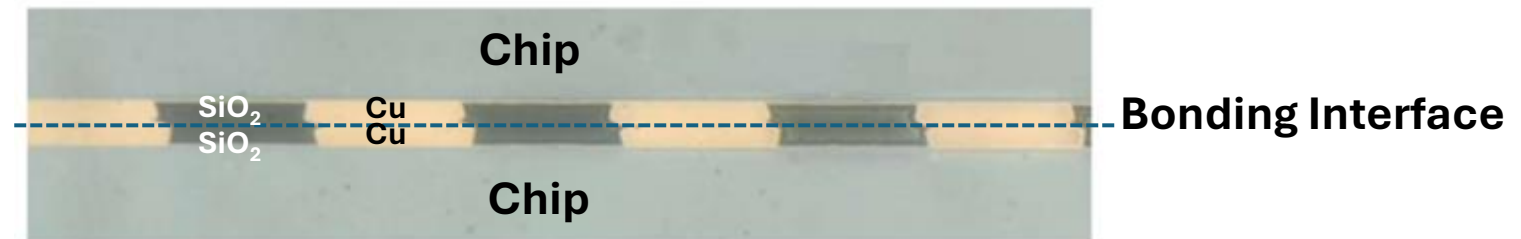
To be shipped in 2026

Micron's HBM with Hybrid Bonding

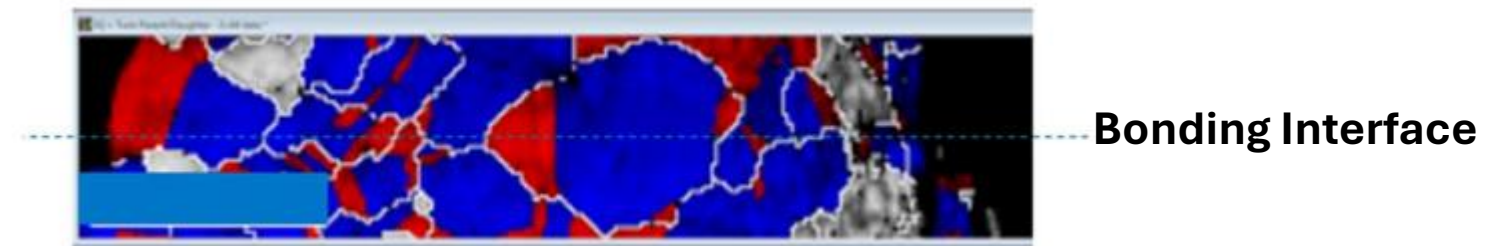
(a)



(b)



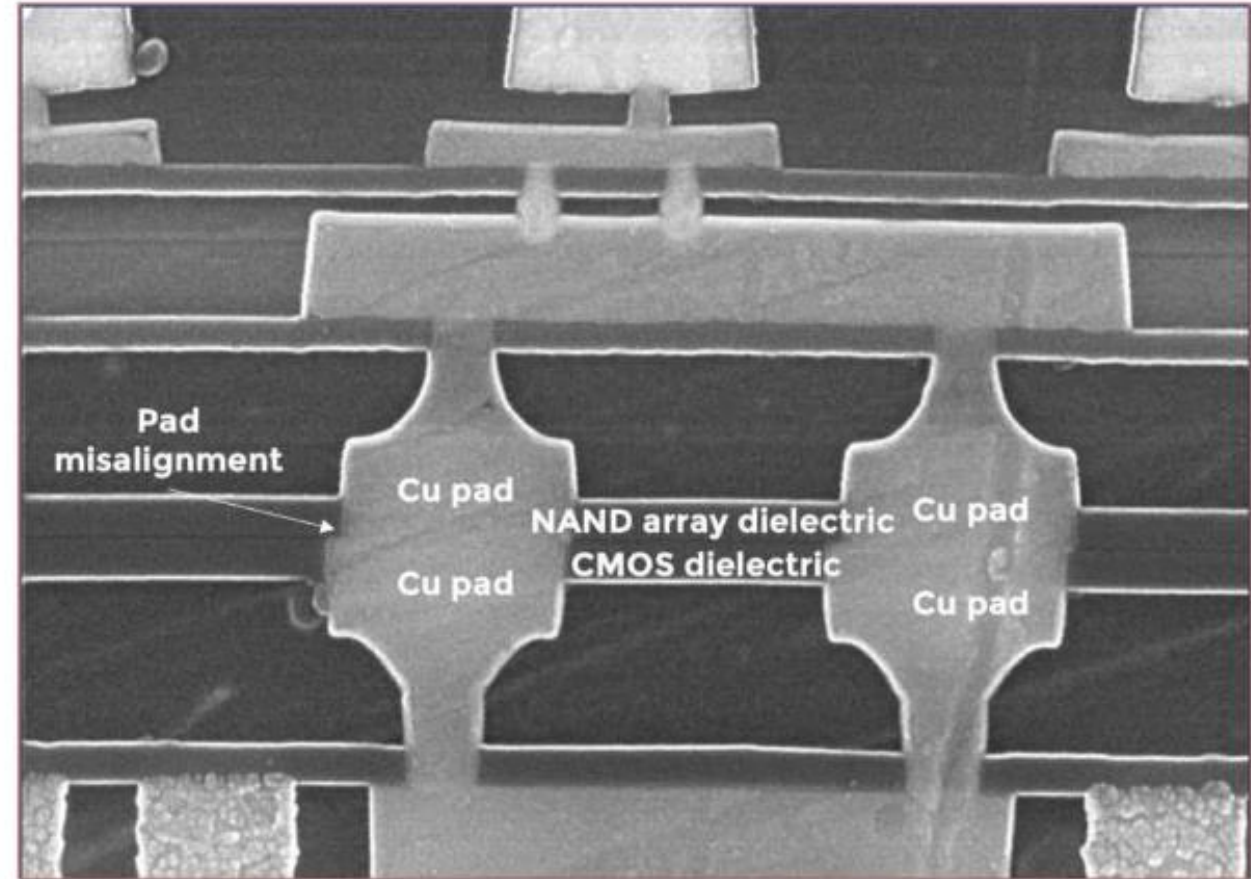
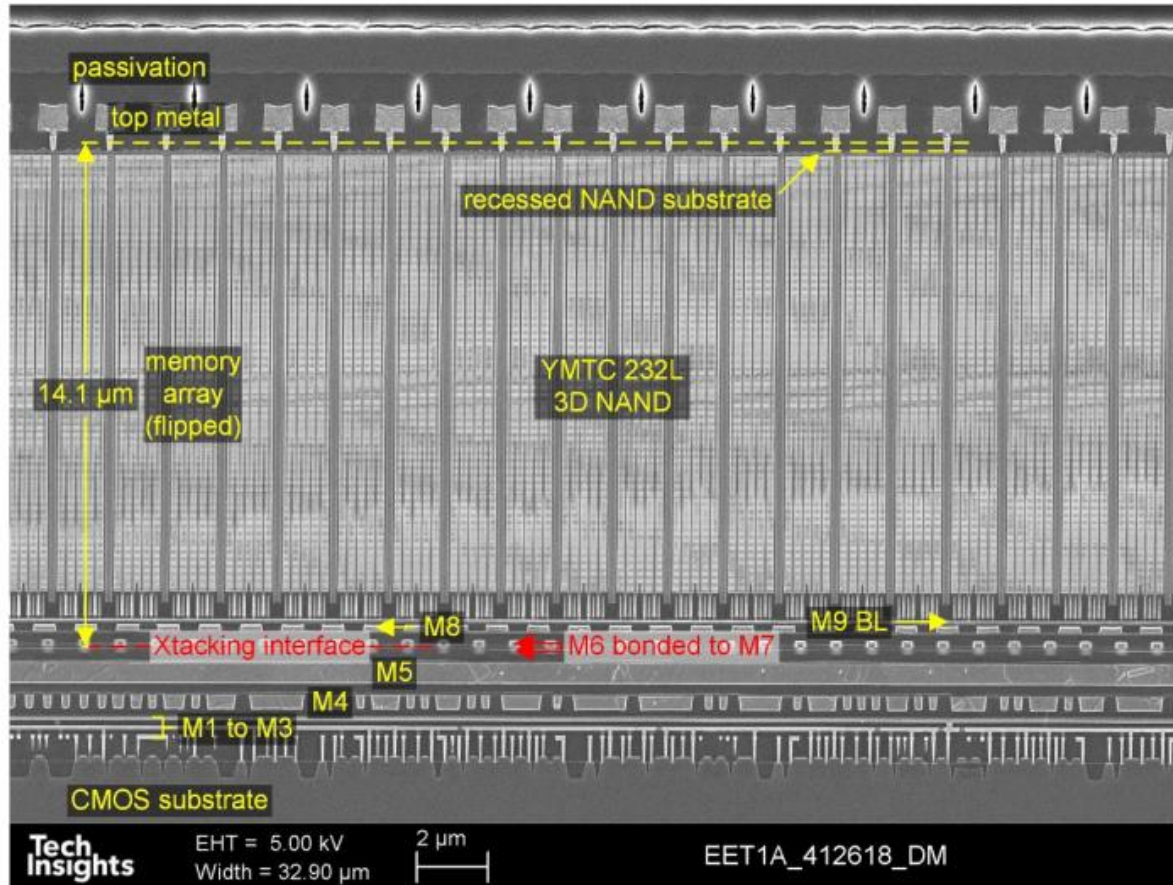
(c)



To be shipped in 2027

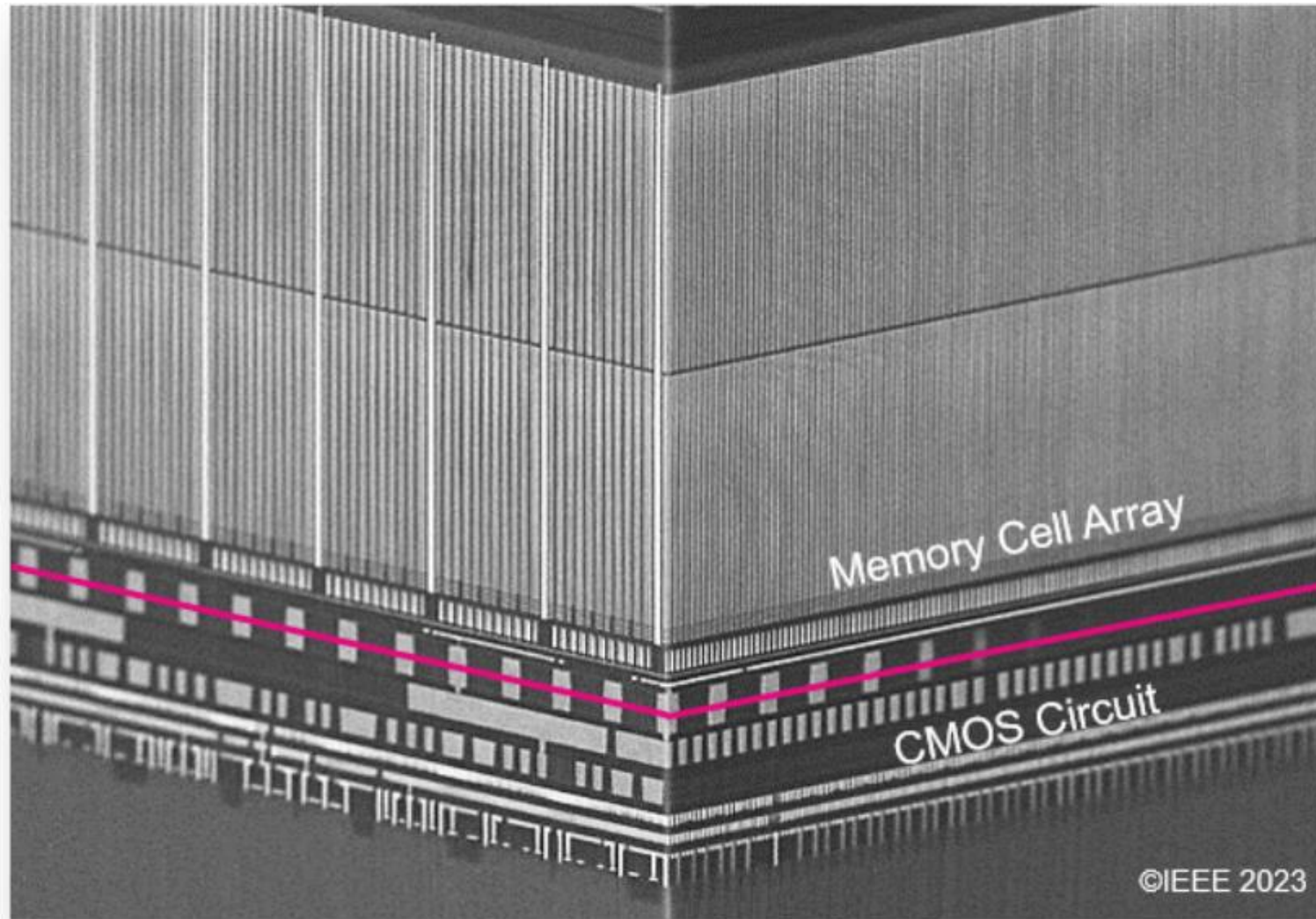
YMTC's 232 Layers 3D NAND Flash Memory by Hybrid Bonding (2023)

Proprietary Xtacking Technology



- 3D NAND flash memory is a 3D monolithic manufacturing method within the chip.
- Apple is considering sourcing memory chips for its iPhone 14 from Yangtze Memory Technologies Company (YMTC). The report, which was obtained by industry news outlet *Light Reading*, states that “YMTC could start supplying memory for new iPhone models in 2022.”

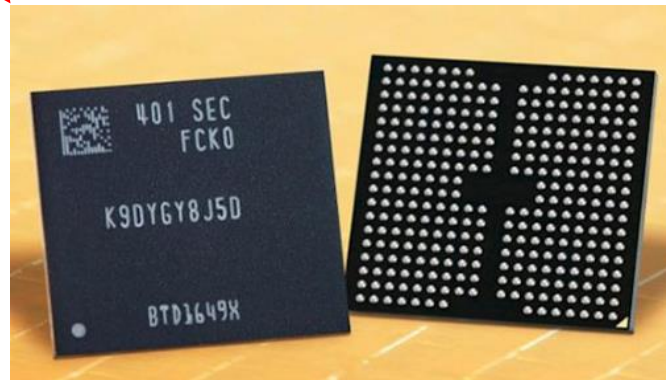
Kioxia-Western Digital's BiCS8 (218-layer) 3D NAND – CMOS directly Bonded to Array (CBA) (2023)



In-side a chip (monolithic)

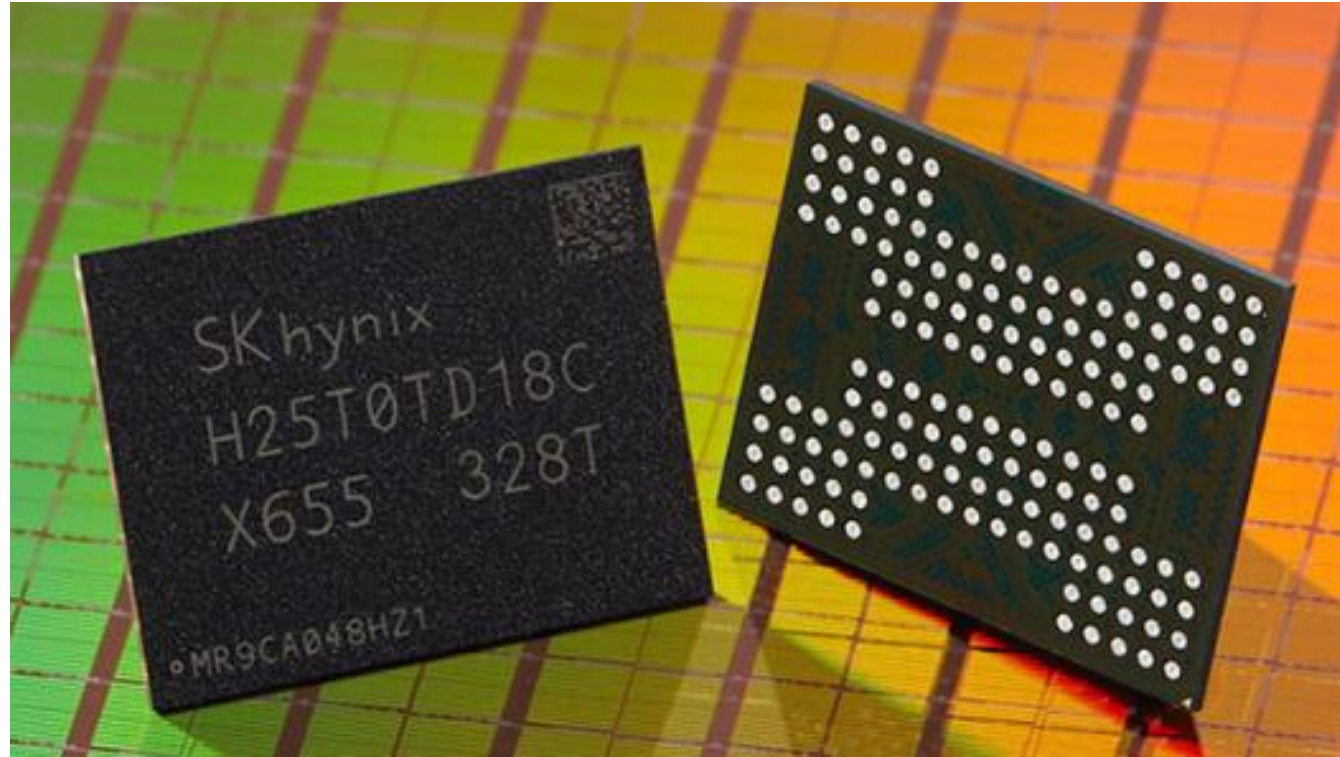
Samsung's 10th-Gen (V10) NAND

Signed a licensing agreement with YMTC (Xtacking) in early 2025



Samsung is currently scheduled to begin full-scale mass production of its 400+ layers 10th-generation (V10) V-NAND in **October 2026**.

SK Hynix's 10th-Gen (V10) NAND



For 400+ layers counts, SK hynix aims to complete development of the V10 pilot line in **2026**, with full-scale mass production targeted for **early 2027**.

Cu-Cu Hybrid Bonding in iPhones Sold in China (September 2026)



- As of **early 2026**, reports indicate that **Apple** is planning to introduce **YMTC 3D NAND Xtacking** flash chips specifically for iPhone models sold within the **Chinese market**.
- Apple's market share in China was reported at approximately **29.48%** as of **March 2026**.

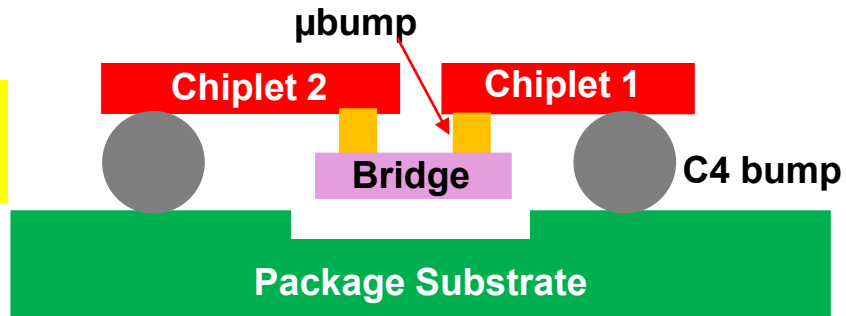
Some Applications of Hybrid Bonding

CONTENTS

- **New Applications of Hybrid Bonding to Chiplets Heterogeneous Integration**
 - **Bridges**
 - **Build-up Package Substrate**
 - **Package-on-Package**
 - **Package of Choice for HPC and Data Centers in AI Era**
 - 2.5D IC Integration
 - 3.3D IC Integration
 - **Co-Packaged Optics with Silicon Photonics**
 - 3D CPO on Fan-Out RDLs
 - 3D CPO on Organic Interposer
 - CPO on TSV Interposer (3.5D)
 - 3D CPO on TGV Interposer
 - 3D CPO on TGV Substrate
 - 3D CPO with Si Photonics
 - **Thermal Management**
 - Microchannels in TSV-interposer
 - Microchannels between chip and TSV-interposer
 - **Future HPC and Data Center Driven by AI**
- **Summary and Recommendations**

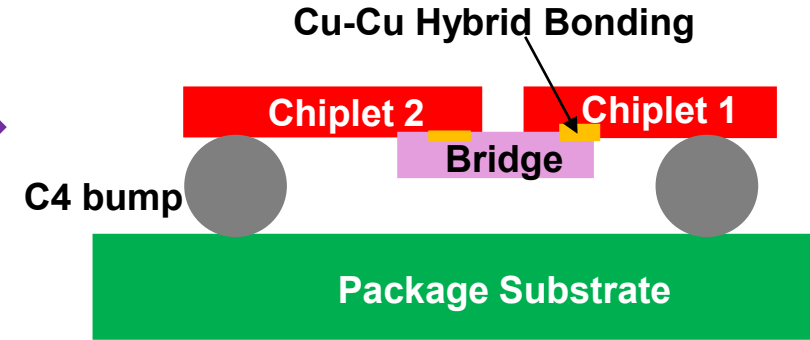
Hybrid Bonding Bridge (2D IC Integration)

Today



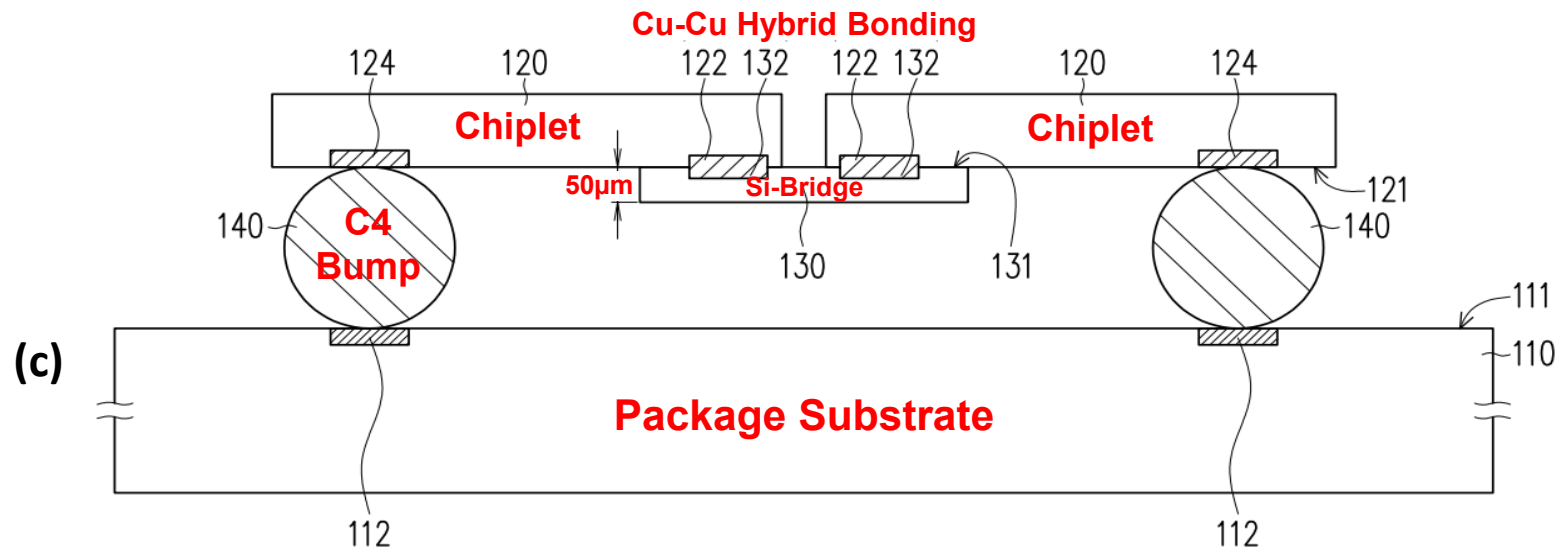
(a)

New

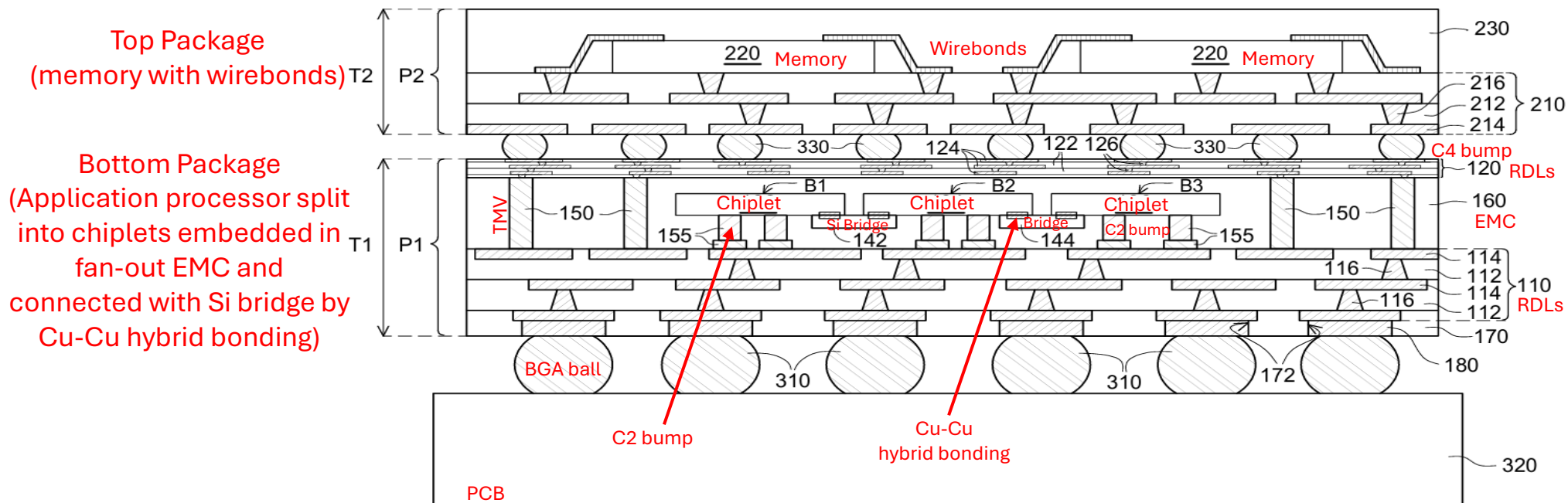
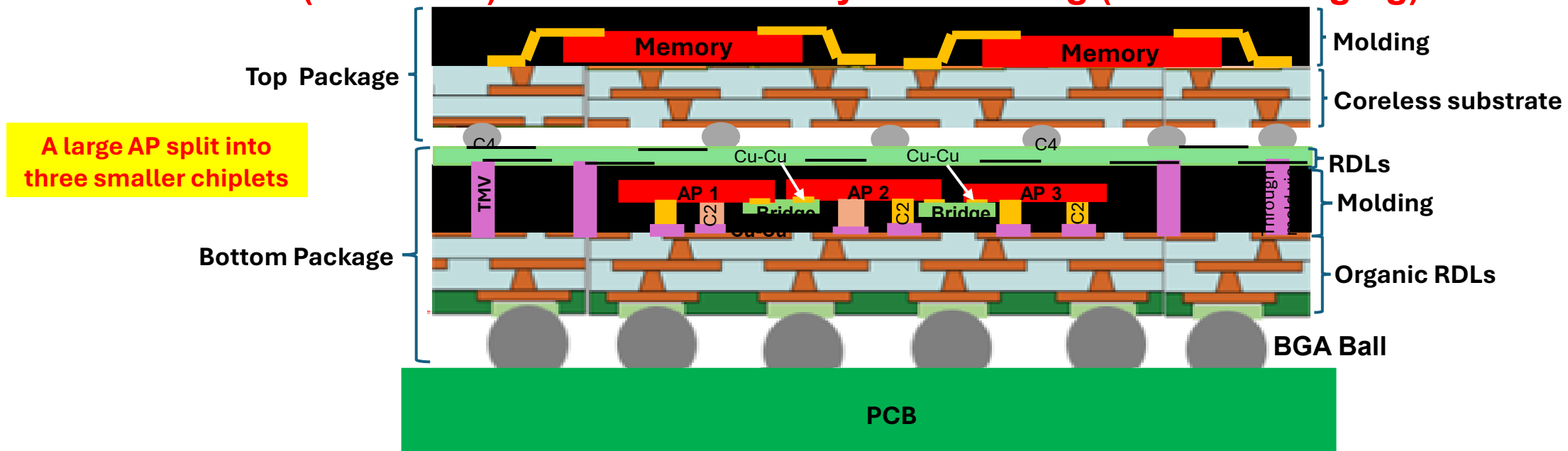


(b)

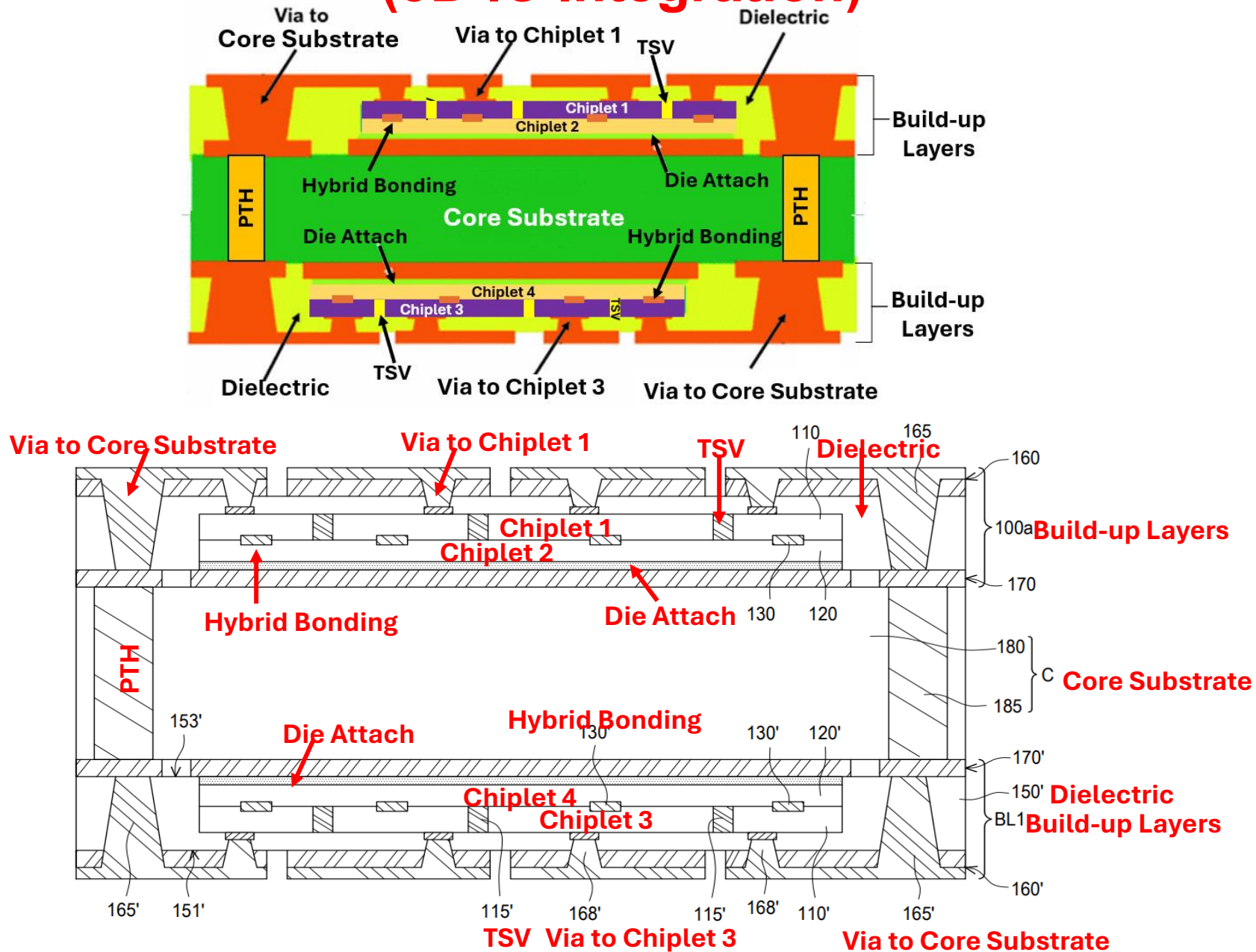
- Finer pitch (Higher density)
- Better performance
- Simpler package substrate
- Potentially lower cost



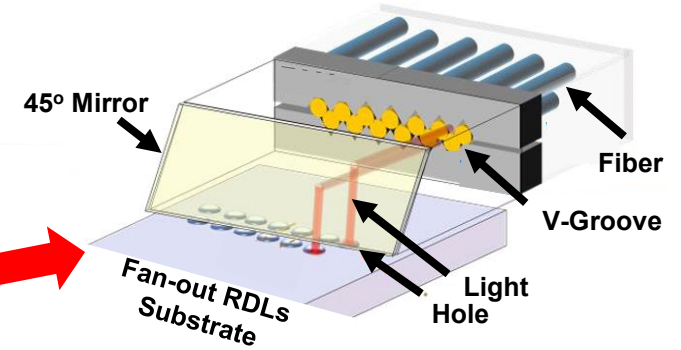
Package-on-Package (PoP) – Chiplets embedded in fan-out (RDL-First) EMC with Cu-Cu hybrid bonding (3D IC Packaging)



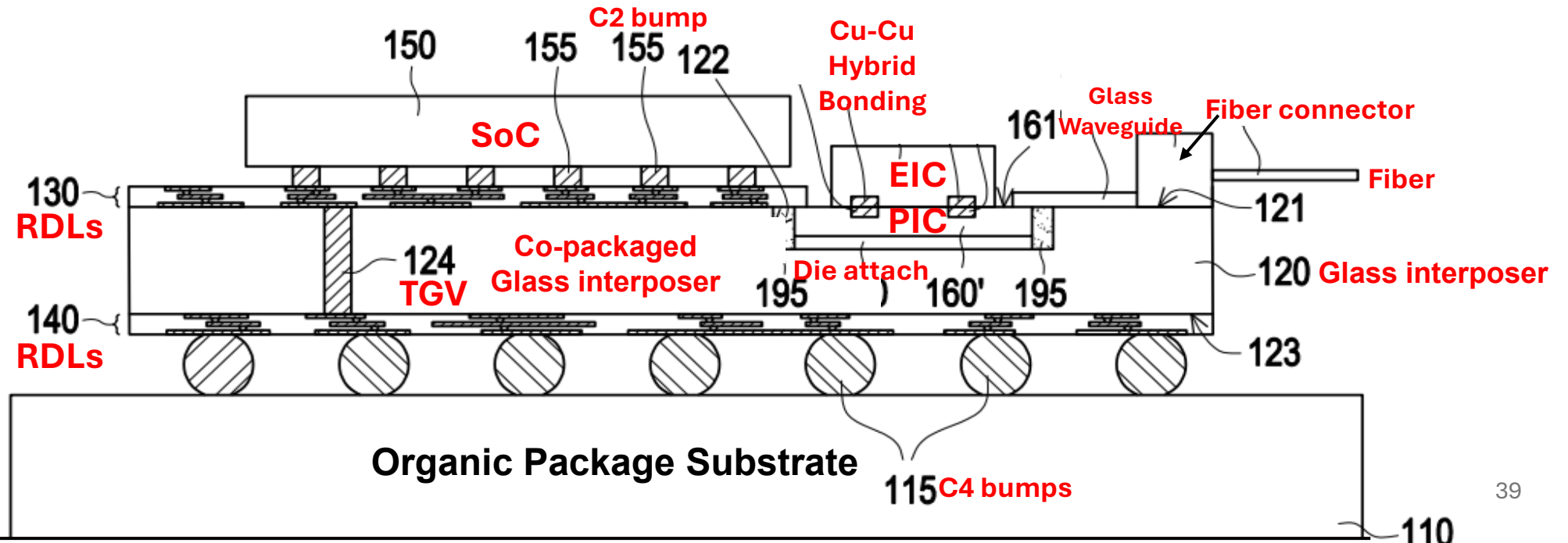
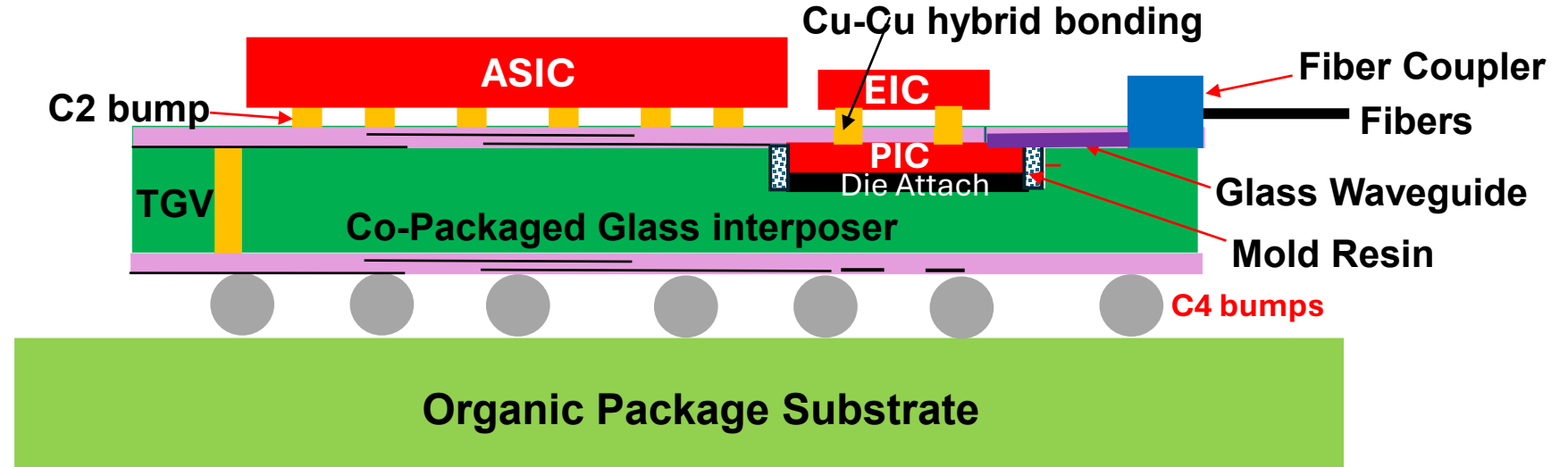
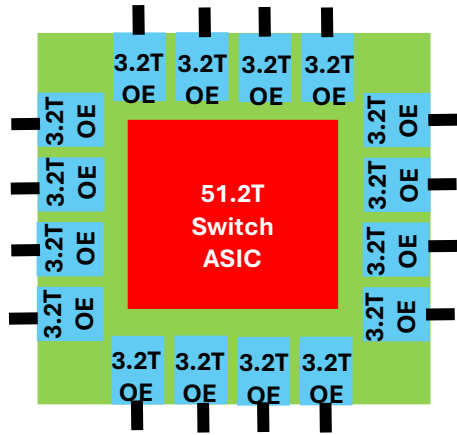
Chipselets Embedded in Build-up Substrate with Hybrid Bonding (3D IC Integration)



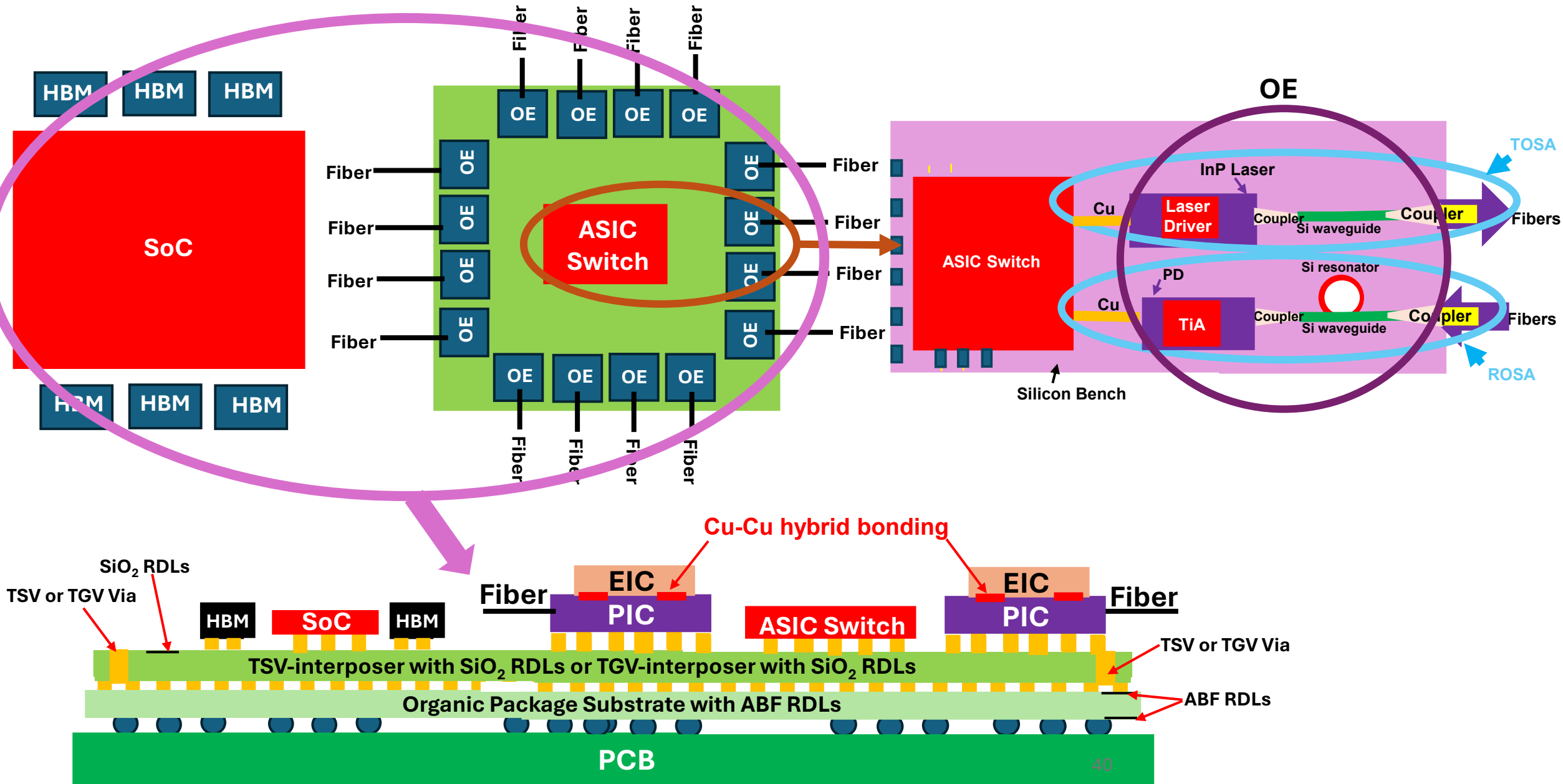
The diagram shows a square chip layout 100. In the center is a large square block labeled 130. Surrounding this central block is a ring of smaller square blocks. The top and bottom edges of this ring each contain four blocks, while the left and right edges each contain five blocks. A vertical dashed line, labeled I-I' at its ends, passes through the center of the chip. Various components are labeled with reference numerals: 110 points to the outer boundary of the chip, 120 points to the right edge of the peripheral block ring, 140 points to one of the blocks on the top edge, and 164(160) points to the blocks on the right edge.



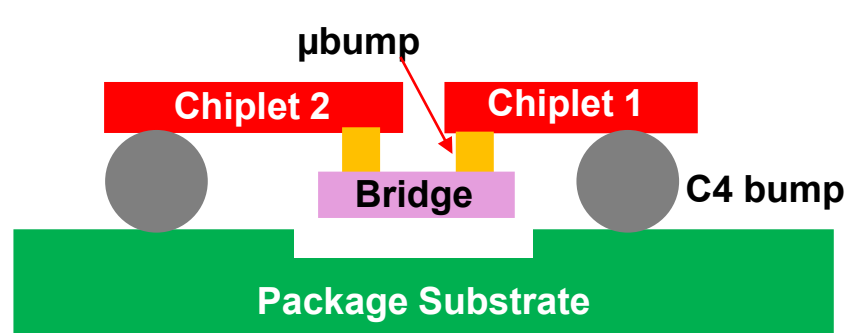
3.5D Heterogeneous Integration of PIC and EIC with Hybrid Bonding



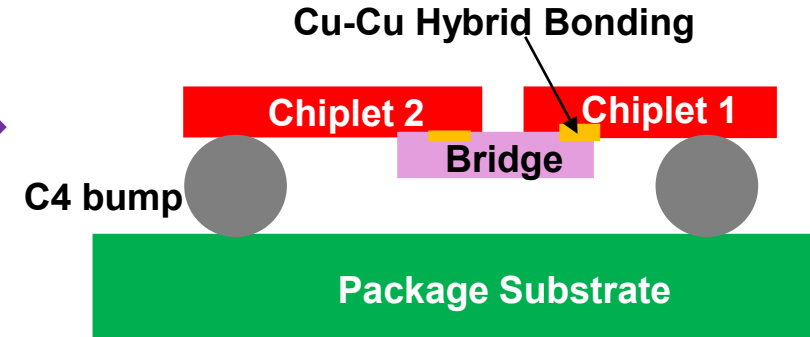
3D Heterogeneous Integration of SoC, HBM, Switch, EIC, and PIC with Silicon Photonics for HPC and Data Centers Driven by AI and High-Speed and High-Bandwidth Communication



Hybrid Bonding Bridge for Chiplets (2D IC Integration)

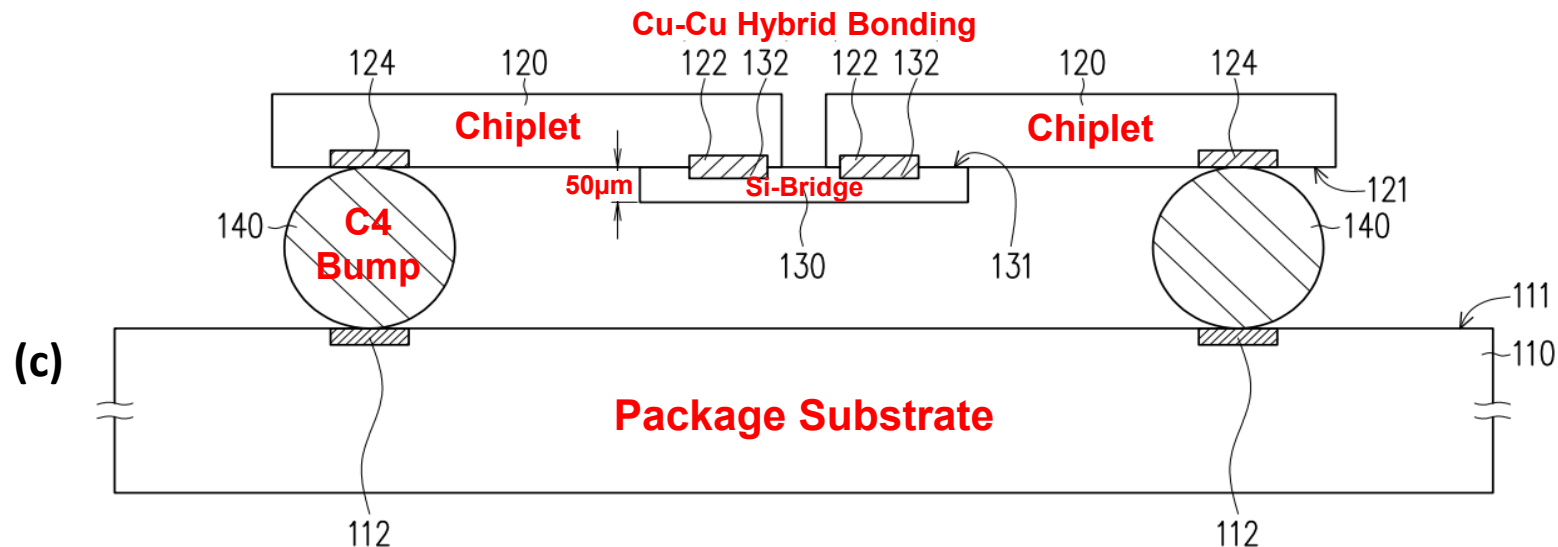


(a)



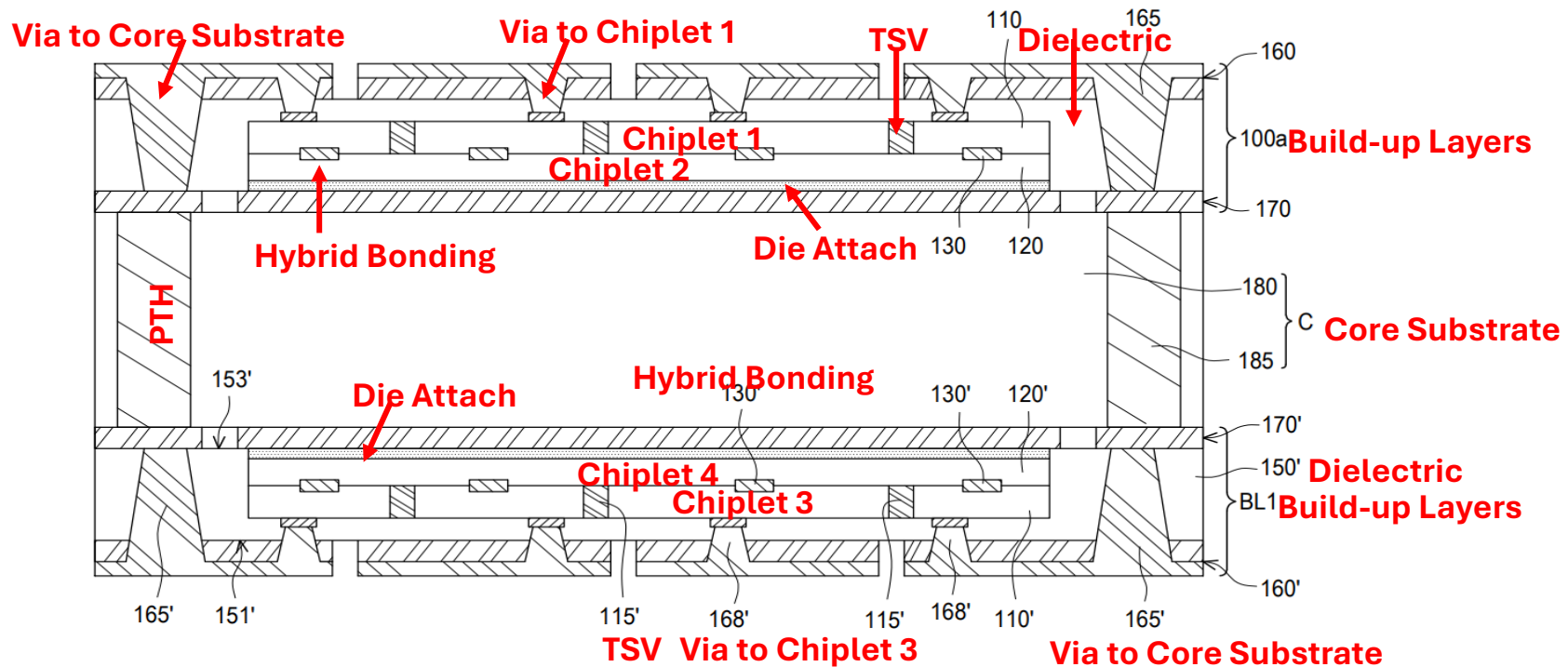
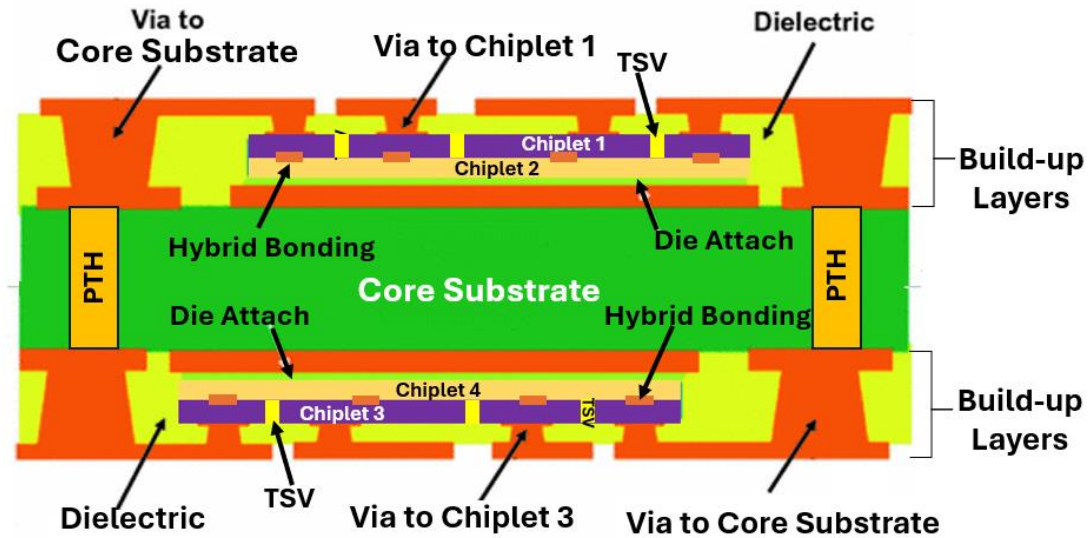
(b)

- **Finer pitch (Higher density)**
- **Better performance**
- **Simpler package substrate**
- **Potentially lower cost**

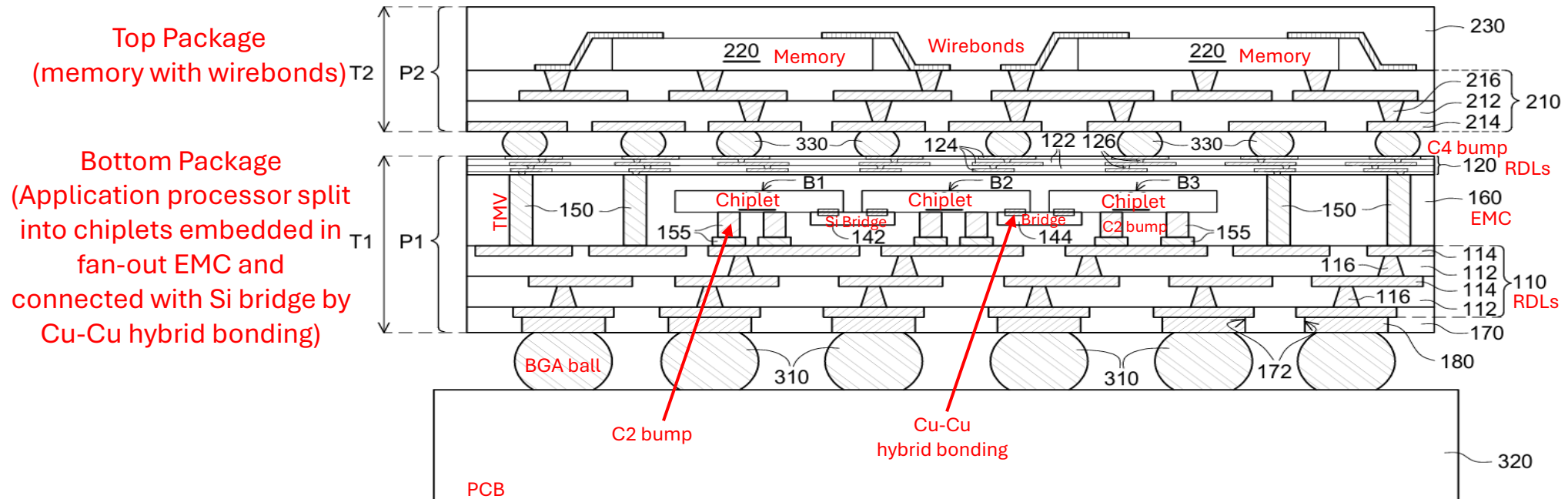
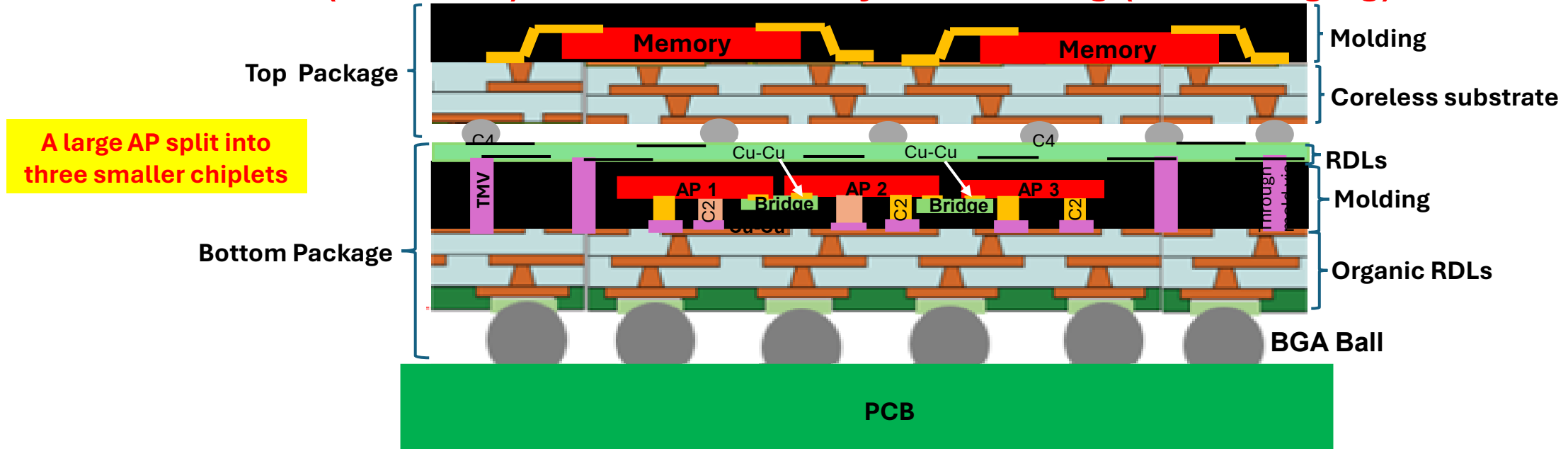


(c)

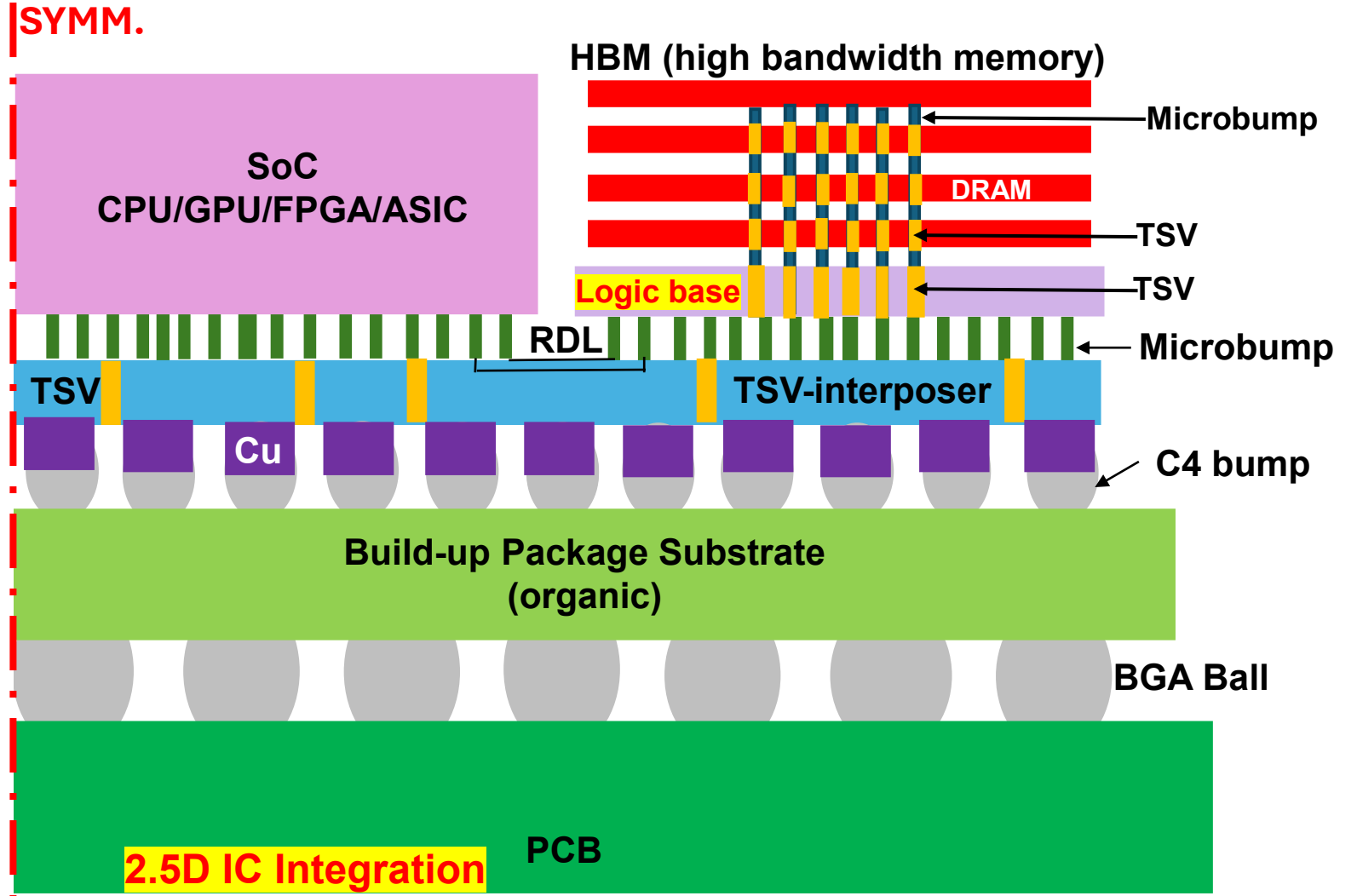
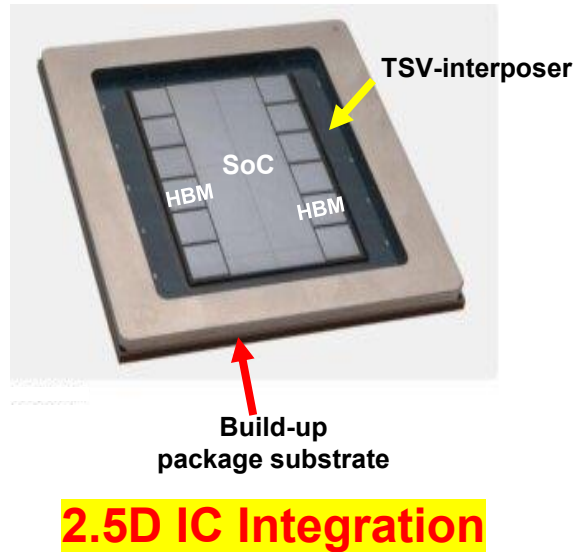
3D Chiplets Embedded in Build-up Substrate with Hybrid Bonding



Package-on-Package (PoP) – Chiplets embedded in fan-out (RDL-First) EMC with Cu-Cu hybrid bonding (3D Packaging)



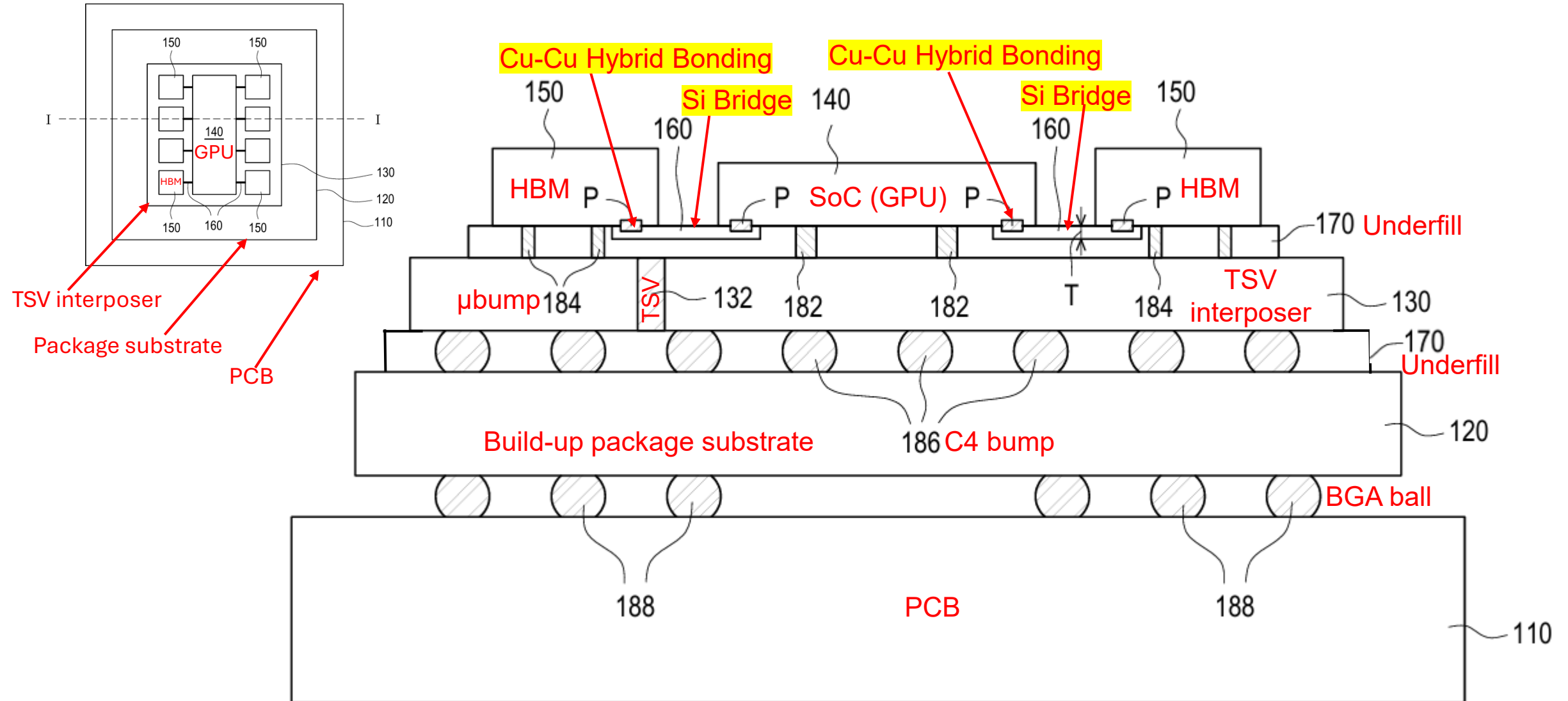
Today, Packaging of Choice (2.5D) for High-Performance Computing (HPC) Driven by Artificial Intelligence (AI)



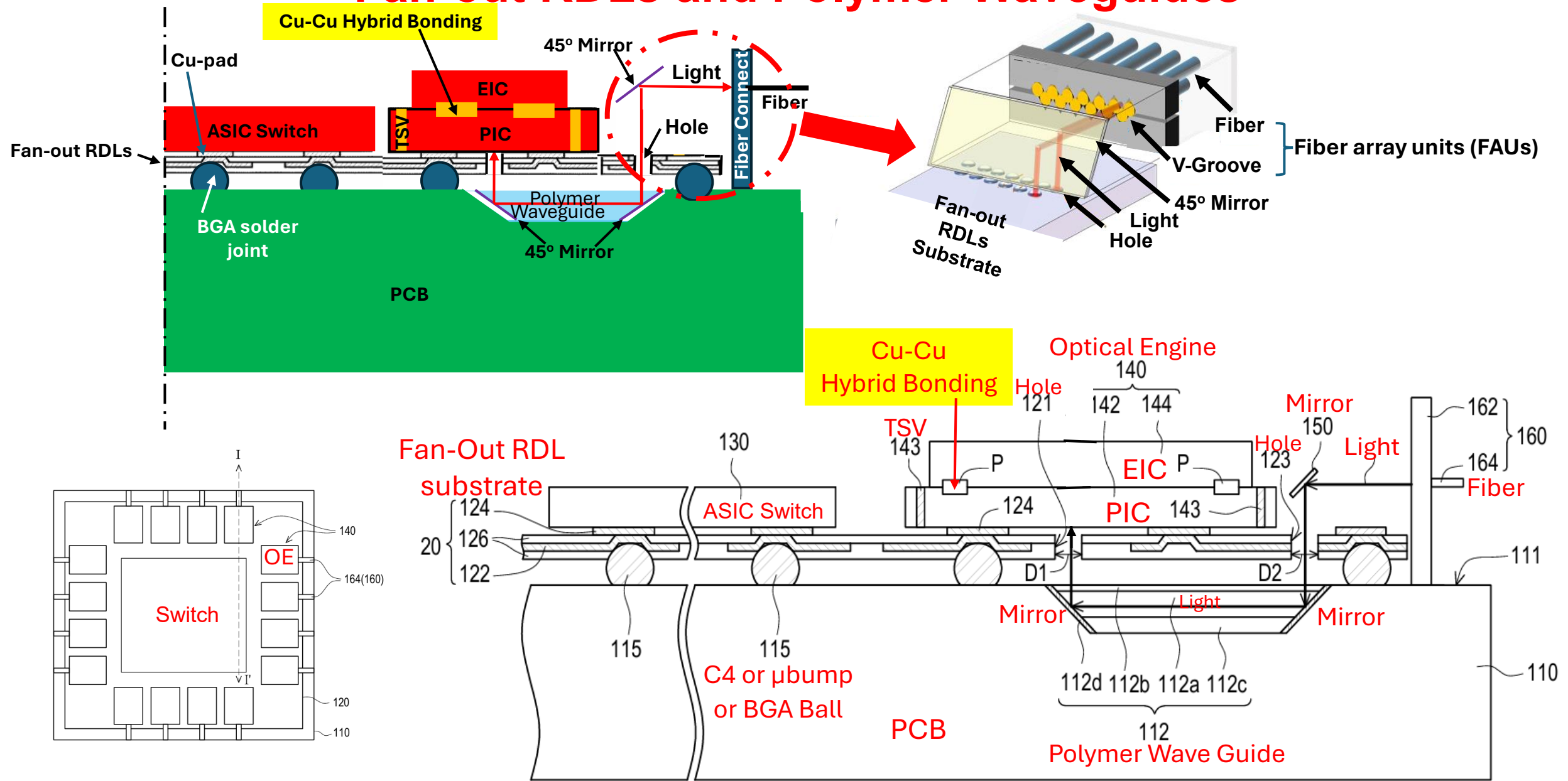
Today, how to take the heat out from the SoC and HBMs is a big problem.

Package of Choice for HPC Driven by AI (Today)

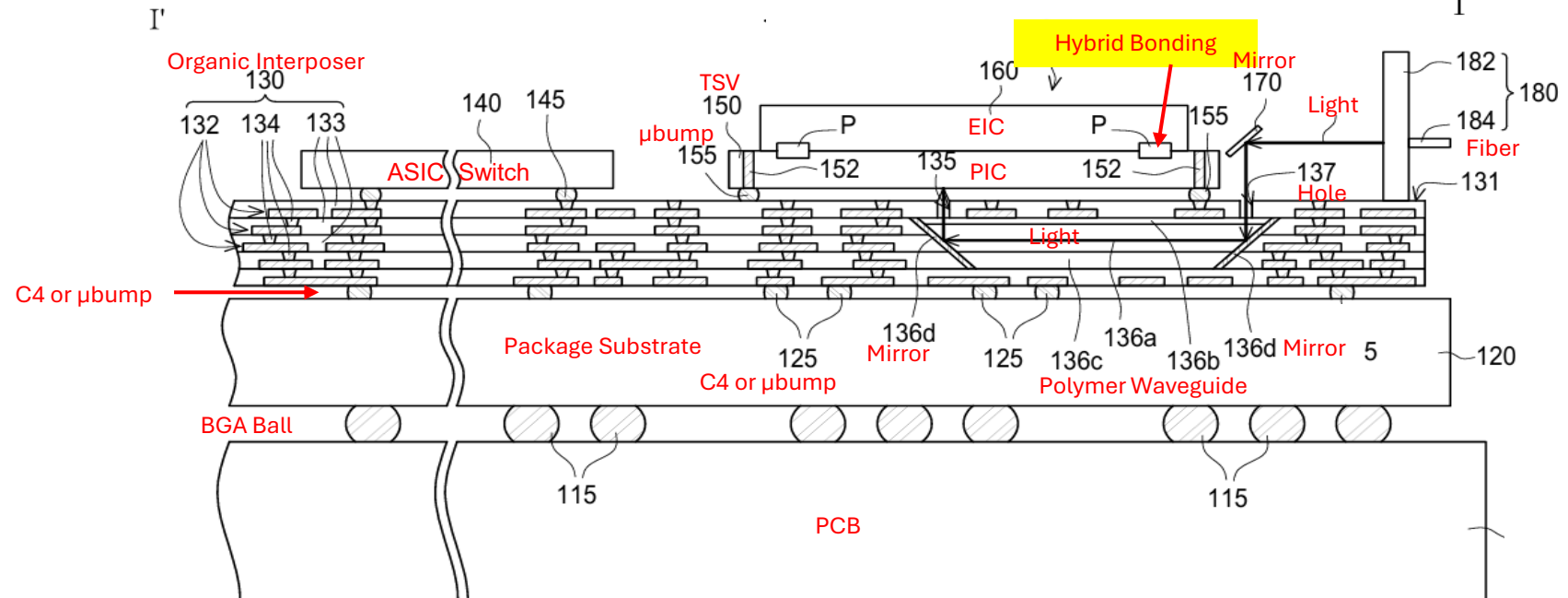
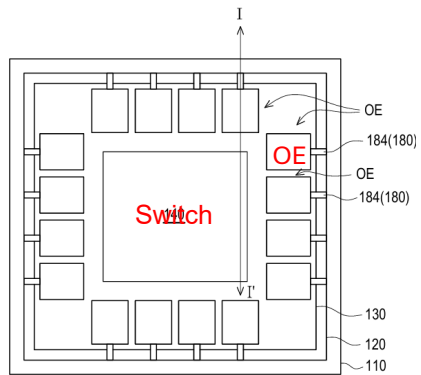
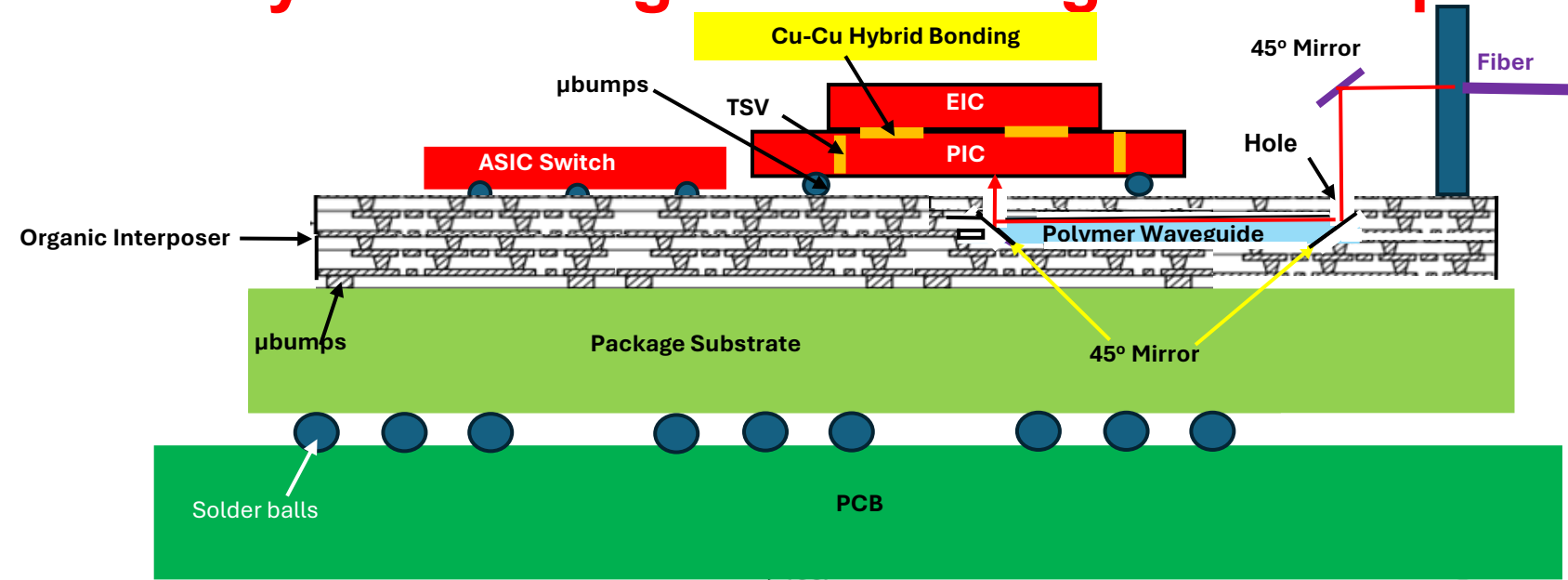
2.5D IC Integration of SoC and HBM with Si Bridge by Hybrid Bonding



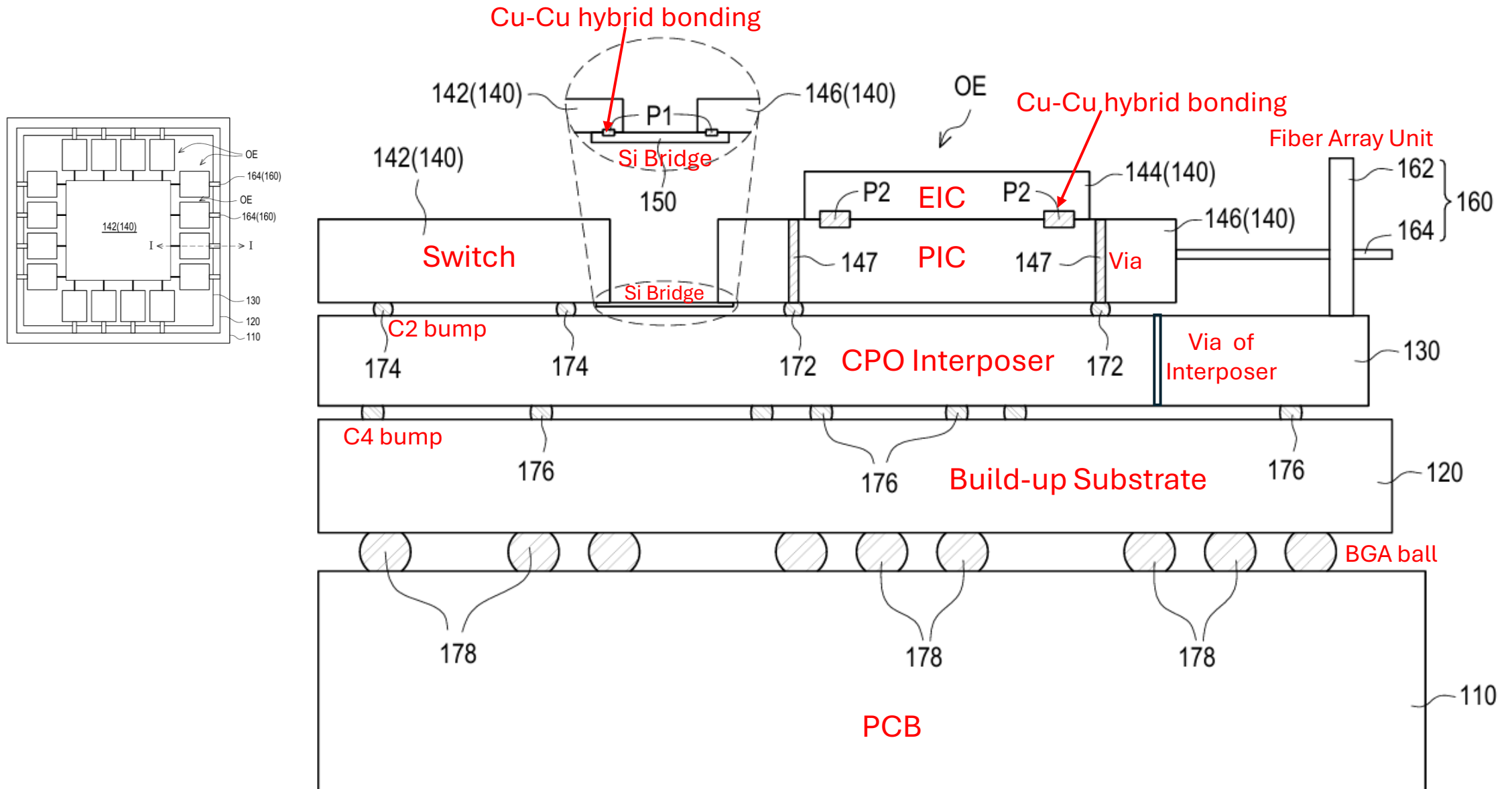
3D Heterogeneous Integration of PIC and EIC with Hybrid Bonding on Fan-out RDLs and Polymer Waveguides



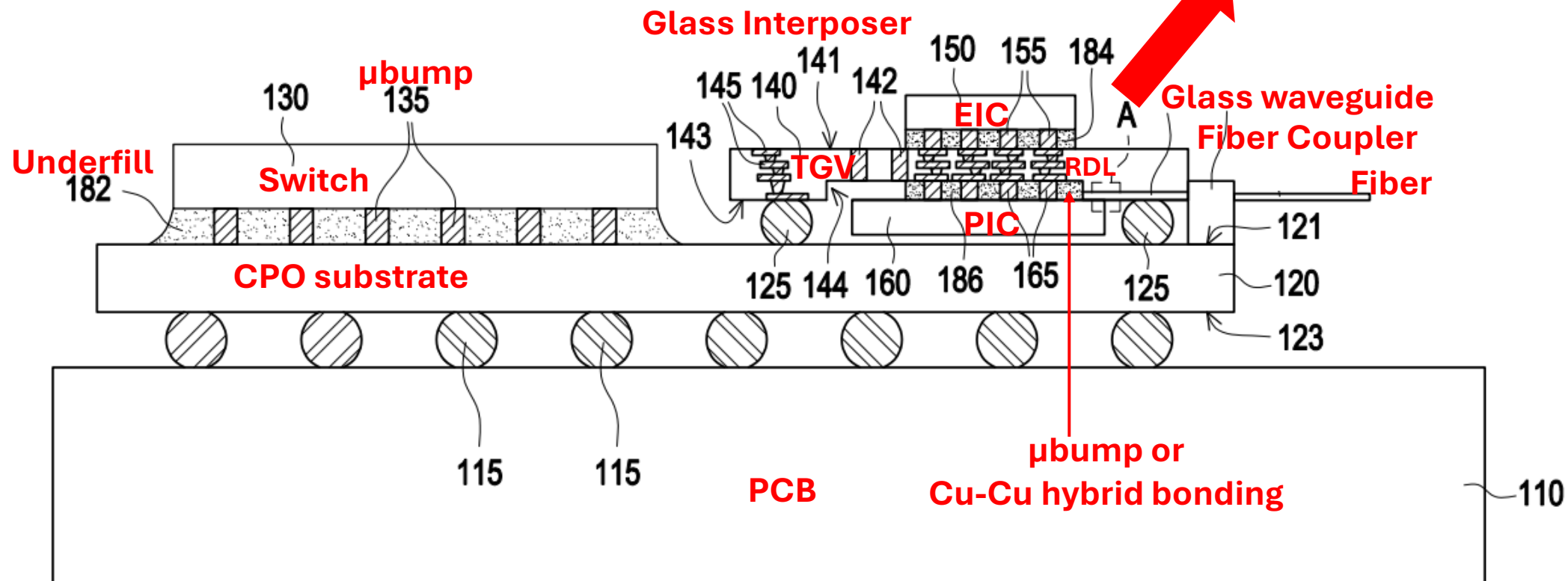
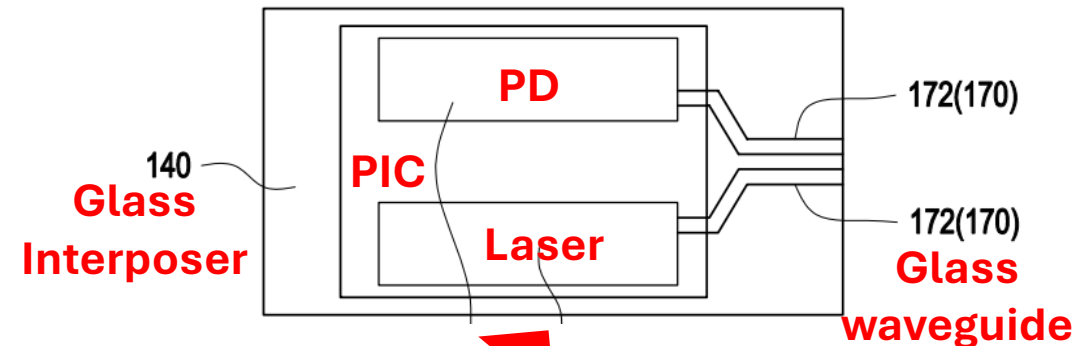
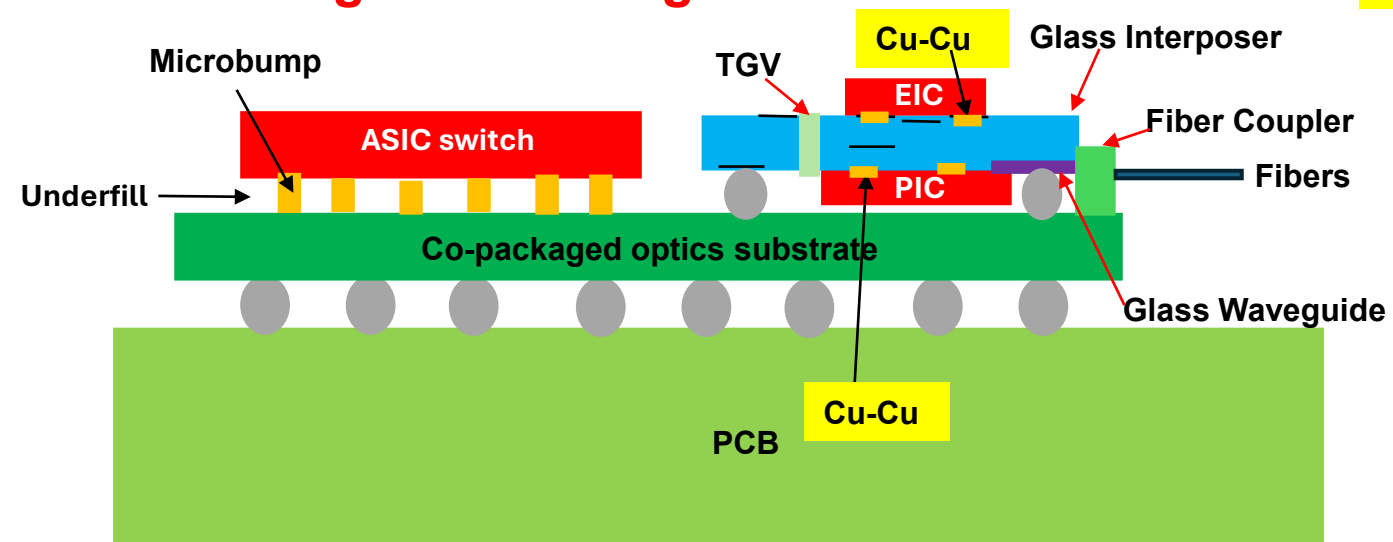
3.5D Heterogeneous Integration of OE (EIC and PIC) and ASIC Switch on Embedded Polymer Waveguide and Organic Interposer



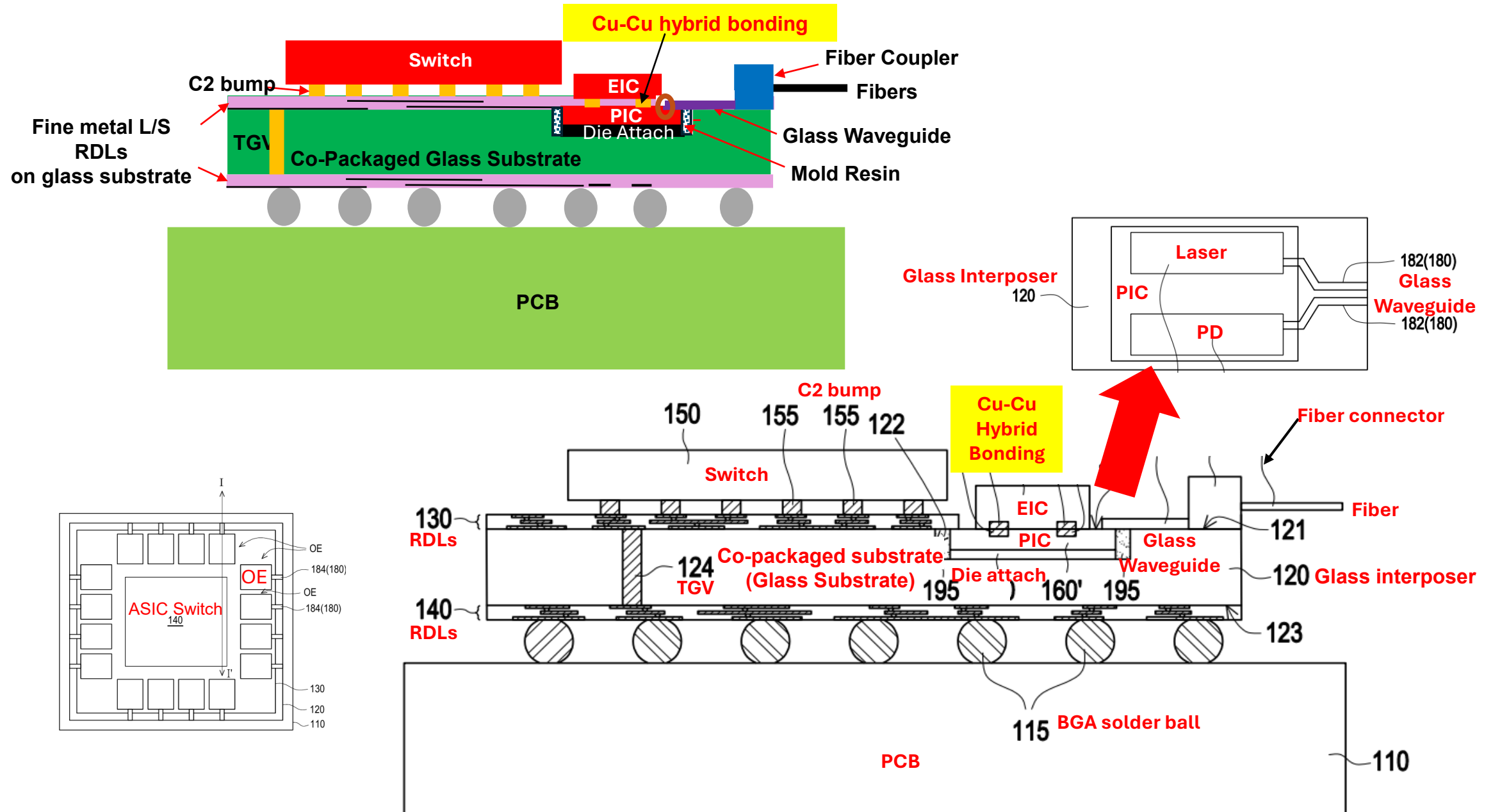
Co-Packaged Optics: 3.5D Heterogeneous Integration of PIC and EIC and Switch with Si Bridge by Hybrid Bonding



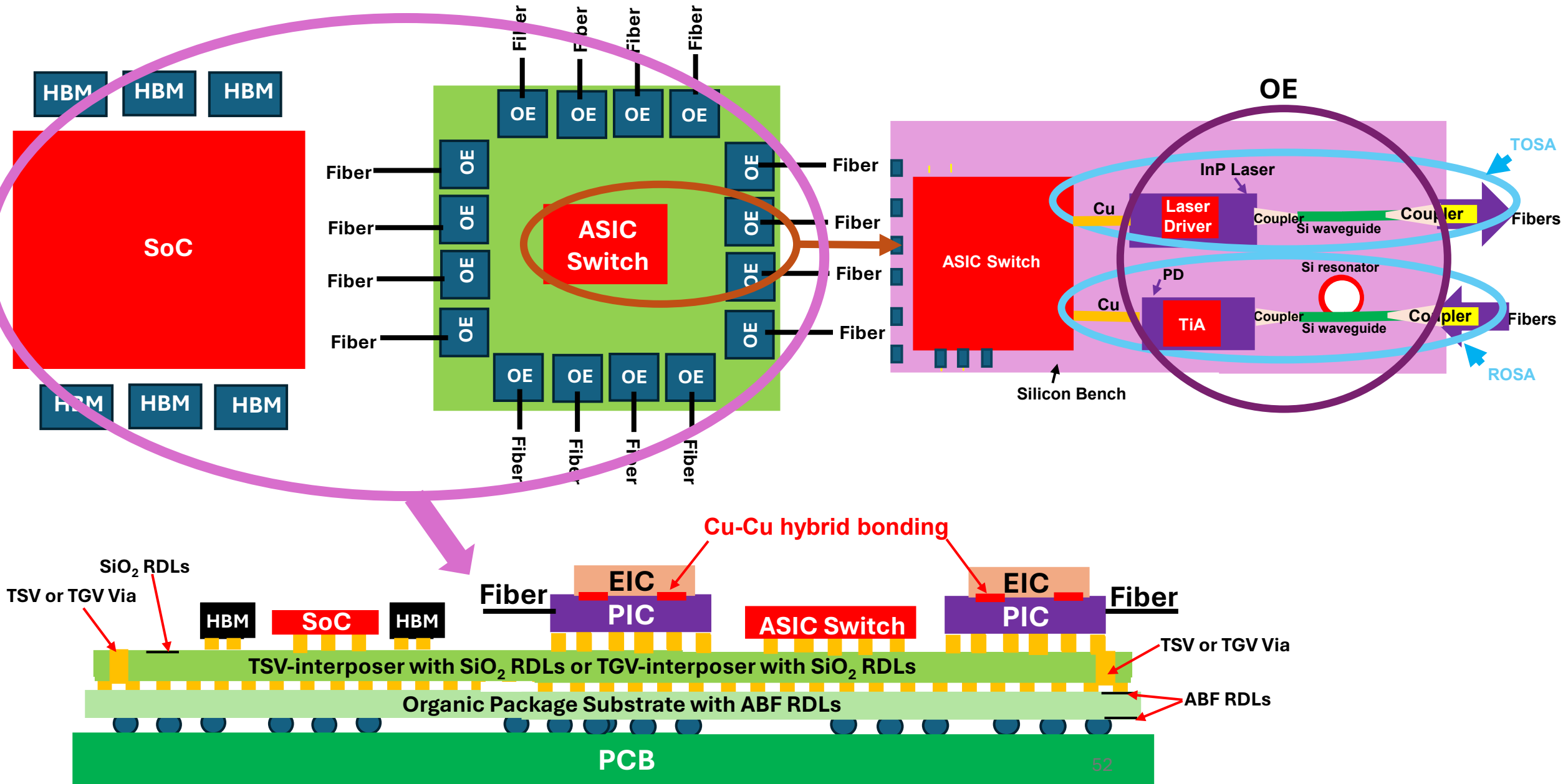
3D Heterogeneous Integration of PIC and EIC with Glass Interposer and Cu-Cu Hybrid Bonding



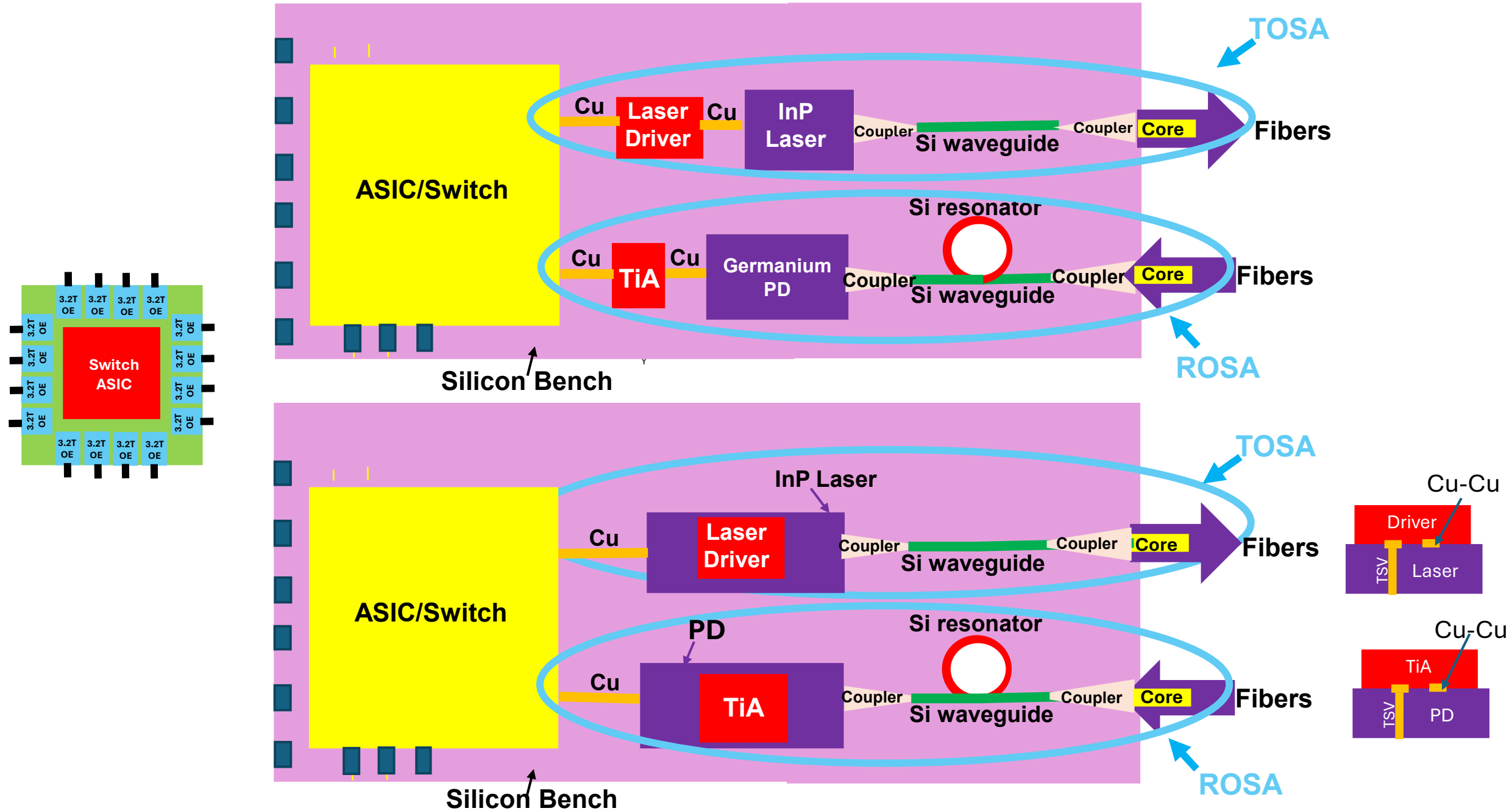
3D Heterogeneous Integration of EIC and PIC by Cu-Cu Hybrid Bonding with the PIC Embedded in a co-packaged substrate (Glass Substrate)



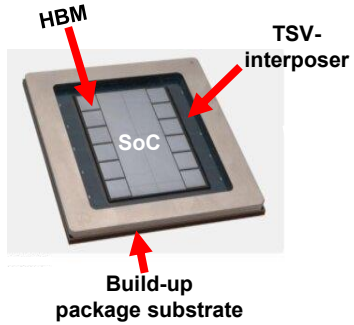
3D Heterogeneous Integration of SoC, HBM, Switch, EIC, and PIC with Silicon Photonics for HPC and Data Centers Driven by AI and High-Speed and High-Bandwidth Communication



3D CPO - PIC and EIC Stacked by Cu-Cu Hybrid Bonding with Silicon Photonics



Thermal Management of 2.5D IC Integration with Hybrid Bonding and TSV Interposer with Microchannels

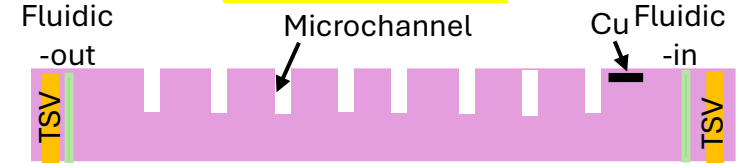


2.5D IC Integration

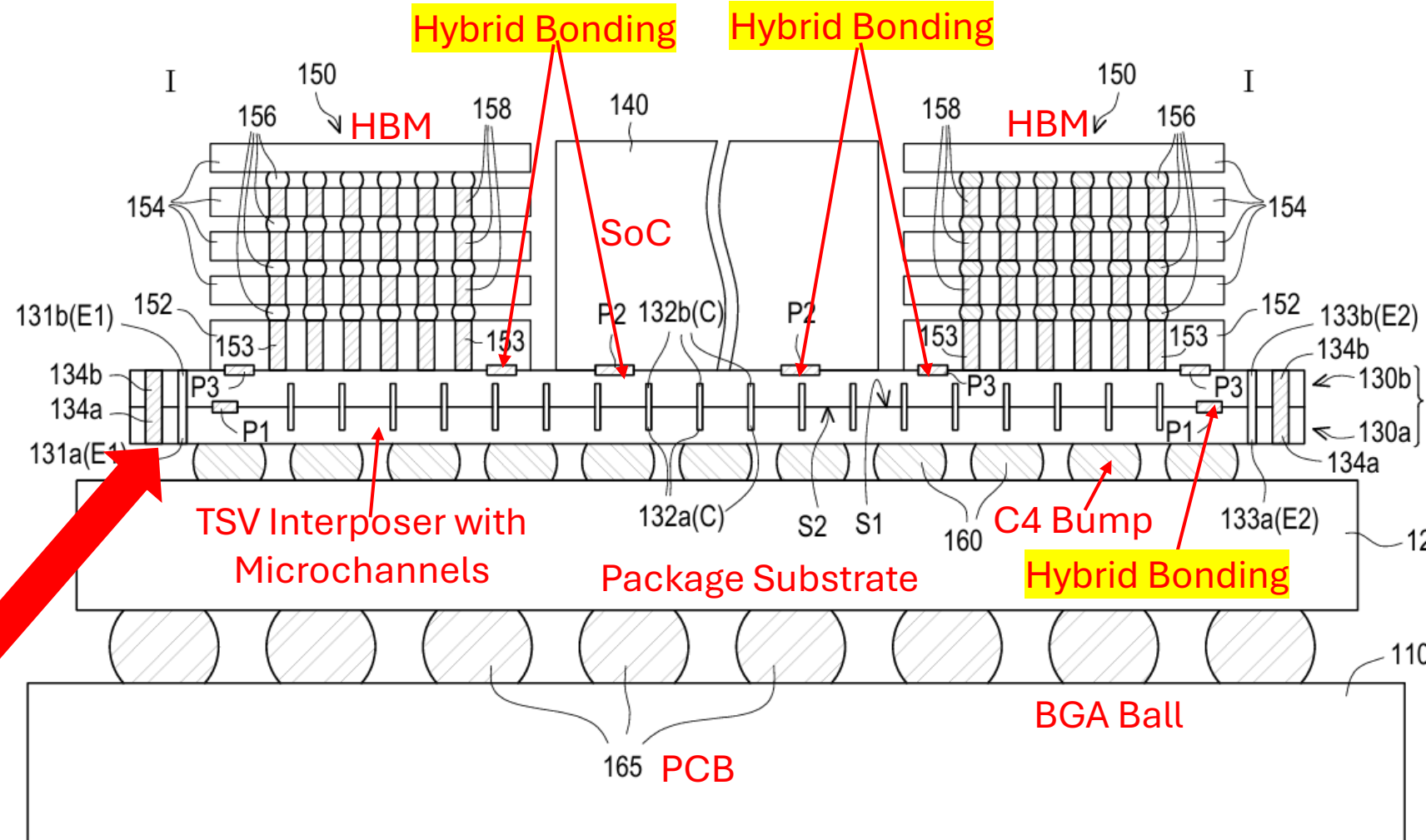
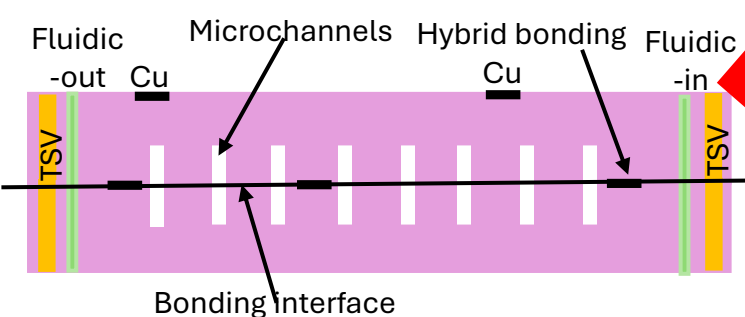
Top Si interposer

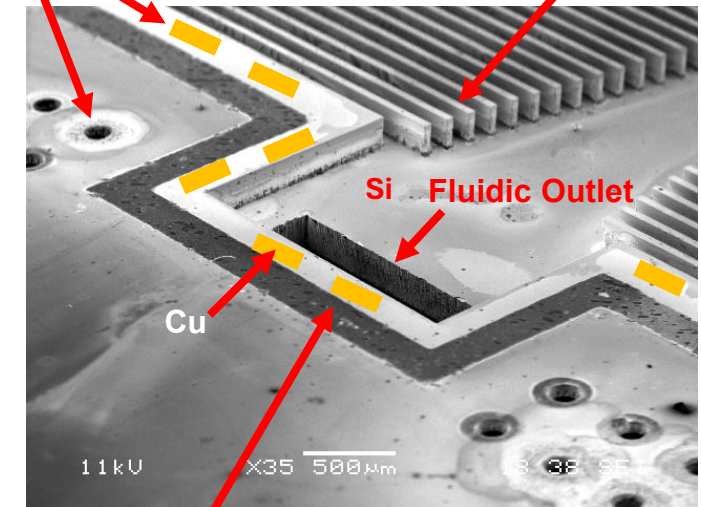
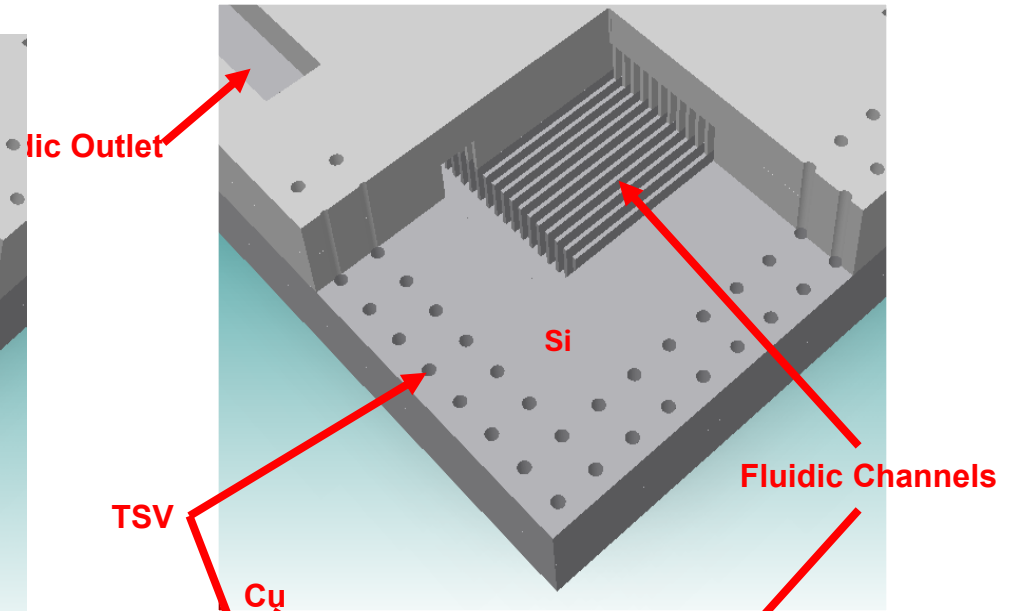
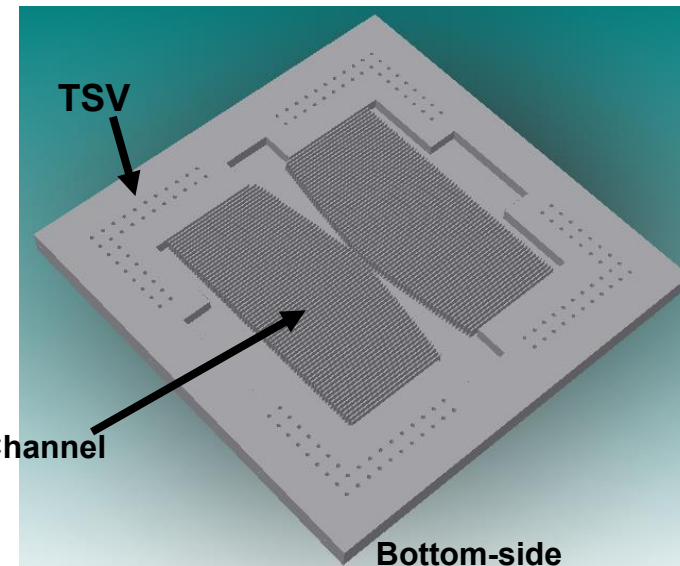
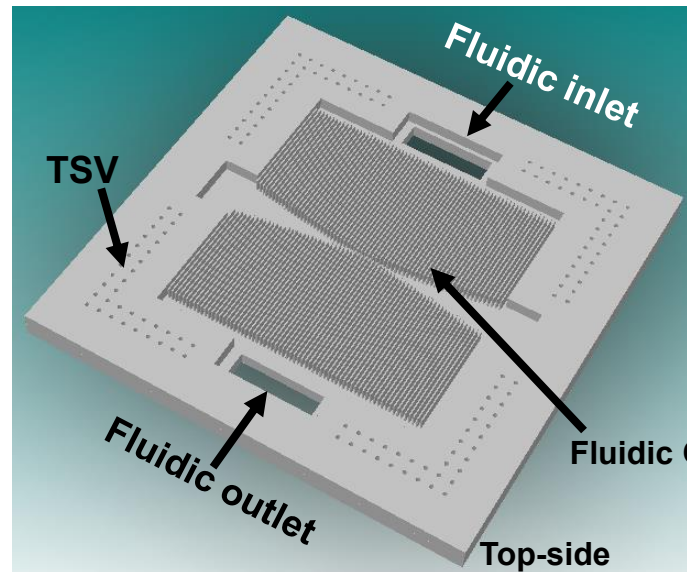
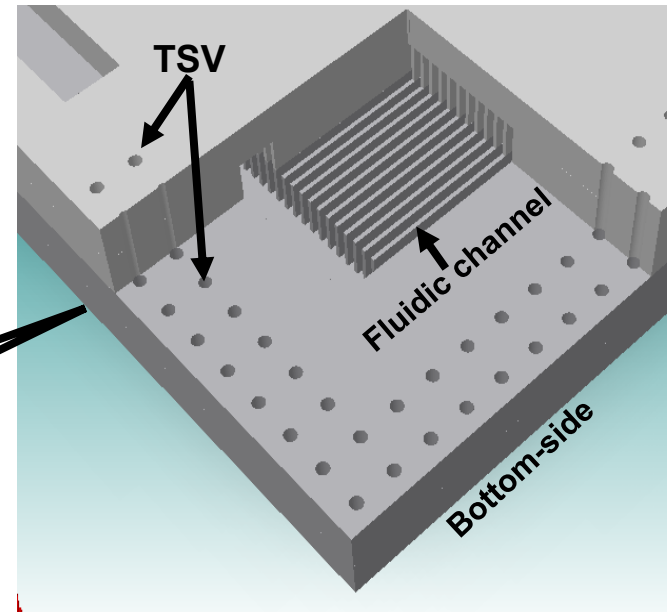
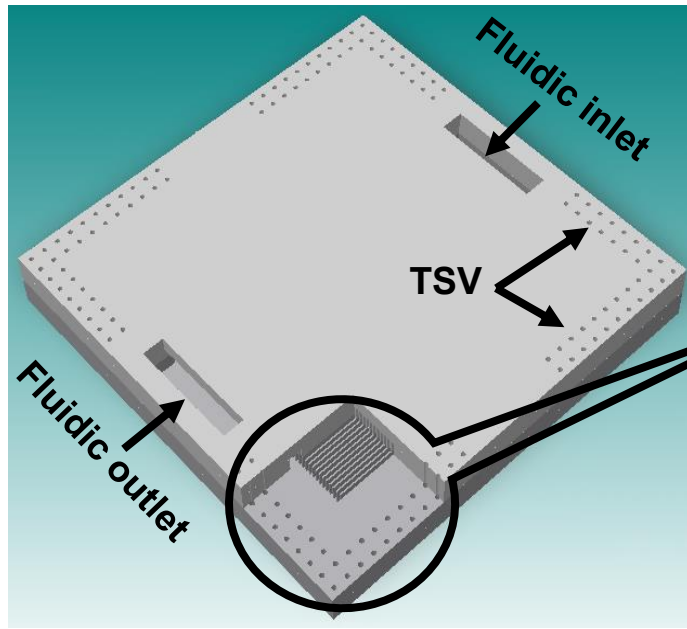


Bottom Si interposer



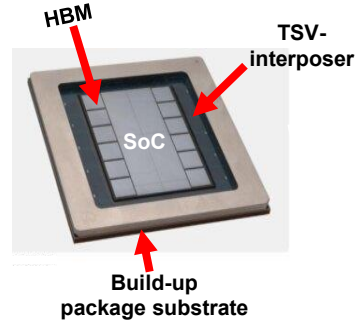
Combined Si interposer



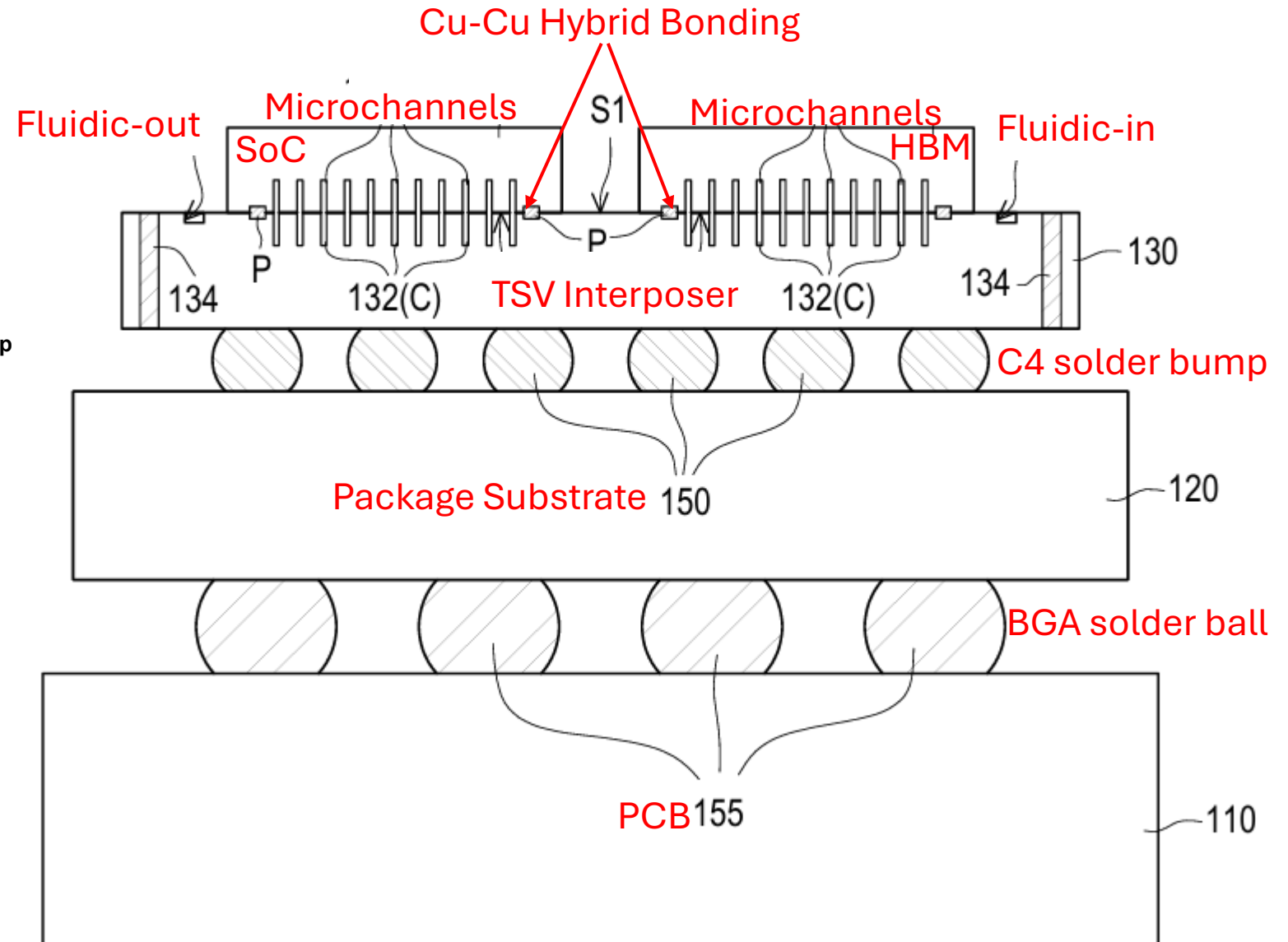
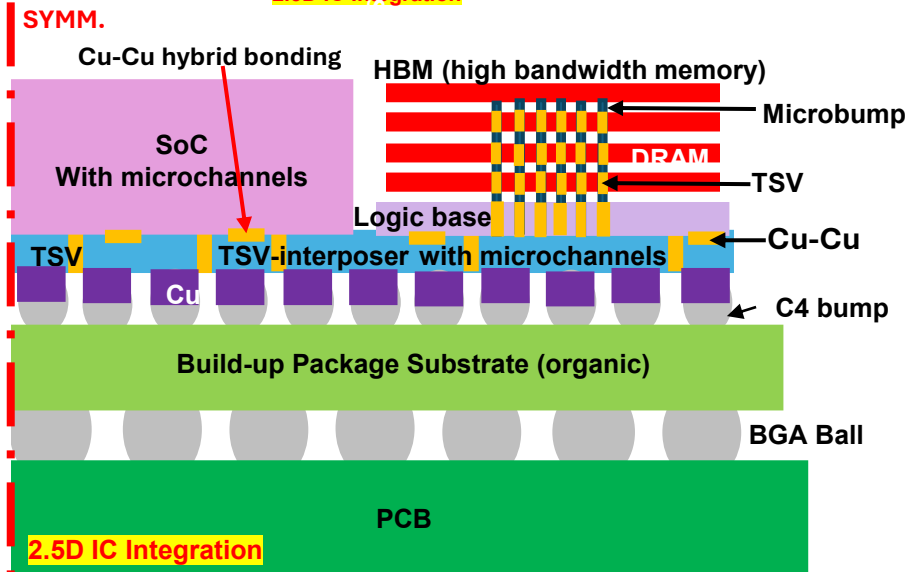


Sealing ring (Cu-Cu hybrid bonding) around the fluidic channels

Thermal Management of 2.5D IC Integration with Microchannels and Cu-Cu Hybrid Bonding



2.5D IC Integration



RECOMMENDATIONS

- Due to the requirement of higher interconnect density, finer pitch, more compact 3D integration, lower power consumption, lower latency, higher bandwidth, and better signal integrity of a **co-packaged optics** system, the **Cu-Cu hybrid bonding** of some of the **photonic IC** and **electronic IC** are strongly recommended.
- In order to reduce the package size and enhance the electrical and thermal performance, **hybrid bonding some of the chiplets before packaging heterogeneous integration (3.5D IC integration)** is strongly recommended.
- More **quality and reliability data** such as the thermal-cycling, thermal shock, mechanical vibration, mechanical shock, high-temperature storage, highly accelerated temperature, highly accelerated moisture resistance etc. **of Cu-Cu hybrid bonding** are desperately needed. **Thermal management of Cu-Cu hybrid bonding** will be an **important topic**.

Glass Substrates Contents

- **Introduction**
- **Glass Substrate vs. Glass Interposer**
- **Process Flow of Glass Substrate/Interposer**
- **Flip Chip on Glass Substrate with μ Bumps**
- **Flip Chip on Glass Substrate with Hybrid Bonding**
- **Summary and Recommendations**

Why Glass Packaging?

It is because of high-performance computing (HPC) and Data Centers driven by Artificial Intelligence (AI)!

- The **AI computing power arms race** has expanded beyond core chip processing capabilities to encompass a materials revolution - the very "skeleton" of the technology.
- Glass substrates/interposer - once seemingly unassuming but now undergoing a spectacular transformation within the realm of **semiconductor packaging** - have emerged as the central protagonists of this revolution.
- As the computing power of AI chips continues to escalate - alongside the integration of increasingly high-bandwidth memory (HBM) - packaging processes have grown correspondingly complex. Consequently, traditional copper-clad laminates (CCLs) - typically composed of resin and fiberglass fabric - have begun to encounter their **physical limits**.
- When substrate/interposer dimensions exceed **120mm to 140mm**, issues such as the "**warping**" of organic materials and **thermal dissipation bottlenecks** place chip stability in jeopardy.
- Leveraging their inherent physical properties, **glass substrates/interposers** have therefore made a cross-industry leap - transitioning from the display panel sector to the battleground of **advanced semiconductor packaging**.

Definition of Glass Packaging

**The glass (substrate or interposer)
is a part of a package structure!**

or

**A glass package must have a glass
substrate or interposer!**

**Glass panel or wafer as a
temporary carrier of
FOWLP or FOPLP –
not part of a package**

Glass as a Temporary Panel Carrier for FOPLP

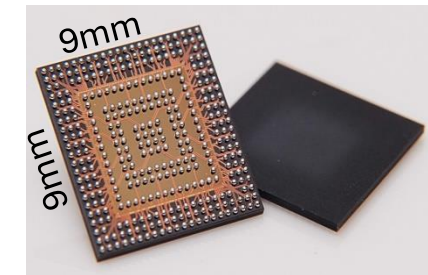
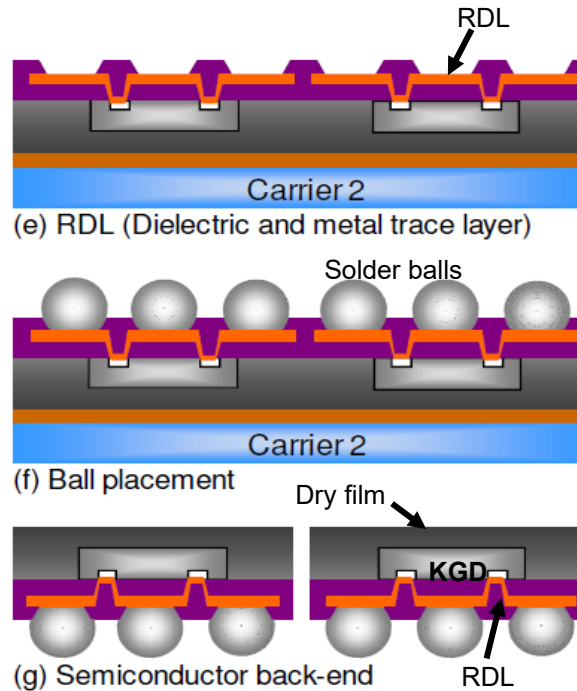
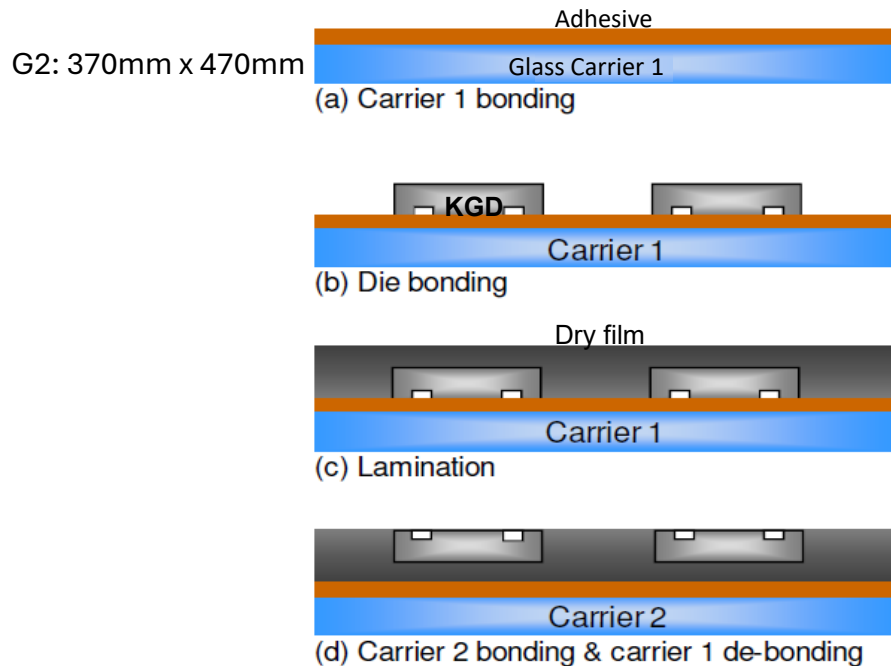
People say: "... the glass substrate of fan-out panel-level packaging (FOPLP) ..."

This is wrong!

There is no glass substrate in the FOPLP!

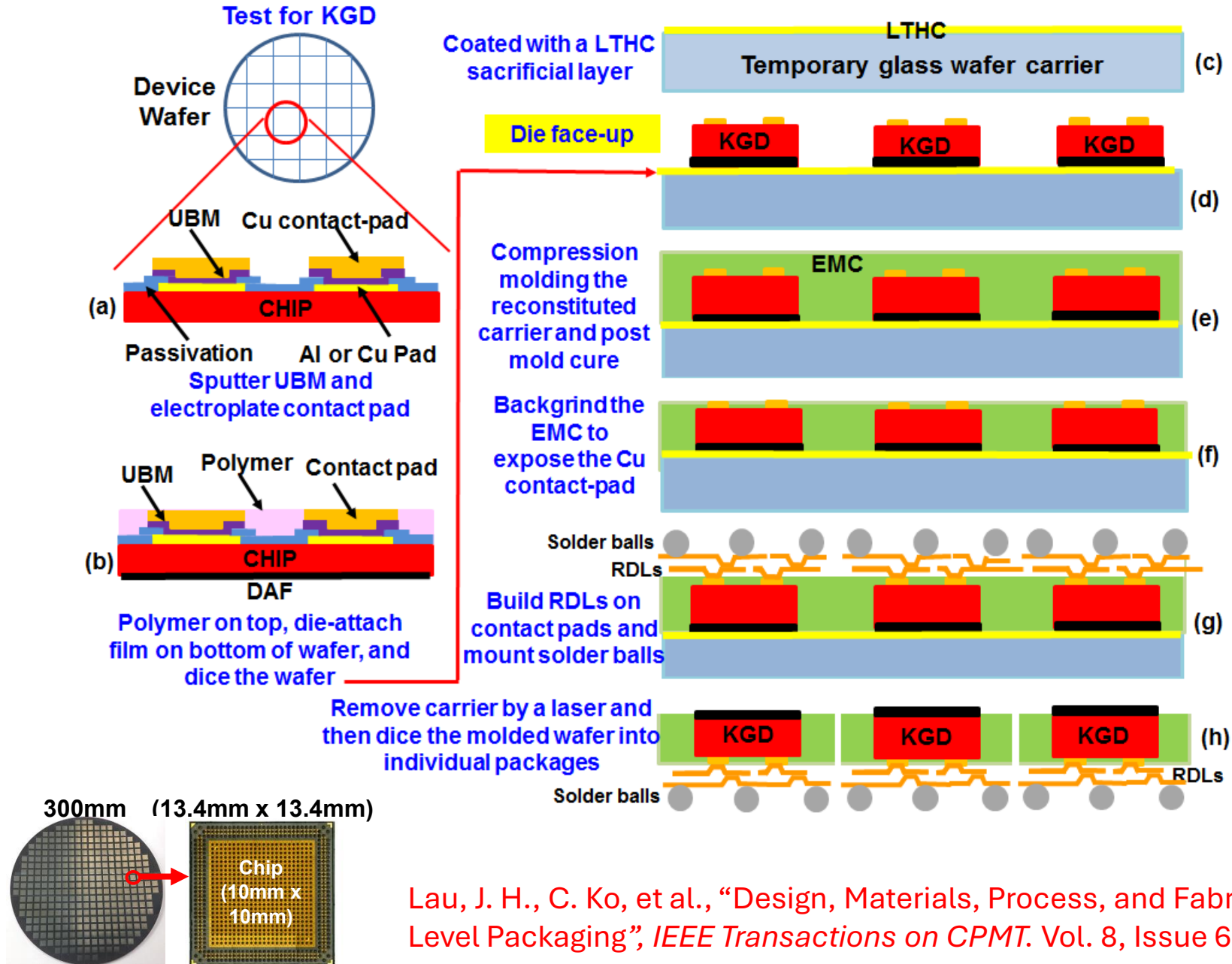
FOPLP is not a glass packaging!

FOPLP process with Glass as a Temporary Carrier



- FOPLP with RDLs substrate
- There is no glass substrate

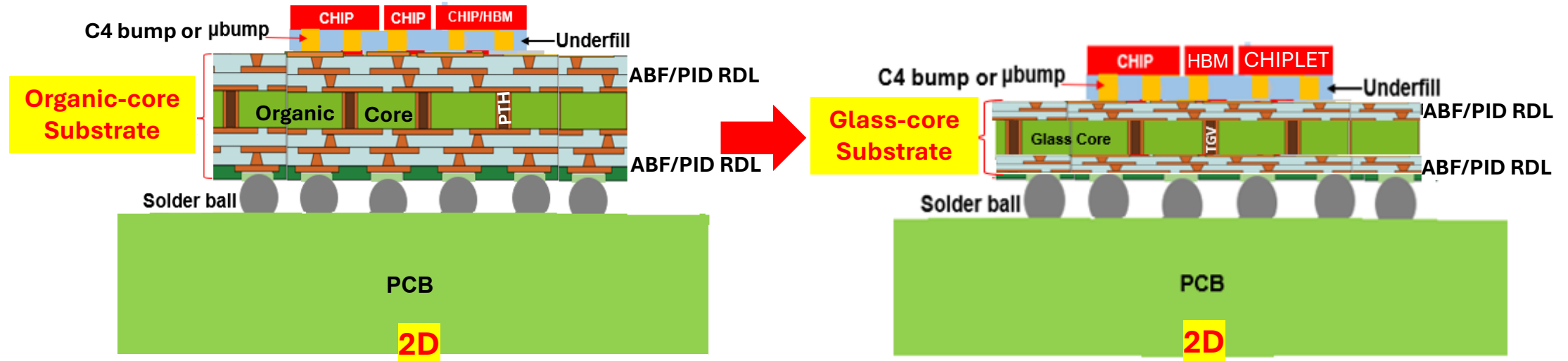
Glass as a Temporary Wafer Carrier for FOWLP



Lau, J. H., C. Ko, et al., "Design, Materials, Process, and Fabrication of Fan-Out Wafer-Level Packaging", *IEEE Transactions on CPMT*. Vol. 8, Issue 6, June 2018, pp. 991-1002.

Glass Substrate vs. Glass Interposer

Organic-core Substrate vs. Glass-core Substrate



The key advantages of glass-core substrate over the organic-core substrate are:

- Superior flatness
- Better dimensional stability
- Better heat resistance
- Finer L/S RDLs
- Cu-Cu hybrid bonding for chiplets
- etc.

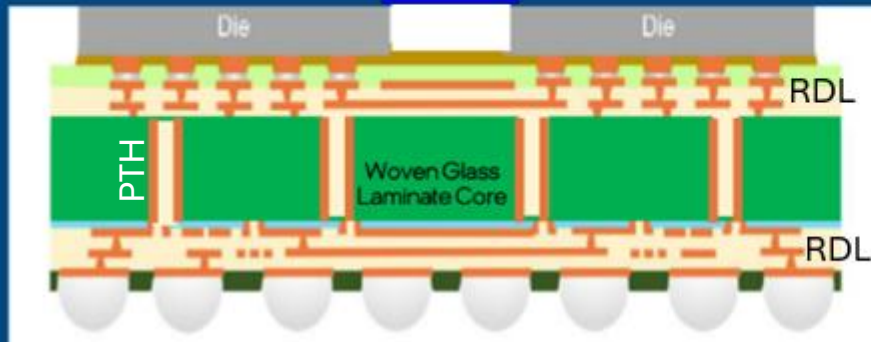
Intel's Glass Packaging

On September 18, 2023, ...

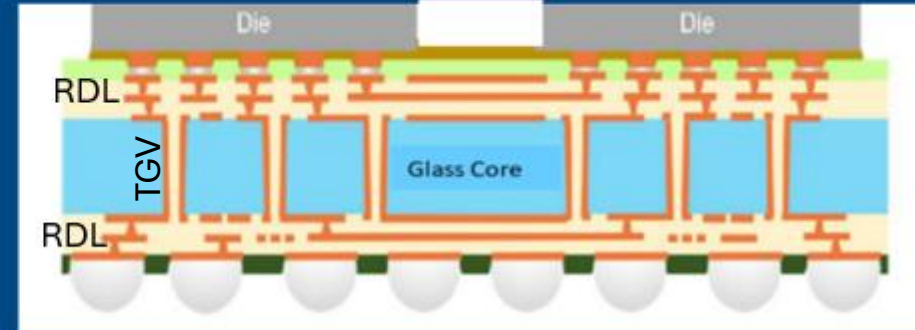
- Intel has announced a new glass-substrate technology for the next generation of **high-power processors**.
- Intel is on the path to delivering **1 trillion transistors** on a package by **2030** and its ongoing innovation in advanced packaging including **glass substrates** will help achieve this goal.

Intel Glass Core Substrate

Organic Substrate



Glass Core Substrate



Compared to organic substrates, glass substrates offer:

- Superior flatness
- Better dimensional stability
- Better heat resistance
- Finer RDL (L/S)

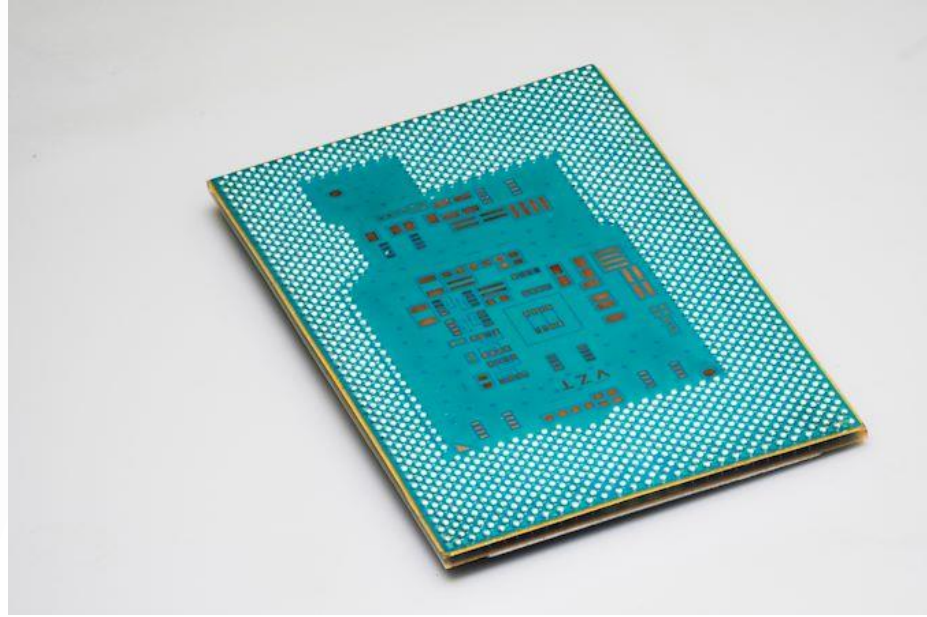
*Based on internal analysis of Intel products and projections of future Intel products

intel

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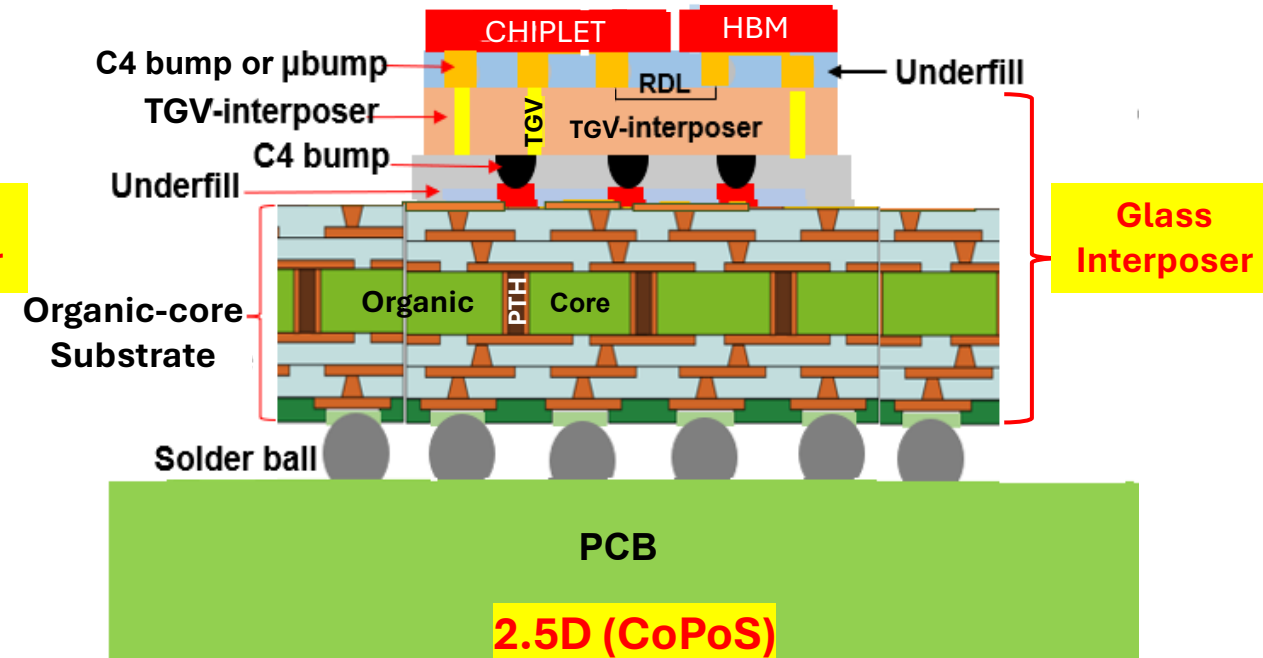
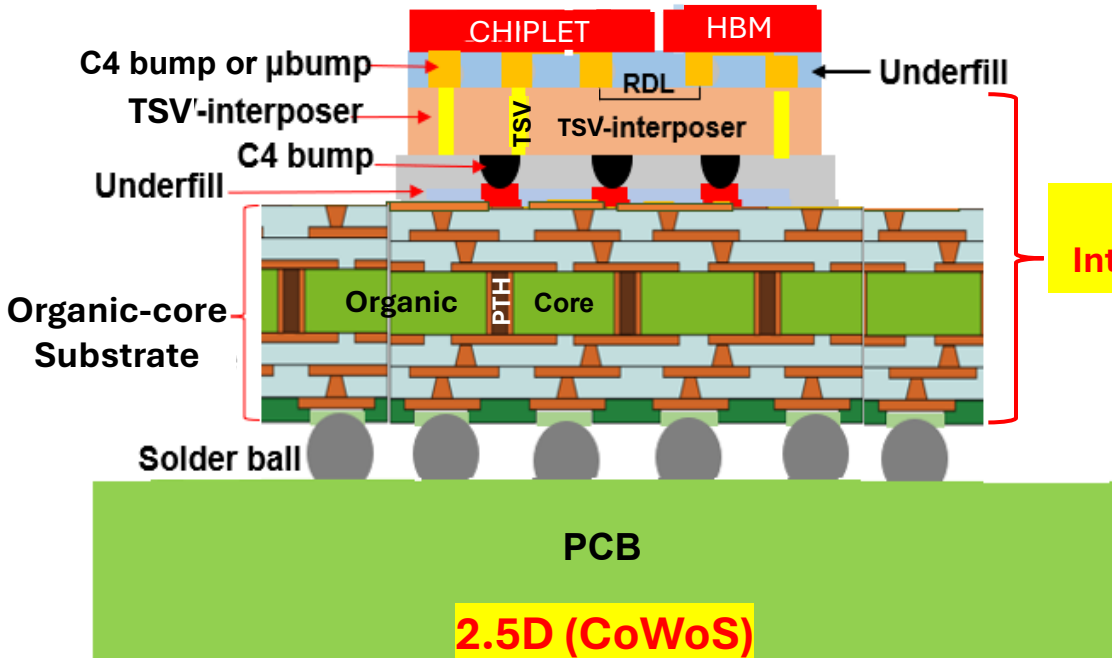
- On **September 18, 2023**, Intel told the world that they had spent more **one billion dollars** in glass packaging R&D. It is for their **1 trillion transistors** on a package to be shipped by **2030**
- During **July 2025**, Intel **stopped** all the in-house glass **manufacturing** activities and started licensing its extensive glass patents to third suppliers.

Intel's Fully Functional Test Chip



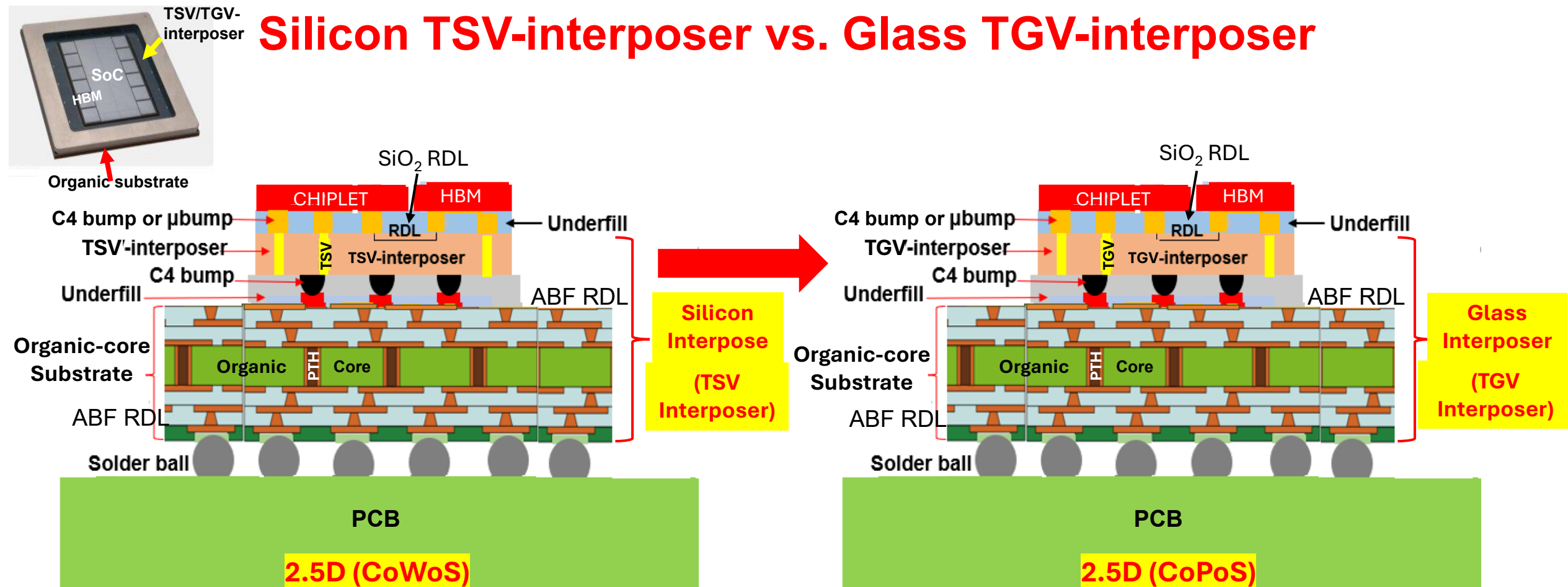
- Altogether, Intel has spent over a **billion dollars** on glass core R&D thus far in Chandler, Arizona.
- The glass core was made very thick – on the order of **1mm** – in order to prove that TGVs would work with such a thick core.
- **3 layers of RDL**, and the **TGVs** have a pitch of **75μm**. Die-to-die bump pitch **< 36μm**.
- Intel claims that glass substrates allow for a much **higher interconnect density** (i.e., **finer pitches**), which is crucial for power delivery and signal routing of next-generation SiPs.
- As part of the company's broader initiative to become a world class contract foundry, Intel will be offering glass core substrates to **IFS (Intel Foundry Services)** customers in due time (**maybe near the end of 2030**).

TSMC's Glass Packaging - CoPoS



During the **TSMC 2025** North America Technology Symposium (April 23), the company announced its **CoPoS** (chip on panel on substrate) technology, which is competing with its **CoWoS** (chip on wafer on substrate) technology.

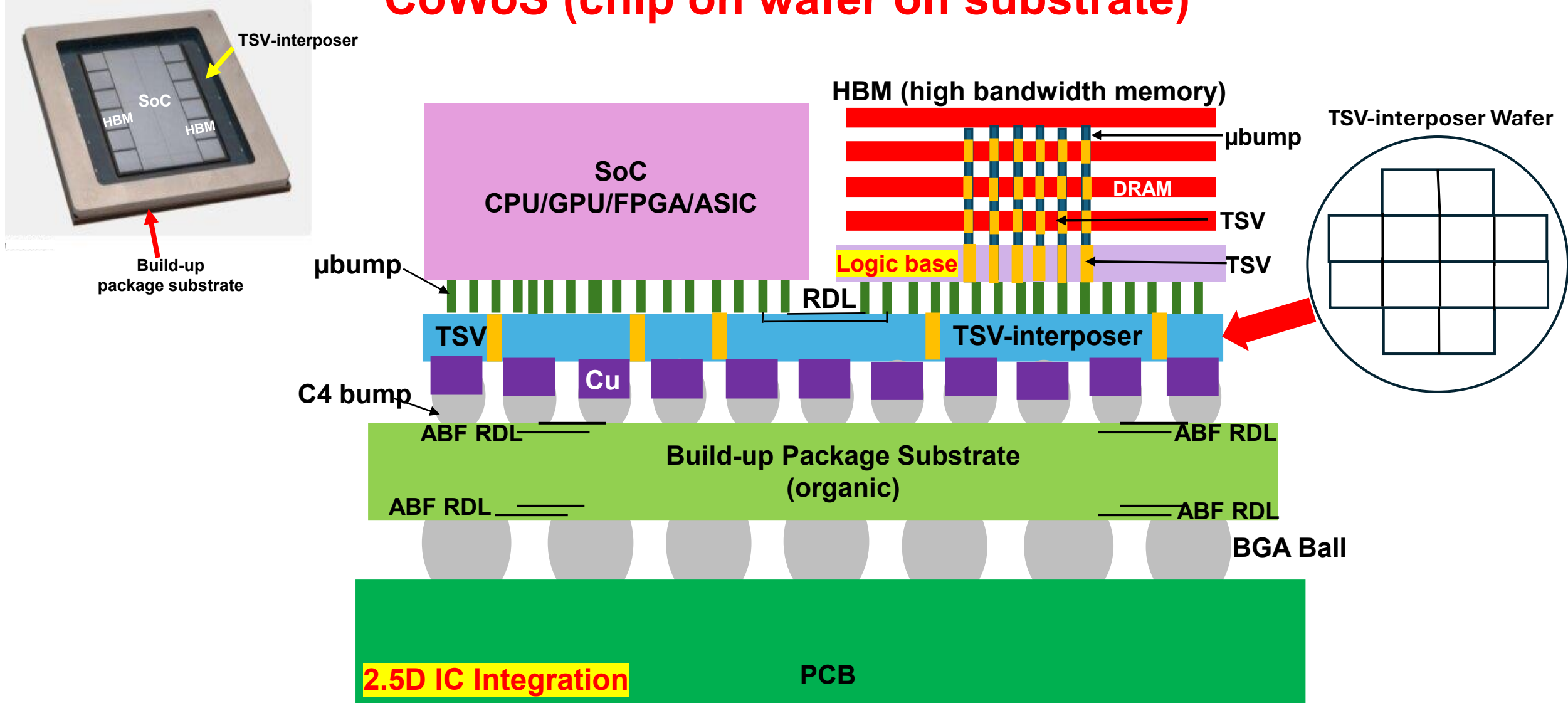
Silicon TSV-interposer vs. Glass TGV-interposer



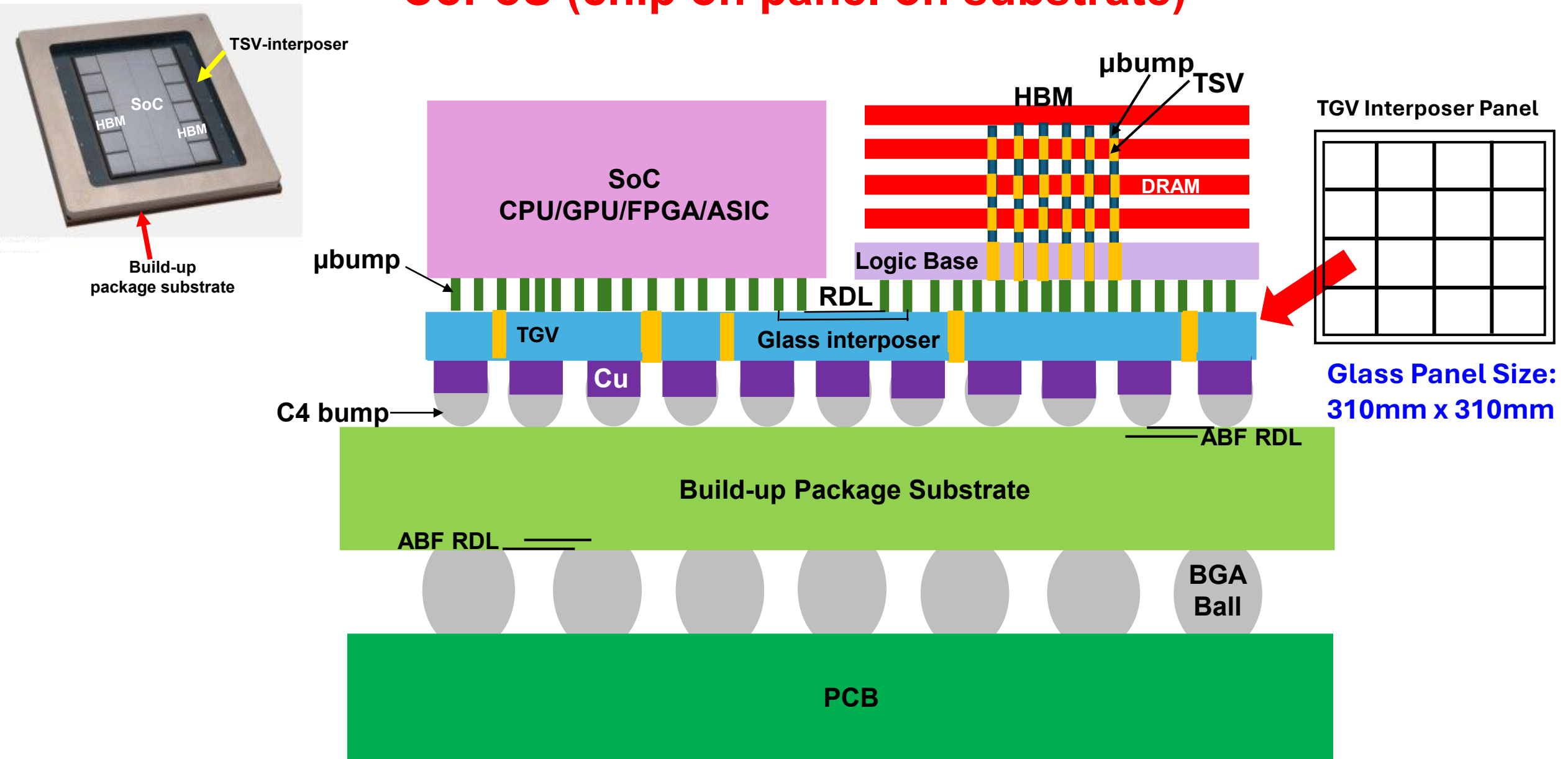
The key advantages of glass TGV-interposer over the silicon TSV-interposer are:

- Better electrical isolation
- Flatter surface
- Lower D_f and D_k
- Better area efficiency
- etc.

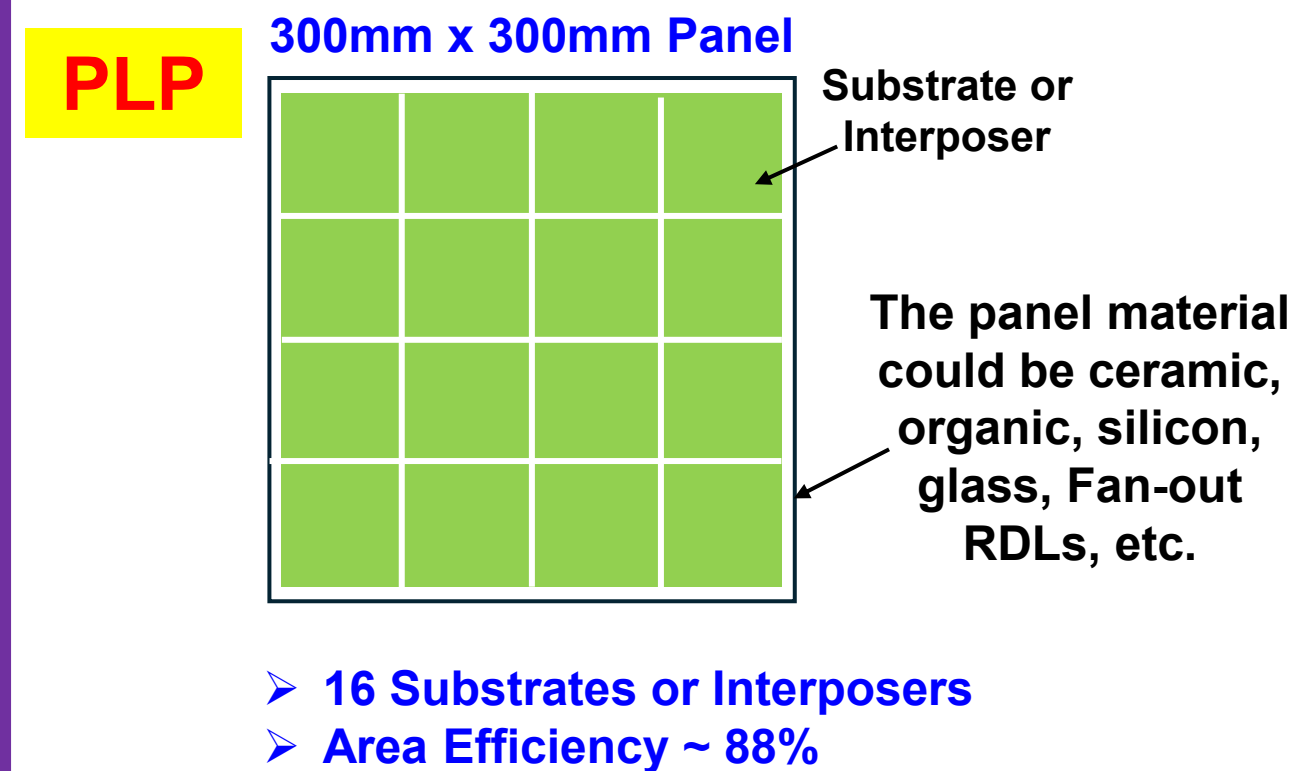
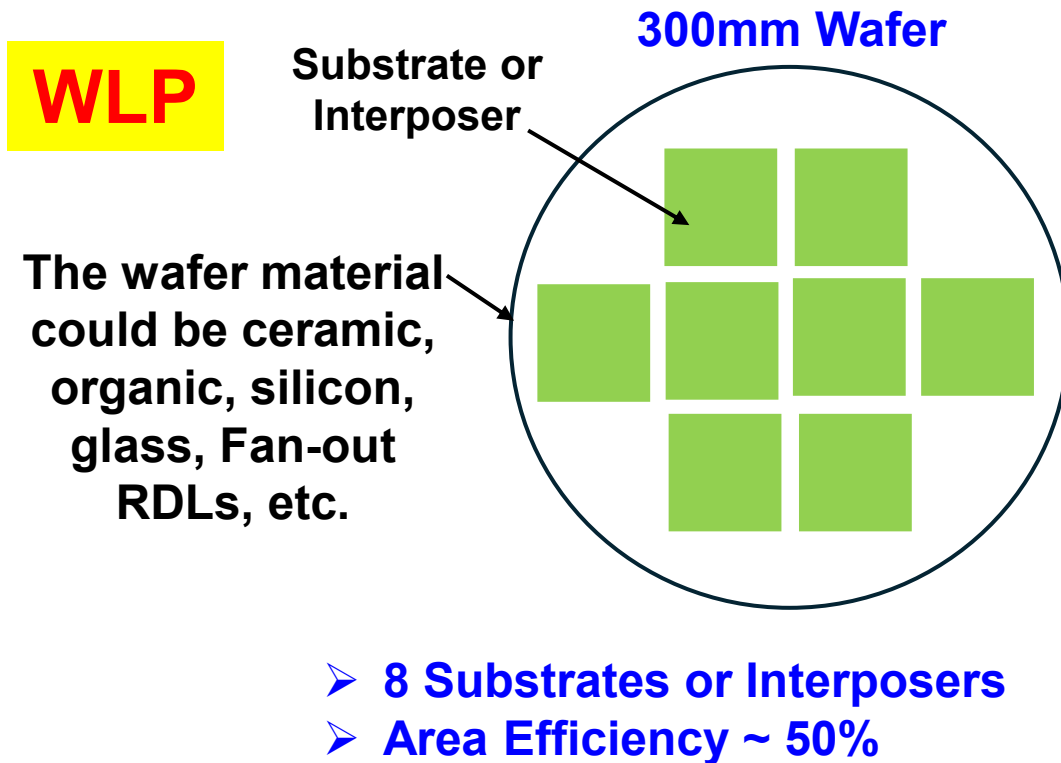
Package of Choice for HPC Driven by AI CoWoS (chip on wafer on substrate)



CoPoS (chip on panel on substrate)

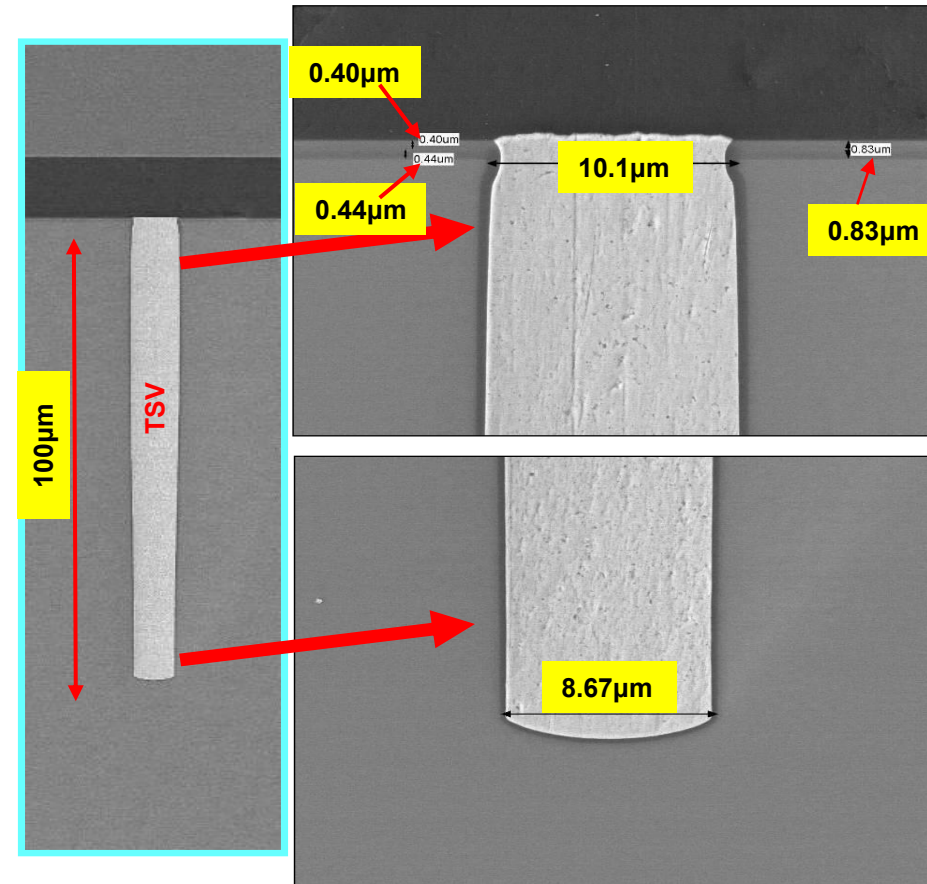
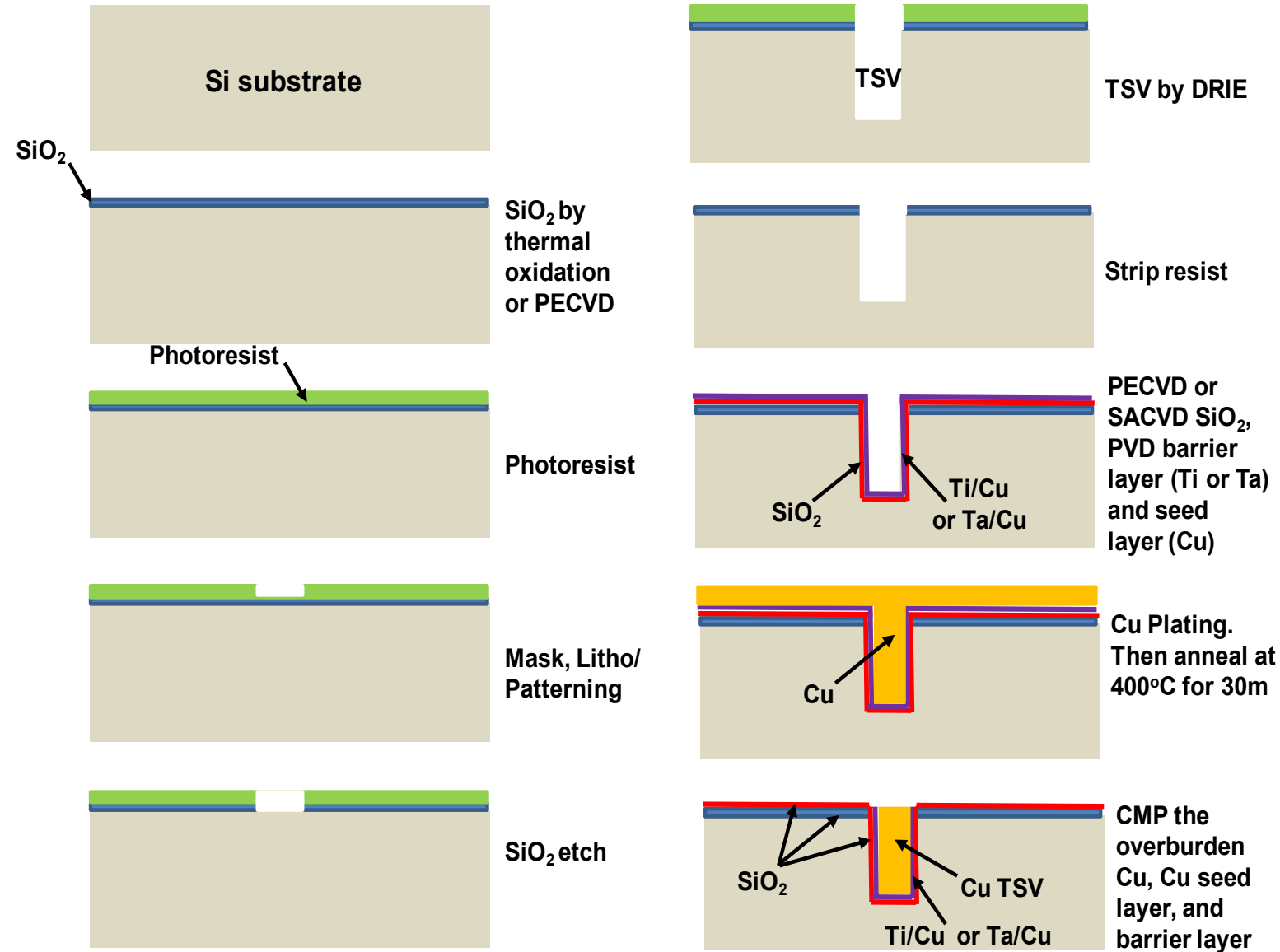


Interposers or Substrates Fabricated on a round wafer (WLP) and on a rectangular panel (PLP) – Area Efficiency.



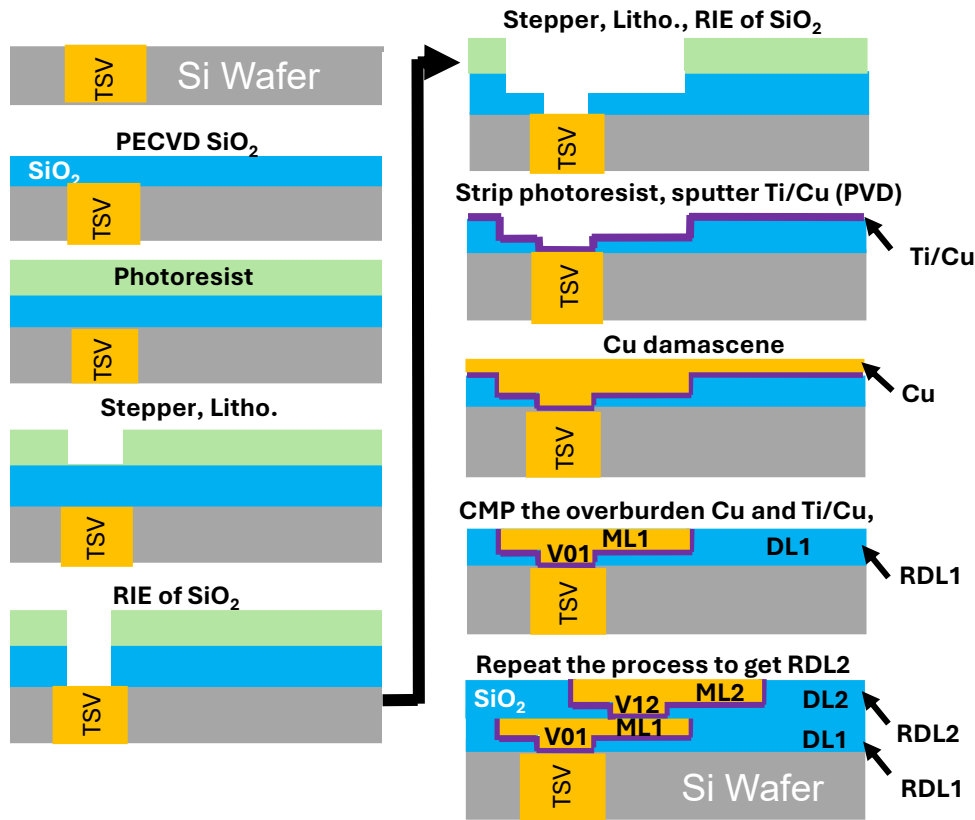
- WLP has been in high volume production for more than 25 years.
- In the past few years PLP has been attracting lots of tractions. The **one and only reason** is PLP has better **area efficiency** (which leads to **lower costs**) compared to WLP.
- The larger the interposer (or substrate) size, the larger the area efficiency of the PLP (which leads to lower cost). This is very important for HPC and data centers in AI era. Because the interposer size is very large, e.g., 2500mm² (8HBM) or 3320mm² (12HBM). There are less than 10 physically possible interposers on a 300mm wafer.

TSV Fabrication (Via-diameter = 5-10 μ m)

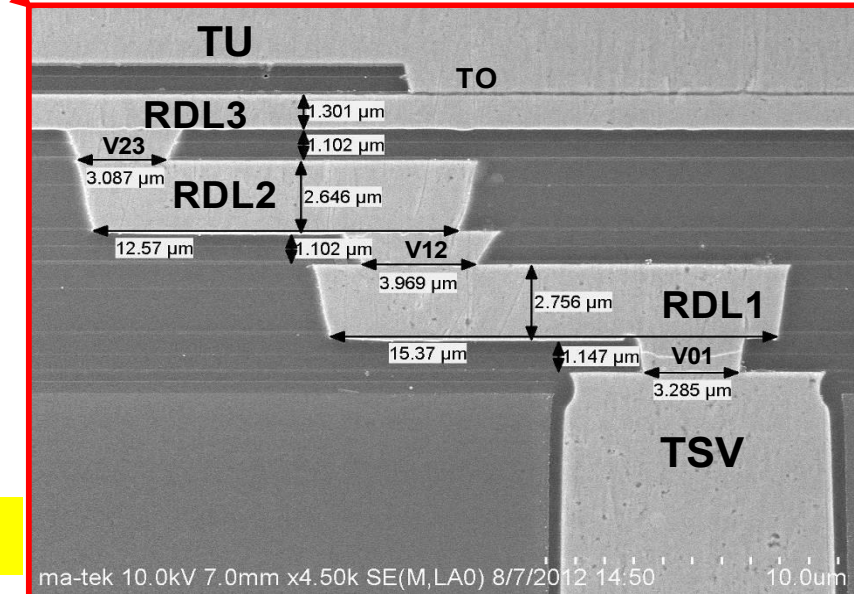
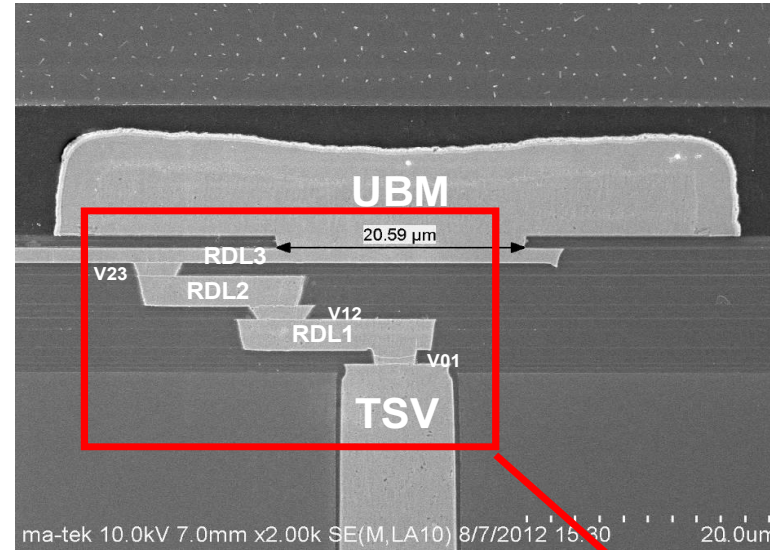


RDL Fabrication (Minimum Pitch = 0.4μm)

PECVD + Dual Cu-Damascenes + CMP



- SiO₂ as dielectric layer (~1μm)
- L/S (< 2μm)
- PECVD
- Stepper
- PVD
- Dual Cu-damascene
- CMP



RDLs minimum pitch = 0.4μm

Status on CoPoS

- **TSMC** has planned to establish its first CoPoS pilot line at **Chiayi** in **2026**, with mass production facilities located at its P4 and P5 plants in AP7, Chiayi.
- Mass production is expected to begin as early as the **first half of 2029**.
- The first wave of equipment supply chains has been largely finalized, with specifications and order volumes confirmed. These are:
 - **International companies:** KLA, TEL, Screen, Applied Materials, and Disco
 - **Taiwanese companies:** Innolux, Sin-Yun, Hung-Soo, Chung Hwa, Chromium, Chih-Sheng, and Da-Long

TSMC license some of Intel's glass patents and work with Ibiden and Innolux to make the TGVs and RDLs on a 310mm x 310mm glass panel.

Status of CoPoS

In May 2026, TSMC issued a strict "gag order" and exclusivity mandate to its advanced packaging supply chain. This restriction targets companies involved in the panel-based CoPoS rather than the current-generation wafer-based CoWoS lines.

Nature of the "Gag Order" & Exclusive Agreements

Non-Disclosure Overhaul: TSMC is forcing Taiwanese materials, equipment, and manufacturing suppliers to sign aggressive legal agreements to ensure proprietary research and development secrets do not leak to rivals.

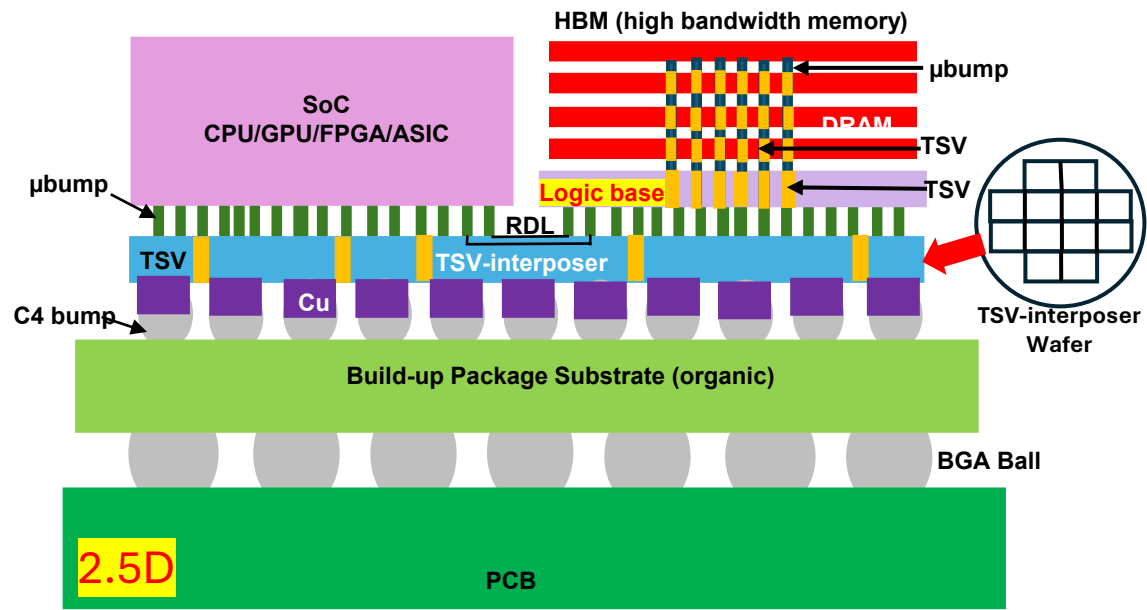
Mandatory Exclusivity: Beyond simple secrecy, the agreements act as a "lock-in" decree, legally barring these supply chain partners from selling the same CoPoS-generation tools or materials to any other semiconductor firms for several years during mass production.

The Strategic Intent

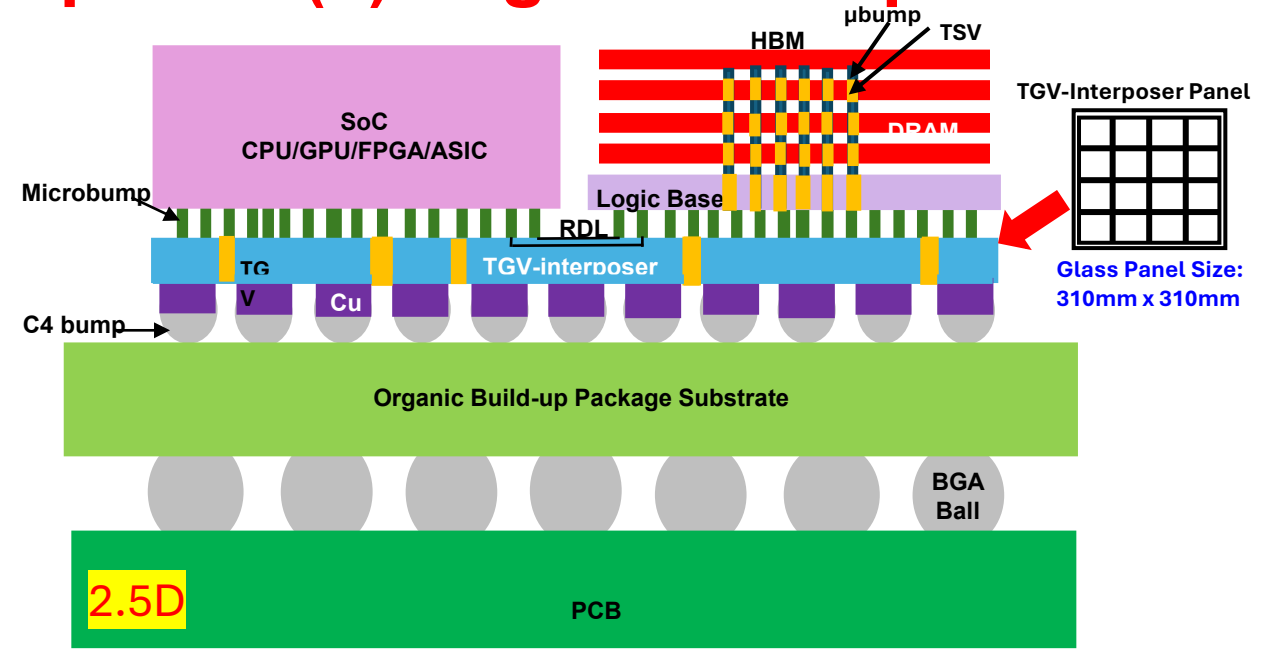
Blocking Intel and Samsung: Intel recently restarted advanced packaging expansions in Malaysia, and Samsung is heavily pitching its alternative solutions. Because some equipment manufacturers holding "TSMC Vendor Codes" began securing spillover orders from Intel, TSMC moved to legally choke off their access to next-gen supply lines.

Defending the Packaging Moat: Next-gen AI chips are hitting size ceilings on traditional silicon interposers. Rival tech like Intel's EMIB has started peeling away some market interest. TSMC intends to build an impenetrable barrier around CoPoS to prevent competitors from capitalizing on its multi-year R&D investments.

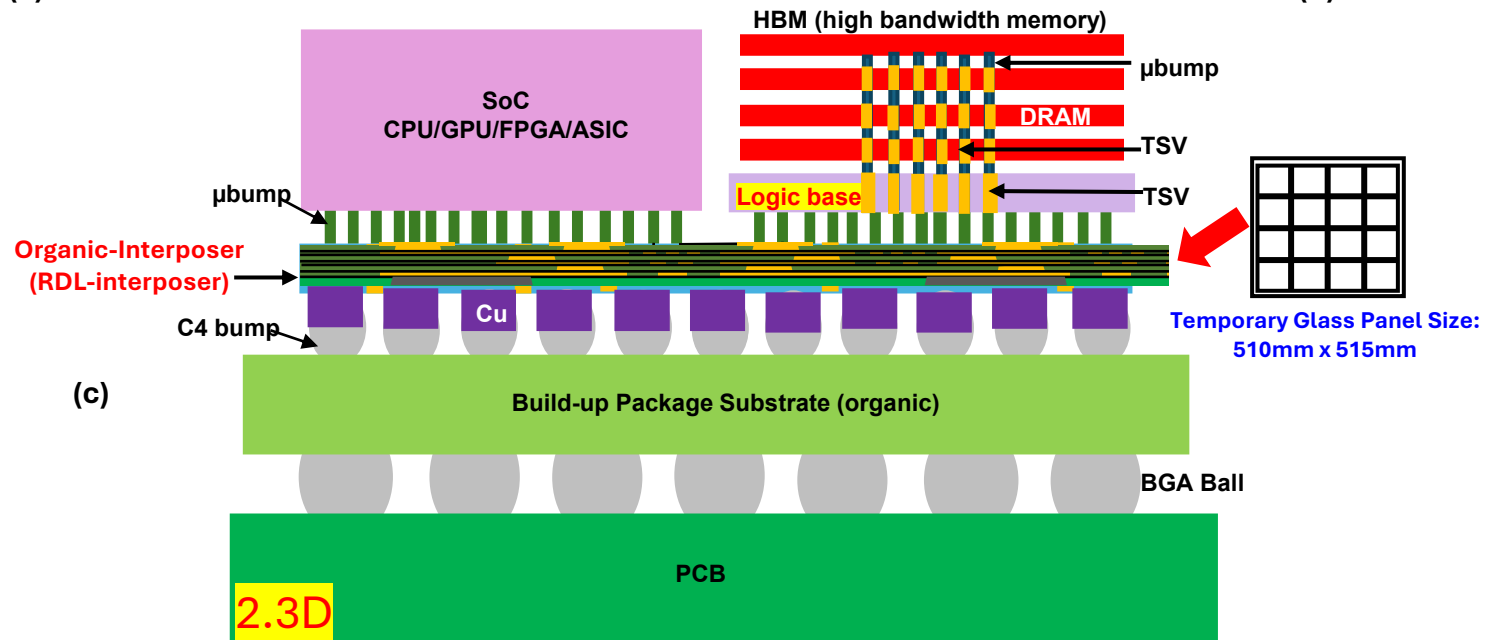
(a) TSV-Interposer. (b) TGV-Interposer. (c) Organic-Interposer.



(a)



(b)



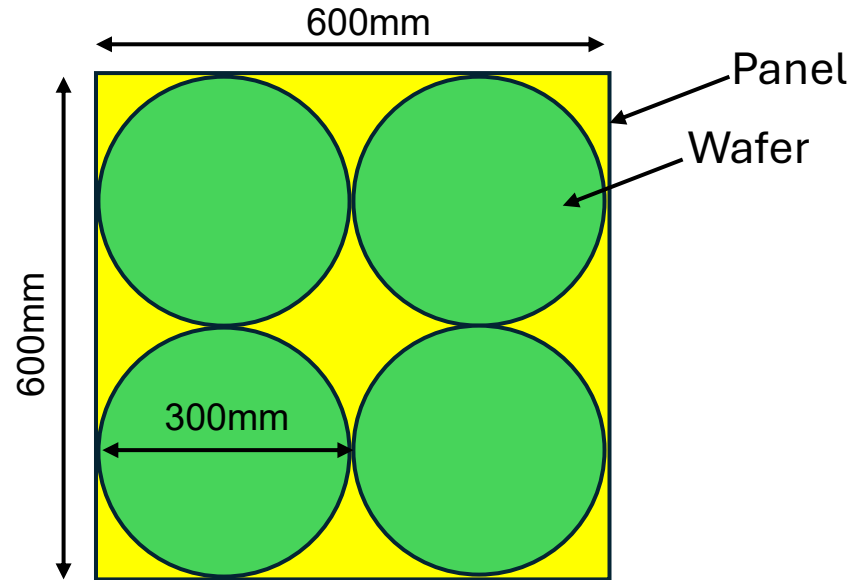
(c)

Comparison between TSV-Interposer, TGV-interposer, and Organic-Interposer

Items	Silicon-Interposer	Glass-Interposer	Organic-Interposer
Material	Crystallin silicon	Silica-based glass	Polymer, ABF, PID
Via	Through-silicon via (TSV)	Through-glass via (TGV)	Stacked/staggered μ vias
RSLs (L/S)	$6\mu\text{m} > \text{L/S} < 1\mu\text{m}$ (.4 μm -pitch _{min})	$8\mu\text{m} > \text{L/S} \leq 2\mu\text{m}$ (.4 μm -pitch _{min})	$2\mu\text{m} \leq \text{L/S} \leq 8\mu\text{m}$
RDLs (Dielectric)	SiO ₂	SiO ₂	Polymer, ABF, PID
RDLs (Metal)	Dual Cu damascene and CMP	Dual Cu damascene and CMP	Cu plating and etching
CTE	Small ($2.8 \times 10^{-6}/^{\circ}\text{C}$)	Medium ($3 - 10 \times 10^{-6}/^{\circ}\text{C}$)	Large ($8 - 18 \times 10^{-6}/^{\circ}\text{C}$)
Thermal Conduct.	Very good ($\sim 150 \text{ W/m}\cdot\text{K}$)	Poor ($< 2 \text{ W/m}\cdot\text{K}$)	Very poor ($< 1 \text{ W/m}\cdot\text{K}$)
D _k and D _f	D _k = 11.8; D _f < 0.008	D _k = 3.2 – 5.5; D _f < 0.0005	D _k = 2.8 – 4.0; D _f < 0.012
Young's M./T. Strength	130 – 190GPa/150 – 300MPa	65 – 90GPa/30 – 150MPa	15 – 30GPa/50 – 250 MPa
Electrical Isolation	Better	Best	Good
Surface Flat./Rough.	Very smooth	Very flat	Unstable and Rough
Size Constraints	Wafer sizes	Large panel sizes	Larger panel sizes
Density	Highest	Higher	High
CPO Si/G Photonics	Best	~Best	NA
Maturity	Mature	Not yet, but working on it	Very mature
Relative Cost	Highest	Higher $\rightarrow$ Highest	High

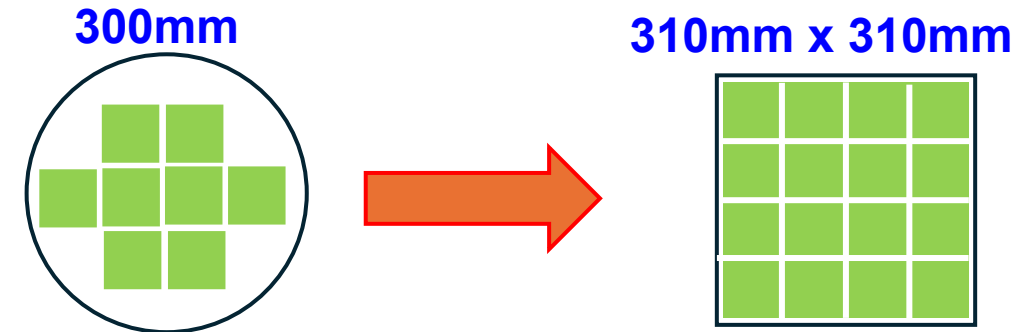
Standardization of Panel size for HPC and Data Centers in AI era

600mm x 600mm Panel vs. 310mm x 310mm Panel



Disadvantages

- More expensive equipment
- Larger floor space
- Longer Pick and Place time
- Larger warpage
- Higher yield loss
- Longer time to clean the equipment
- The large panel must be cut into smaller panels for solder ball mounted
- Etc.



- 8 Interposers
- Area Efficiency ~ 50%

- 16 Interposers
- Area Efficiency ~ 88%

Advantages

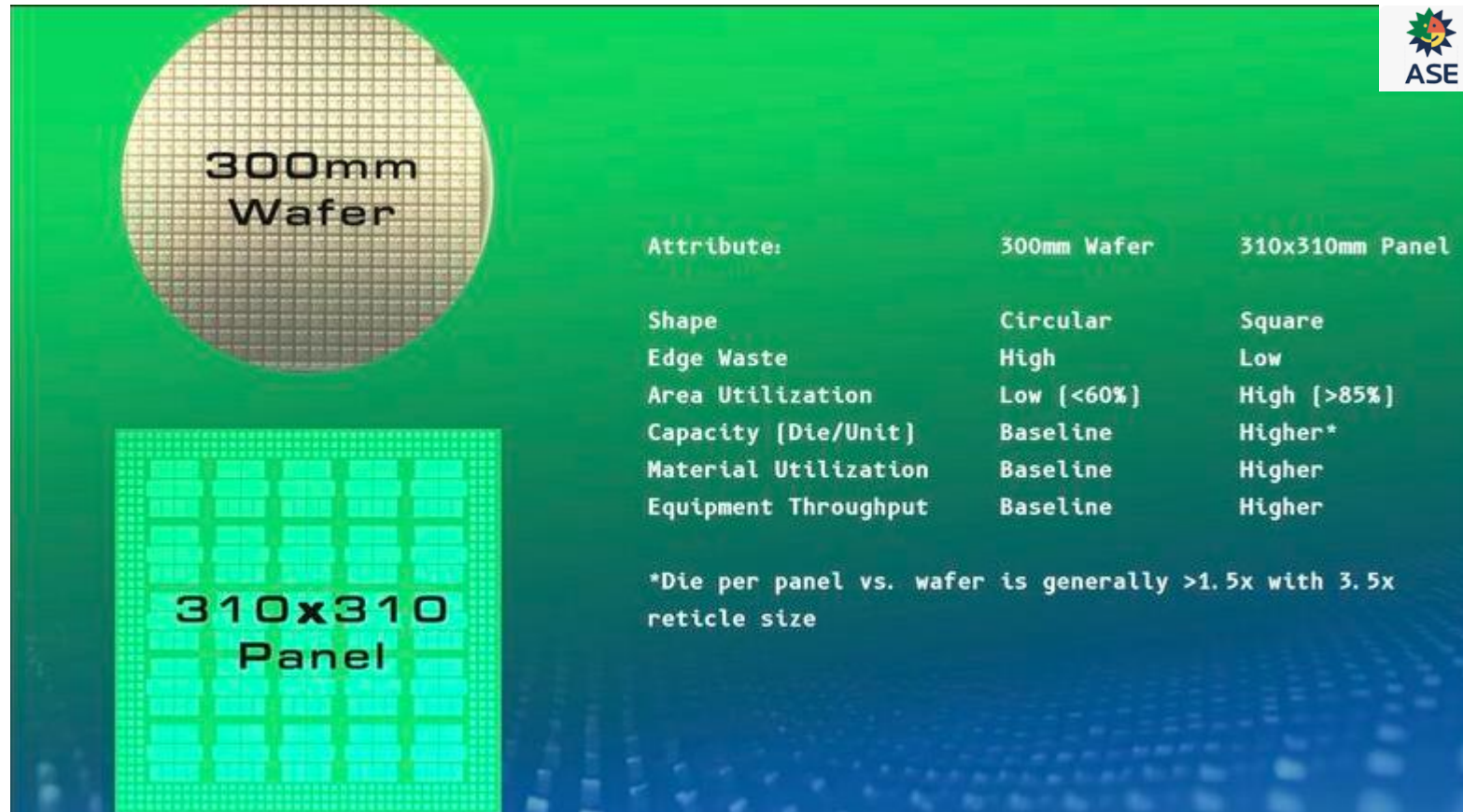
- Higher area efficiency compared with 300mm-wafer
- Similar process control as with 300mm-wafer
- Similar yield loss as with 300mm-wafer
- All the experience from 300mm-wafer can be adopted to 310mmx310mm panel

Cost! Cost! Cost!

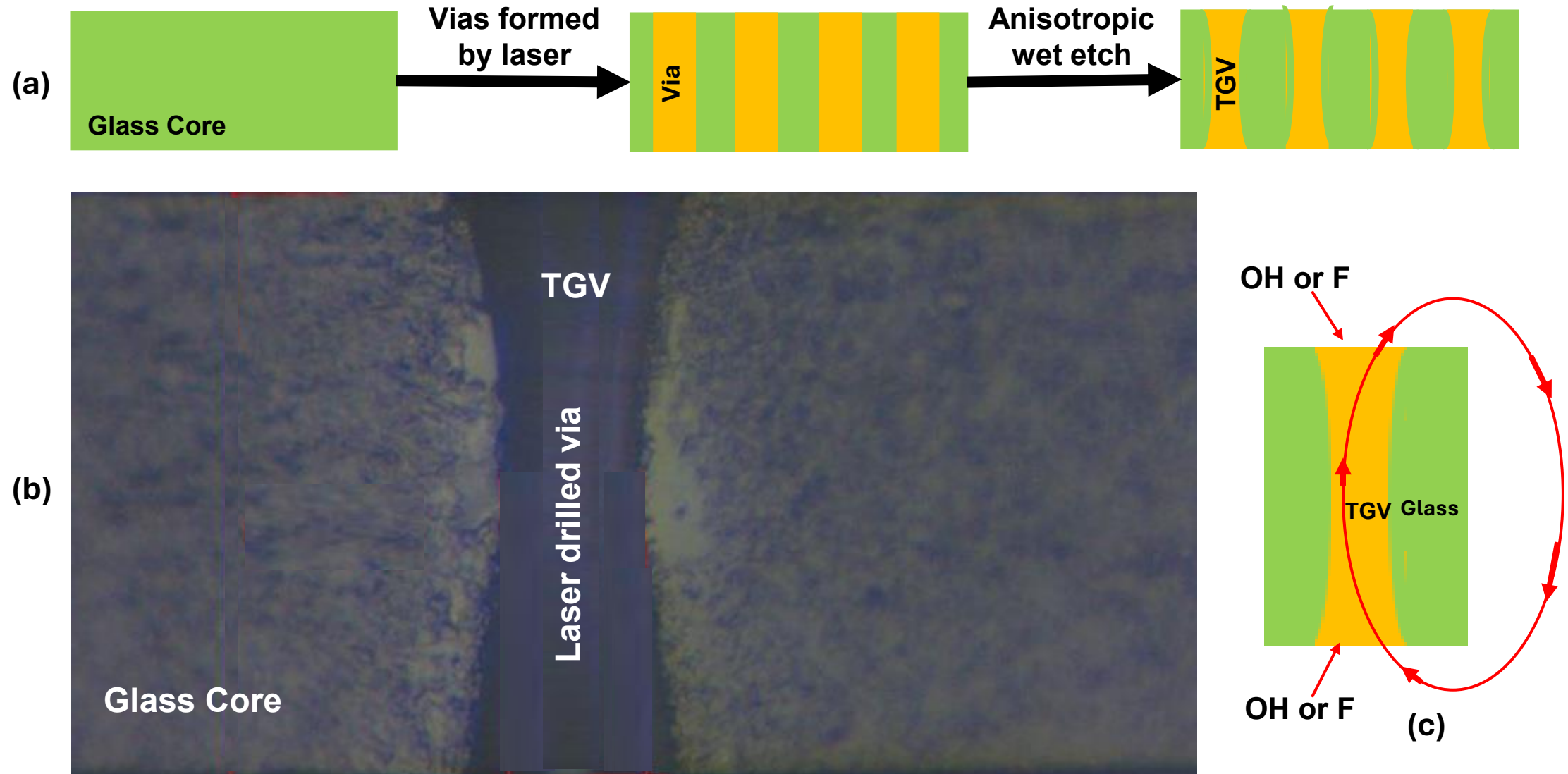
Status of Panel Size

- On April 23, 2025, **TSMC** announced they'll use **310mm x 310mm** panel size for their CoPoS.
- In March 2026, while **ASE** originally planned for a 600mm x 600mm panel line, it scaled back to 310mm x 310mm to align with TSMC's panel size. ASE aims to have a fully automated 310mm x 310mm production line operational for pilot production by the end of 2026.
- On May 26, 2026, **ASE** formally announced the 310mm x 310mm panel size by the CEO of ASE at ECTC2026. **Most of the successful experiences from 300mm wafer can be transferred to 310mm x 310mm.**
- With the #1 foundry (TSMC) and the #1 OSAT (ASE) now aligned, the market is poised to shift from experimentation to **volume production**.
- Standardizing this panel size 310mm x 310mm is expected to help the entire semiconductor ecosystem scale AI chip packaging **more reliably by providing a common platform for testing and manufacturing**.
- I do think that 310mm × 310 mm format strikes a **critical balance**: **it is large enough to capture the area efficiency (cost) and small enough to maintain the processing control (yield). All the experience from 300mm-wafer can be adapted to 310mm x 310mm panel.**

ASE's 310mm x 310mm

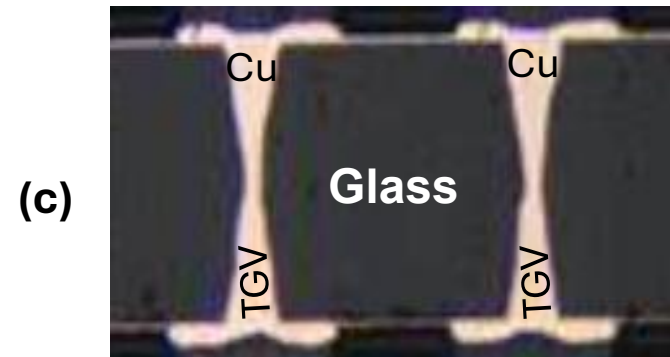
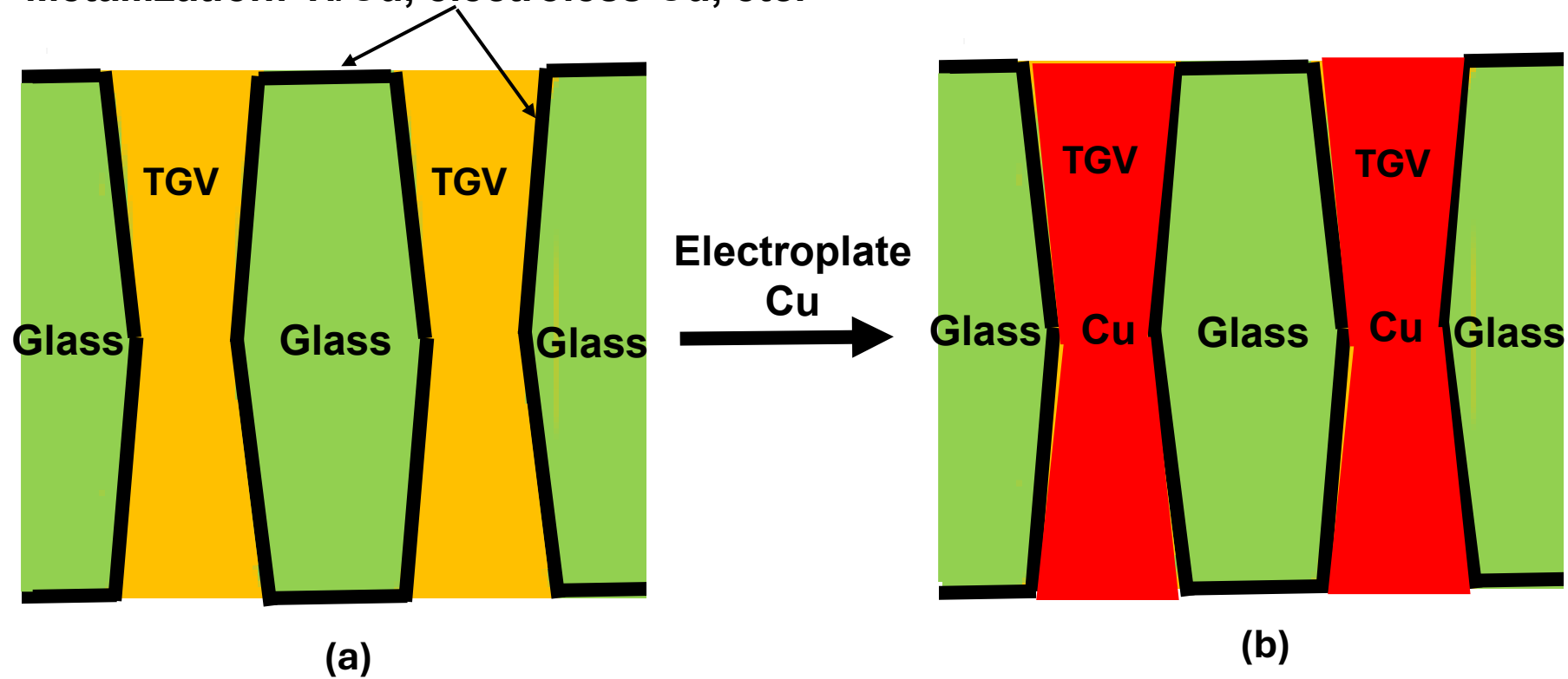


Laser Induced Deep Etching (LIDE). (a) TGV Process flow. (b) SEM image of a TGV. (c) Etch solution mechanism

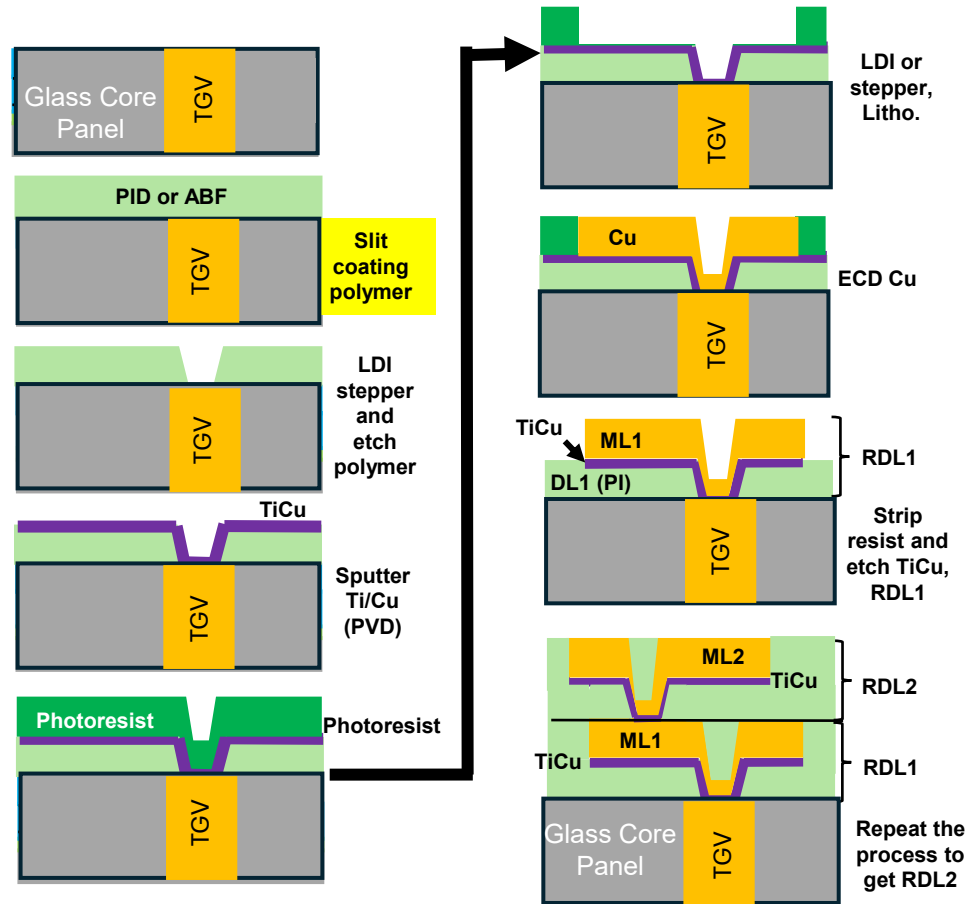


(a) TGV sidewall metallization. (b) Cu plating. (c) An image of Cr-filled TGV

Metallization: Ti/Cu, electroless Cu, etc.

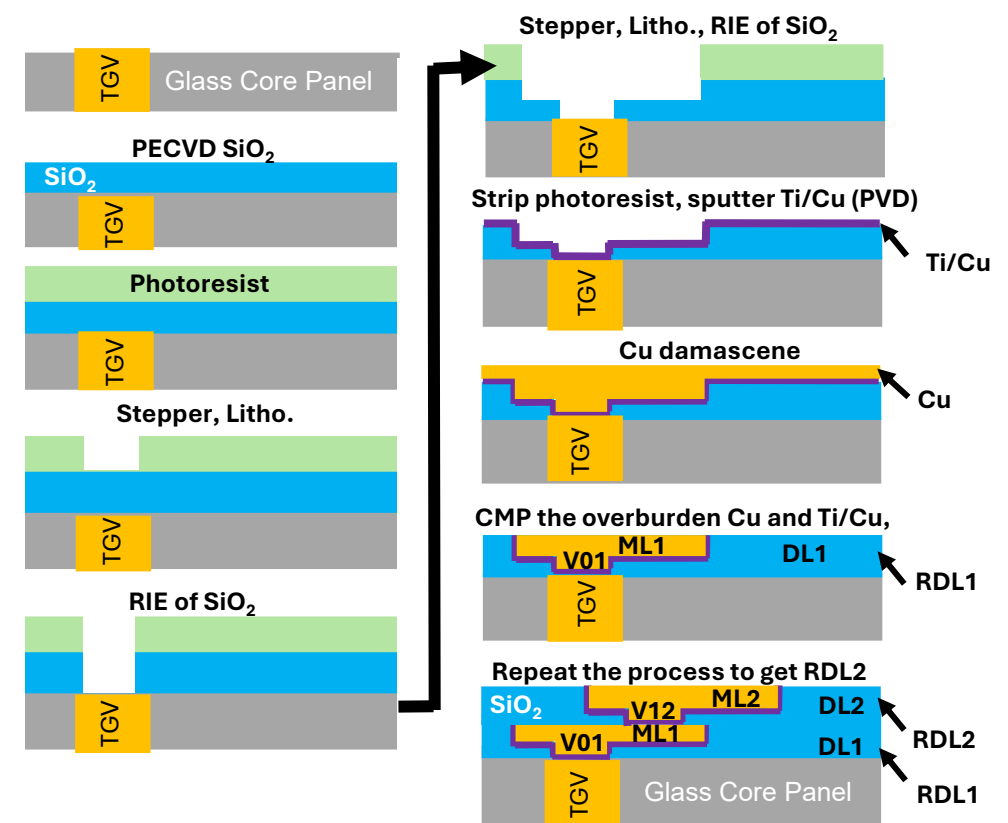


TGV RDL Process Flow. (a) $L/S \geq 2\mu\text{m}$. (b) $L/S < 2\mu\text{m}$.



- PID or ABF as dielectric layer ($\geq 5\mu\text{m}$)
- $L/S (\geq 2\mu\text{m})$
- LDI or Stepper
- PVD
- ECD Cu

(a)

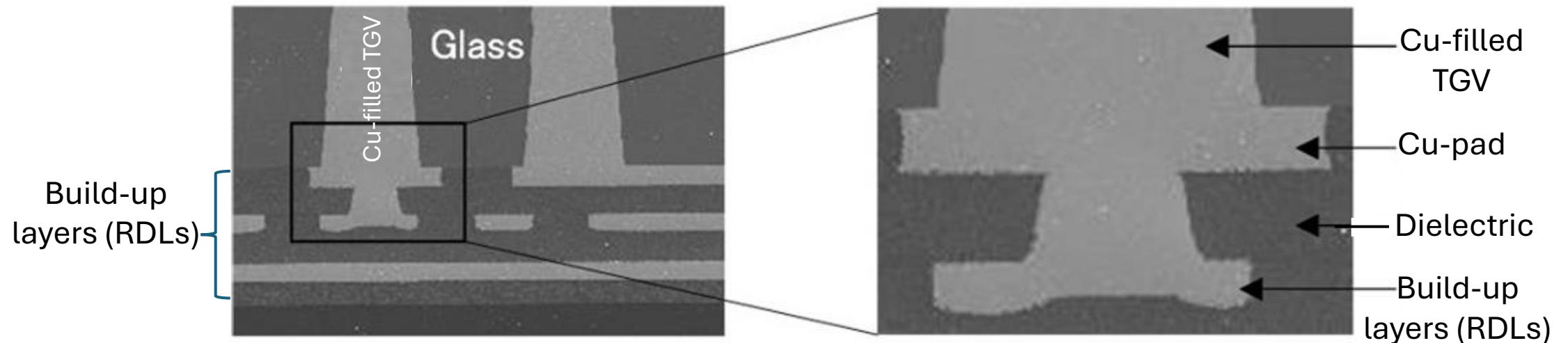
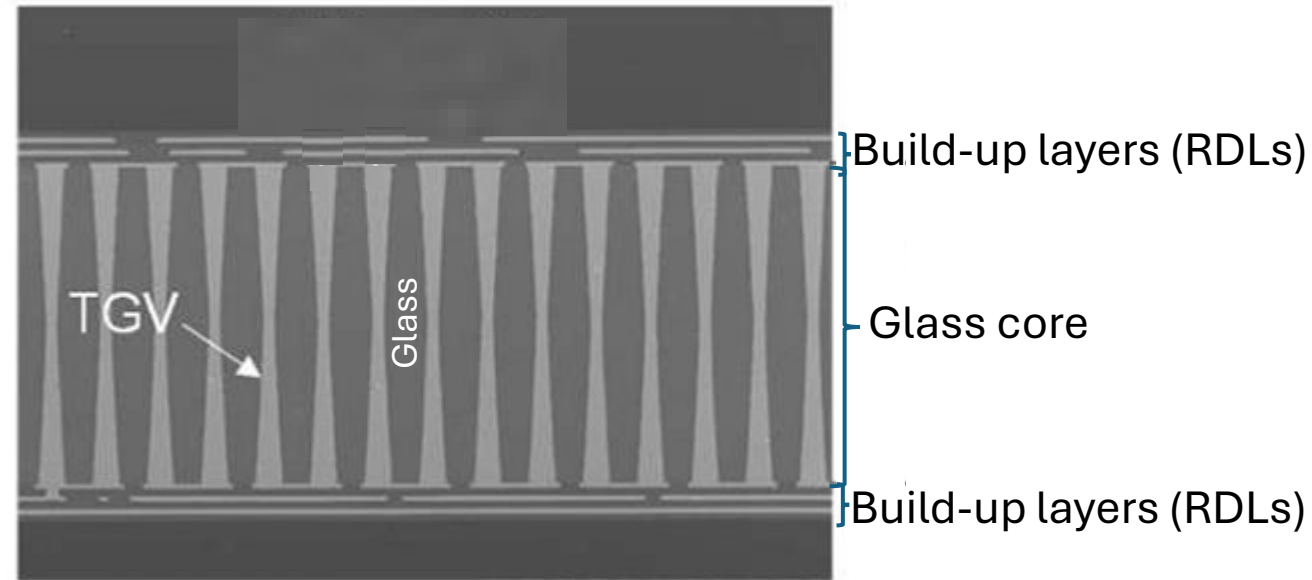


- SiO_2 as dielectric layer ($\sim 1\mu\text{m}$)
- $L/S (< 2\mu\text{m})$
- PECVD
- Stepper
- PVD
- Dual Cu-damascene
- CMP

64nm Process

(b)

SEM image of glass-core substrate with TGV and RDLs ($L/S \geq 2\mu\text{m}$)



**RDLs ($L/S = 0.2\mu\text{m}_{\text{min}}$) on Top of Glass
TGV-Interposer **have not** been published
in the literature yet!**

Process Compression between the TSV and TGV

Items	Through-Silicon Via (TSV)	Through-Glass Via (TGV)
Base Material	Silicon wafer	Alkali-free flat glass or fused silica
Via Formation	Deep Reactive-Ion Etching (DRIE)	Laser drilling / Laser Induced Deep Etching (LIDE)
Chemical Post-Processing	Gas-phase plasma etch chemistry	Anisotropic wet chemical etching (HF or NaOH)
Insulation Layer	SiO ₂ (PECVD)	None - Glass is natively non-conductive
Metallization and Filling	Ti or Ta (PVD barrier layer)	Direct seed layer, e.g., Ti/Cu or electroless Cu
Sidewall Profile	Straight, vertical sidewalls.	Distinct taper angle (hourglass shape)
Via Filling	Electroplated with Cu	Electroplated with Cu
Maturity	Very	Not yet

RDL Process Compression between the TSV-interposer and TGV-interposer

**There should not be significant
differences!**

**May be the RDLs on top of the glass
TGV-interposer is a **little easier** because of its
superior flatness!**

Summary

In general, the **challenges** of glass packaging are:

- Crack-free TGV formation
- Fine L/S = $0.2\mu\text{m}_{\text{min}}$ RDLs fabrication in AI era
- RDLs thickness uniformity
- Panel warpage for fabricating the RDLs
- Handling
- Testing
- Integration within existing manufacturing environments
- Immutable technology
- etc.

**So far, not many people talk
about the Reliability because of
the glass substrate!!!**

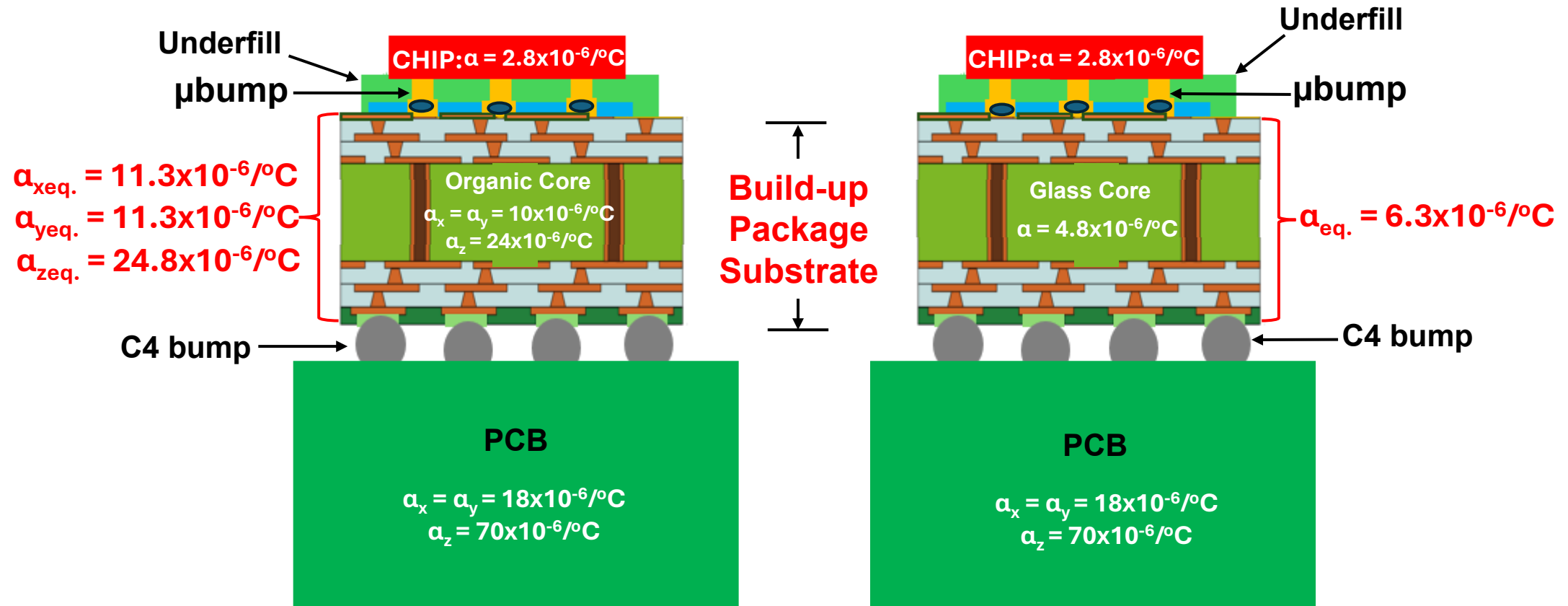
One of the reliabilities is the

**Solder joints on PCB reliability
because of the glass substrate.**

Flip Chip on Glass-core Substrate with μ bumps

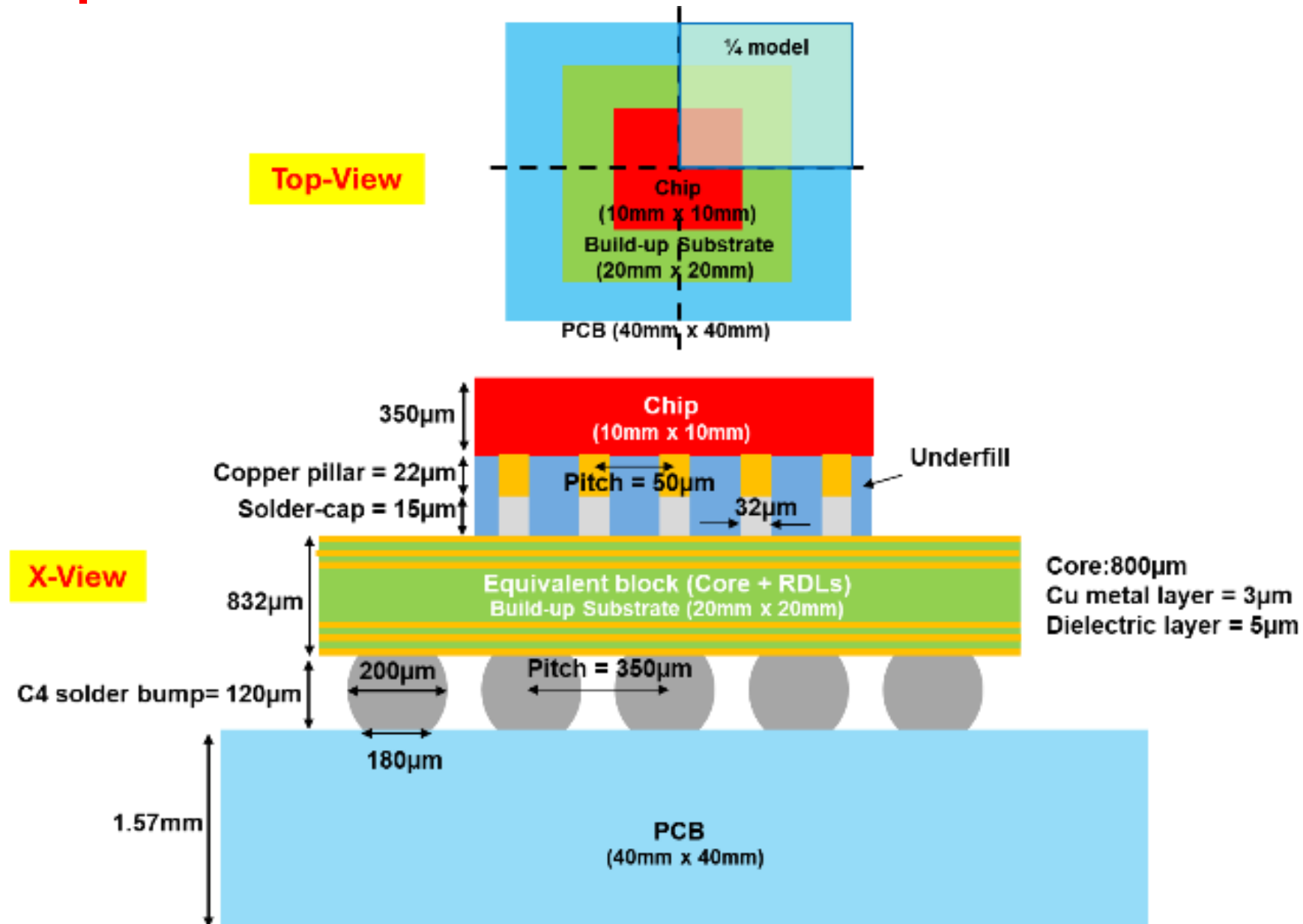
(Effects of glass-core substrate on Solder Joint Reliability)

Flip Chip (a) on organic-core substrate, and (b) on glass-core substrate



The chip dimensions are 10mm x 10mm x 350 μm . The C4 bump is SAC. The μbump is Cu-pillar + Sn0.7Cu. Both solders obeyed Anand model. Build-up layers (RDLs) = 2 layers on top and 2 layers at the bottom. The thickness of each layer is 8 μm (Cu metal layer = 3 μm and dielectric layer = 5 μm). The thickness of the glass core and organic core is 800 μm . The thickness of the PCB = 1.57mm.

Top-view and Cross-section view of the structure



Anand Viscoplasticity Constitutive Equation

All the solders, **Sn3Ag0.5Cu** and **Sn0.7Cu**, obey the **Anand viscoplasticity constitute equation**. The Anand flow equation which governs the inelastic strain ε has the following form [1-6]:

$$\frac{d\varepsilon}{dt} = A \left[\sinh \left(\frac{\xi \sigma}{s} \right) \right]^{1/m} \exp \left(-\frac{Q}{RT} \right)$$

where $d\varepsilon/dt$ is the inelastic strain rate, A is the pre-exponential factor, Q is the activation energy, R is the universal gas constant ($8.314 \text{ J}\cdot\text{K}^{-1}\cdot\text{mol}^{-1}$), T is the absolute temperature (Kelvin), ξ is the multiplier of stress, σ is the equivalent stress, m is strain rate sensitivity. The evolution equation which defines an internal variable s of the model, and its saturation value is:

$$\frac{ds}{dt} = \left\{ h_0 (|B|)^a \frac{B}{|B|} \right\} \frac{d\varepsilon}{dt}$$

where

$$B = 1 - \frac{s}{s^*}$$

and

$$s^* = \hat{s} \left[\frac{d\varepsilon_p/dt}{A} \exp \left(\frac{Q}{RT} \right) \right]^n$$

where h_0 is the hardening/softening constant, a is the strain rate sensitivity of hardening/softening. The quantity s^* represents a saturation value of deformation resistances. $\hat{s}$ is a coefficient, and n is the strain rate sensitivity for the saturation value of deformation resistance, respectively. The evolution equation has an extra initial condition of $s(0) = s_0$, where s_0 is the initial value of s at initial time $t = 0$. The loading-unloading criterion and viscoplastic flow occurs for yield criterion or an any non-zero stress. The Anand model does not have an explicit criterion or a loading-unloading criterion and viscoplastic flow occurs for any non-zero stress.

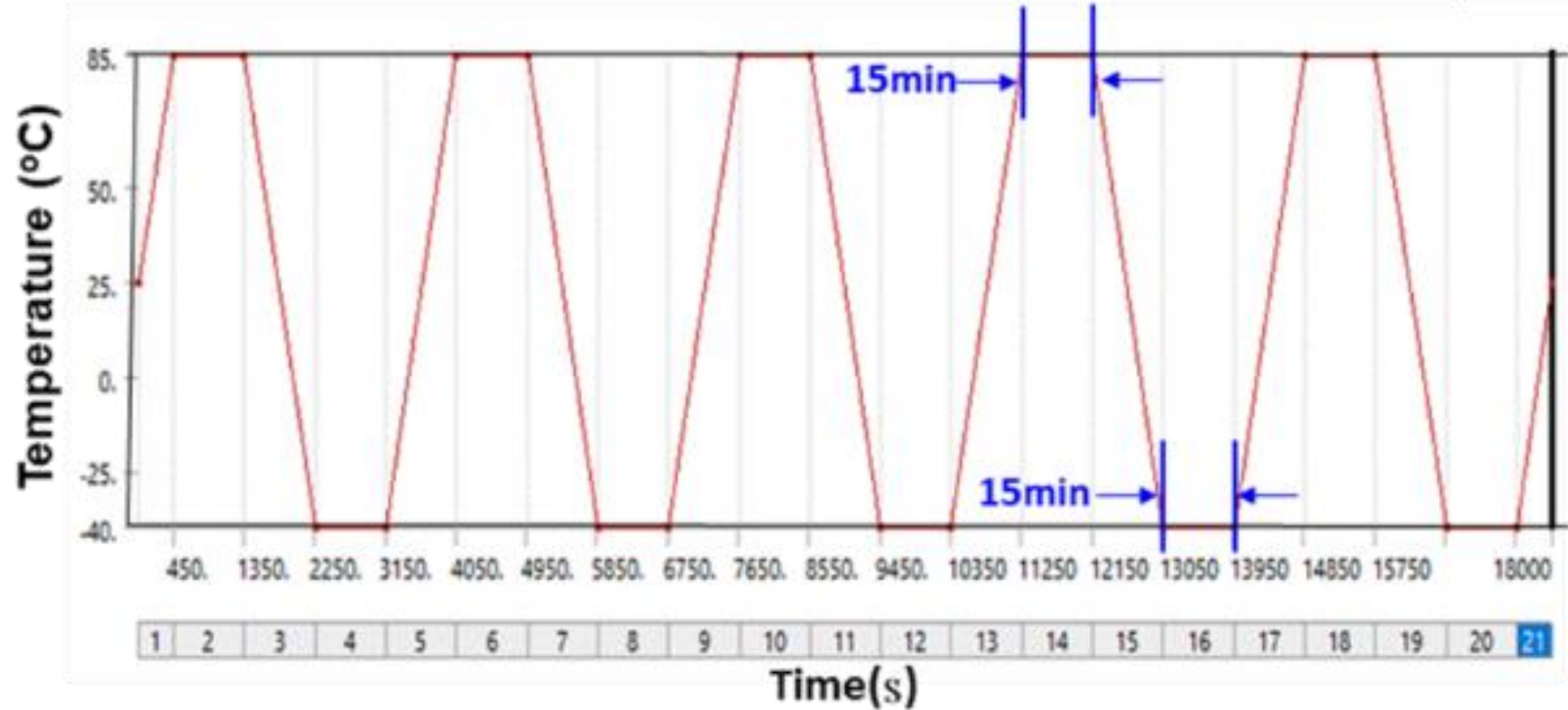
Anand parameters for Sn3Ag0.5Cu (SAC305) and Sn0.7Cu

Anand Model		
Parameters	SAC305	Sn0.7Cu
s_0 (Pa)	18.07×10^6	33.8×10^6
Q/R (K)	9096	5276
A (s ⁻¹)	3484	9875
ξ	4	2
m	0.2	0.176
h_0 (Pa)	1.44×10^{11}	61987.3×10^6
$\hat{s}$ (Pa)	26.4×10^6	65.2×10^6
n	0.01	0.003
a	1.9	1.03

Material properties for simulations

Materials	Young’s modulus (GPa)	Poisson’s ratio	CTE (10x ⁻⁶ /°C)
Silicon	131	0.278	2.8
μbump (Sn0.7Cu)	30	0.3	22
C4 bump (SAC305)	49 - 0.07T(°C)	0.3	21 + 0.017T(°C)
PCB	E _x = E _y = 22; E _z = 10	0.28	α _x = α _y = 18; α _z = 70
Underfill	4.5	0.35	50
RDL (Dielectric)	2.0	0.3	60
RDL (Copper)	121	0.34	16.3
Glass core	72	0.29	4.8
Organic core	24	0.3	α _x = α _y = 10; α _z = 24
Equivalent block (Glass core + RDLs)	71	0.29	6.3
Equivalent block (Organic core + RDLs)	25	0.3	α _x = α _y = 11.3; α _z = 24.8

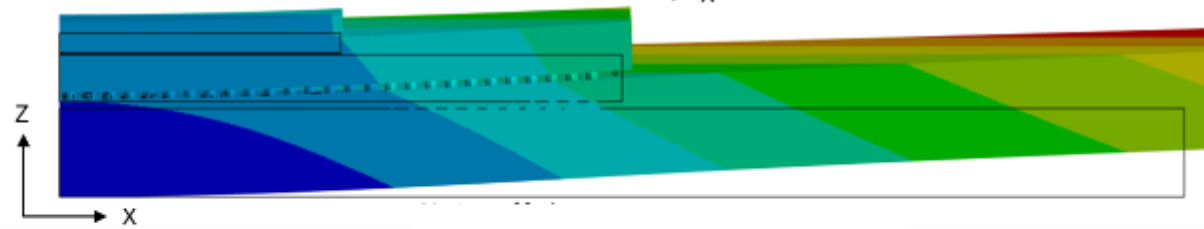
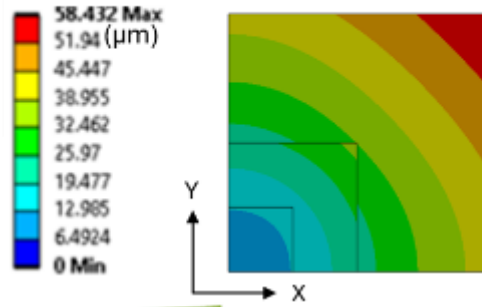
Temperature boundary condition



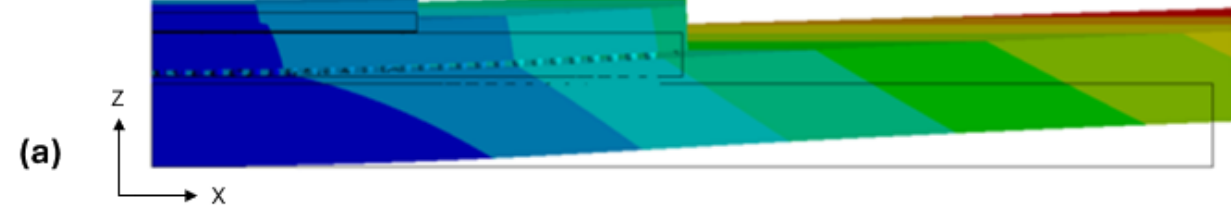
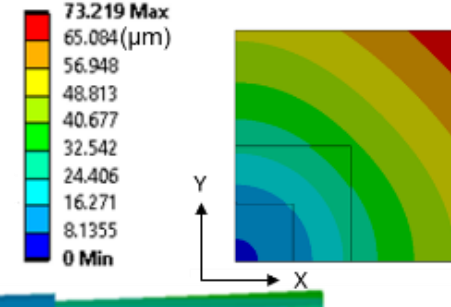
Deformation of structure with organic core substrate

Deformation of structure with glass core substrate

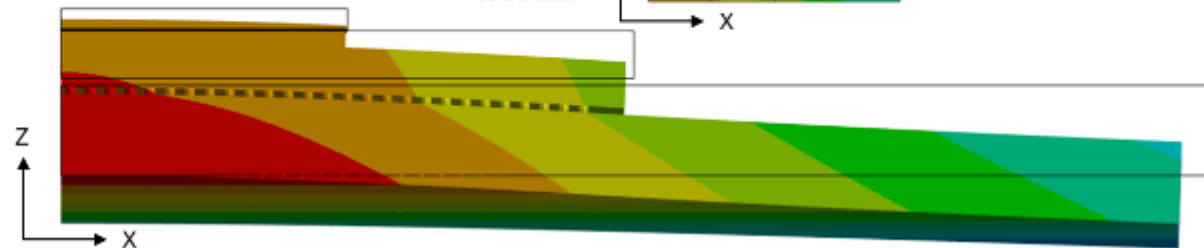
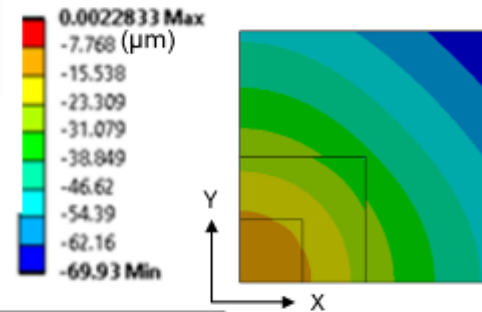
85°C (450s)



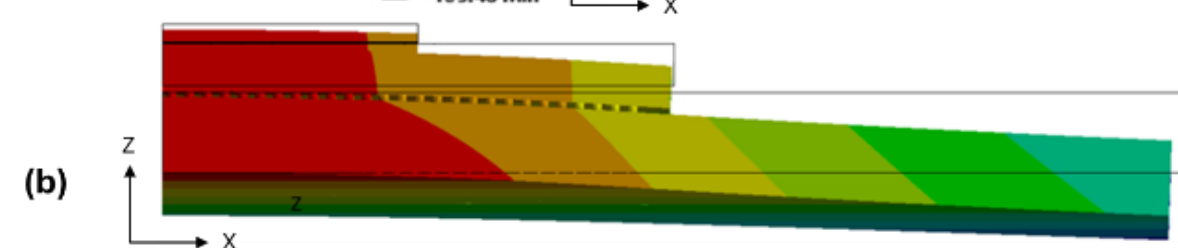
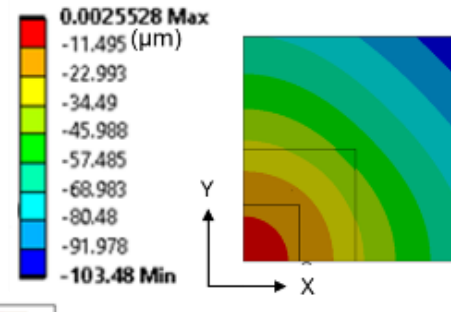
85°C (450s)



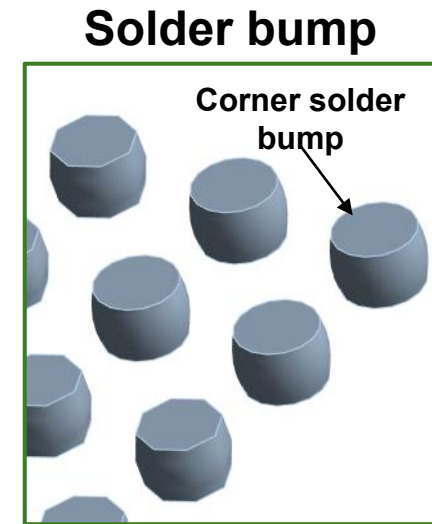
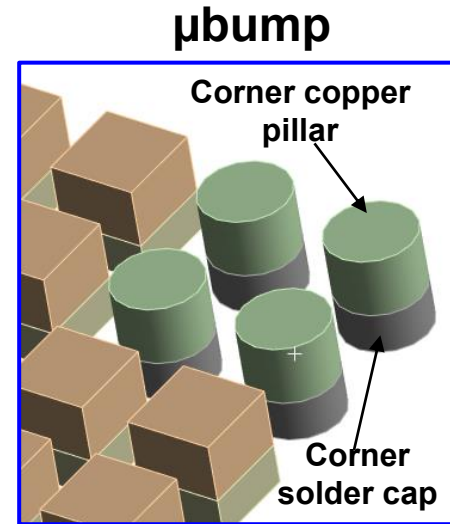
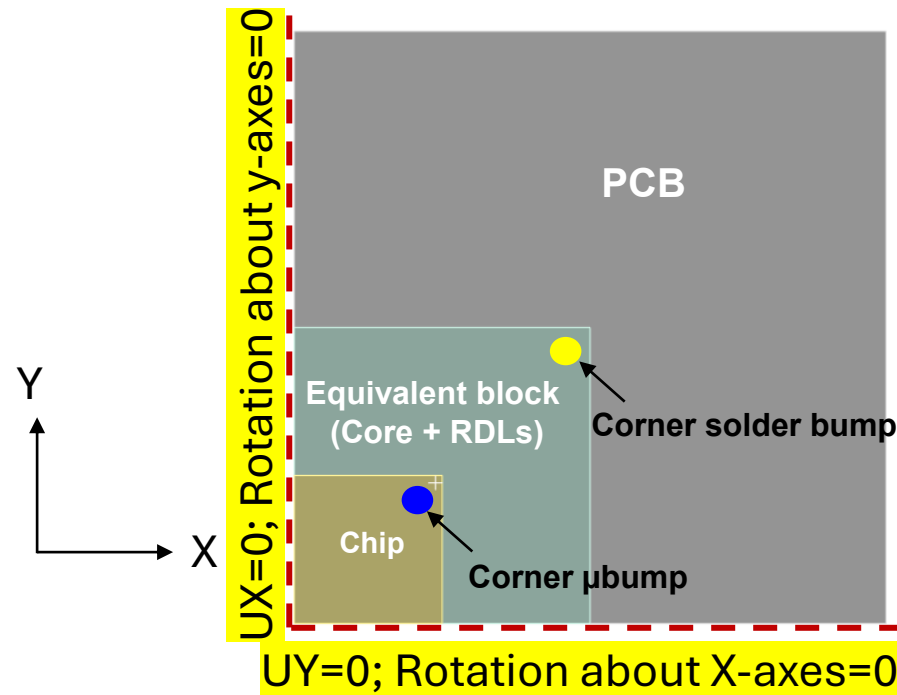
-40°C (2250s)



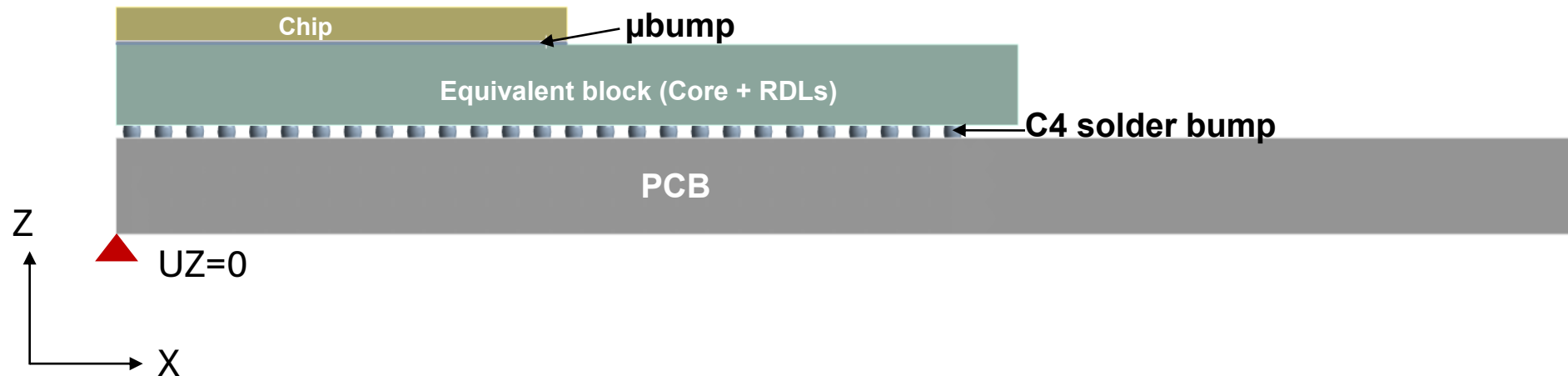
-40°C (2250s)



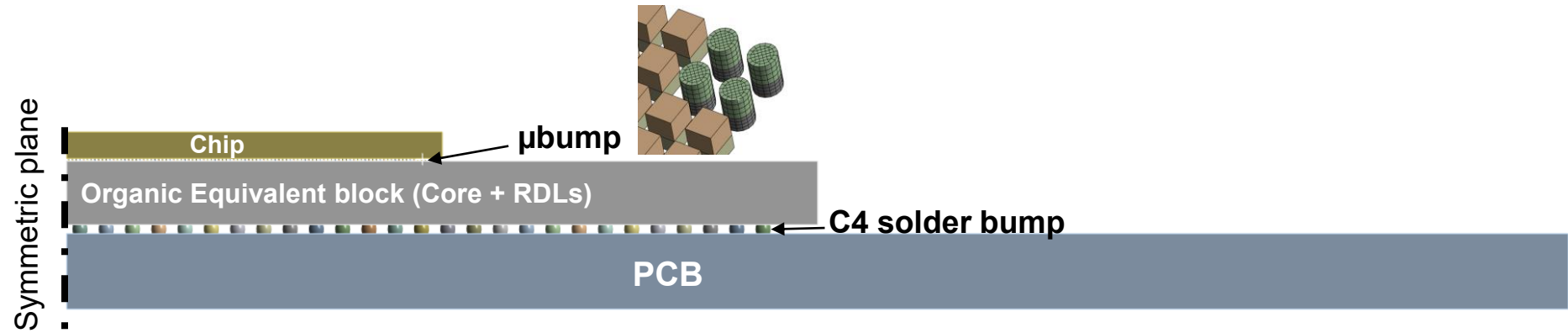
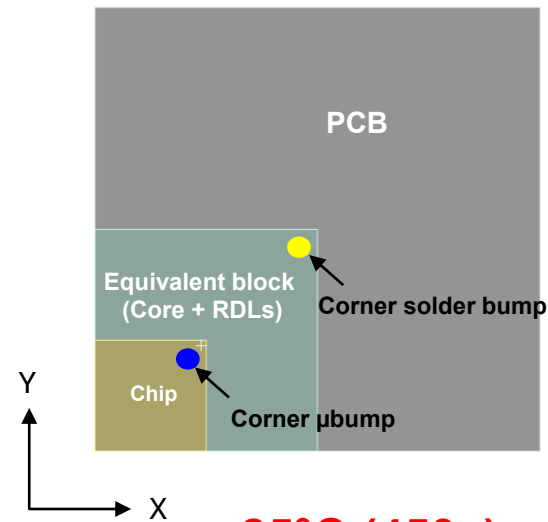
Finite element modeling of the structure



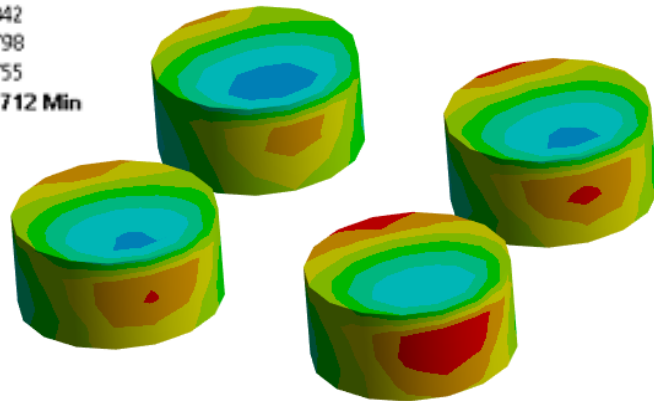
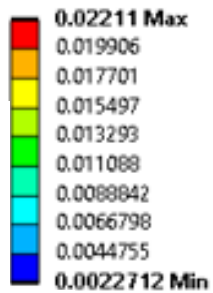
- **μ bump (quarter model)**
 - Pitch=50 μ m
 - Number=9216(96x96 array)
- **C4 solder bump (quarter model)**
 - Pitch=350 μ m
 - Number=729(27x27 array)



Maximum accumulated inelastic strain in corner μ bump of structure with organic core substrate

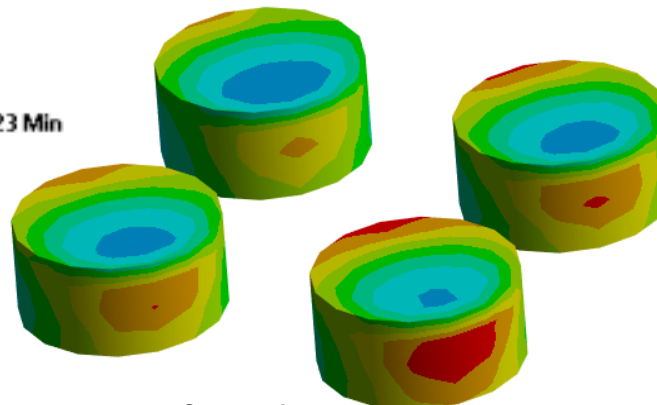
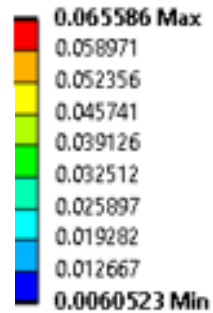


85°C (450s)



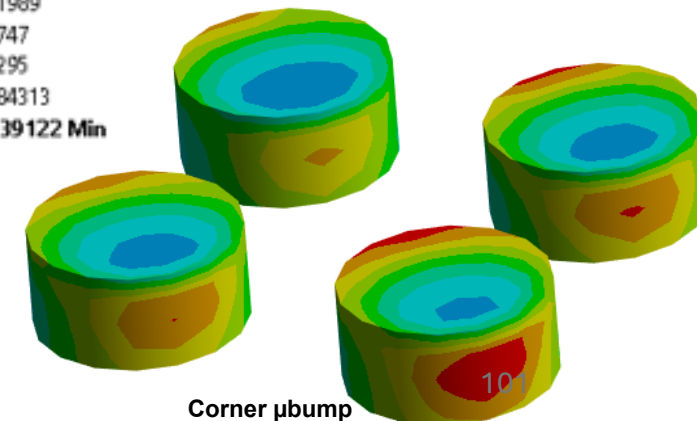
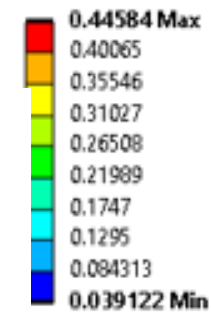
Corner μ bump

-40°C (2250s)



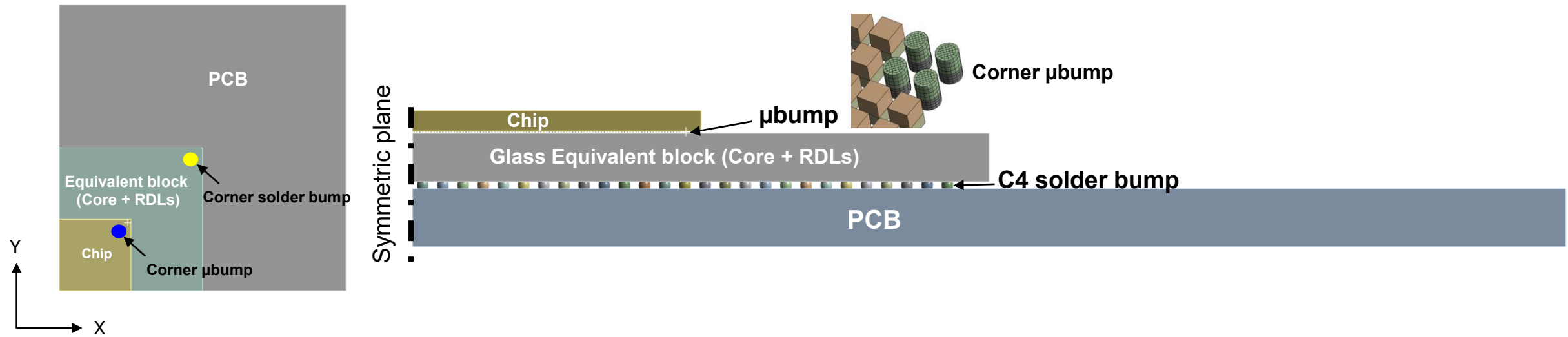
Corner μ bump

25°C (18000s)



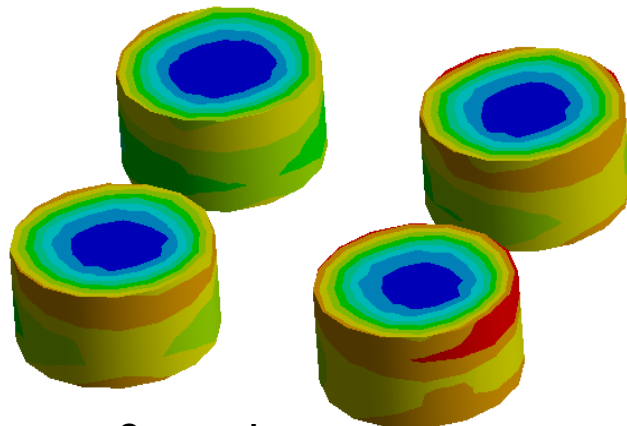
Corner μ bump

Maximum accumulated inelastic strain in corner μ bump of structure with glass core substrate



85°C (450s)

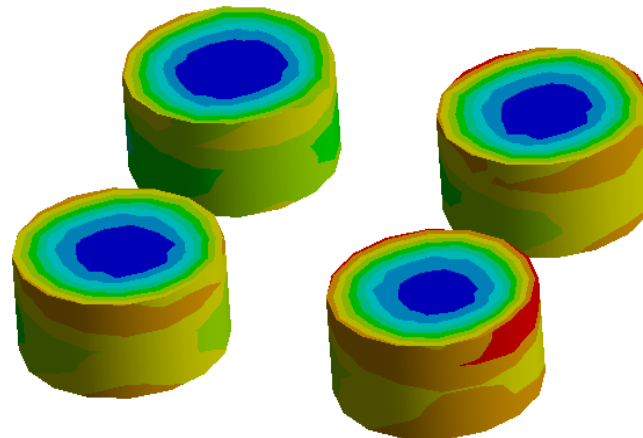
0.010903 Max
0.0099626
0.0090217
0.0080807
0.0071398
0.0061989
0.005258
0.0043171
0.0033761
0.0024352 Min



Corner μ bump

-40°C (2250s)

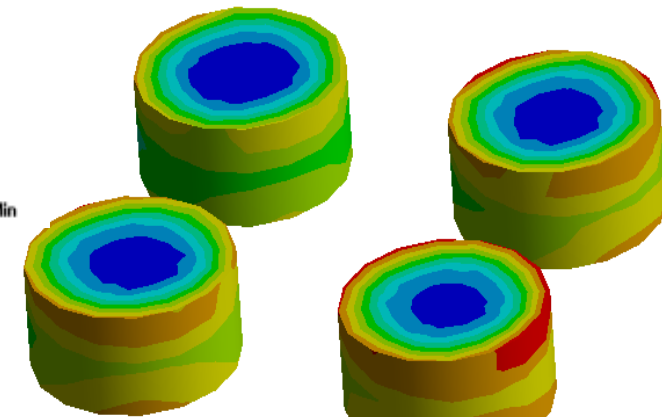
0.032329 Max
0.029551
0.026773
0.023995
0.021217
0.018438
0.01566
0.012882
0.010104
0.0073257 Min



Corner μ bump

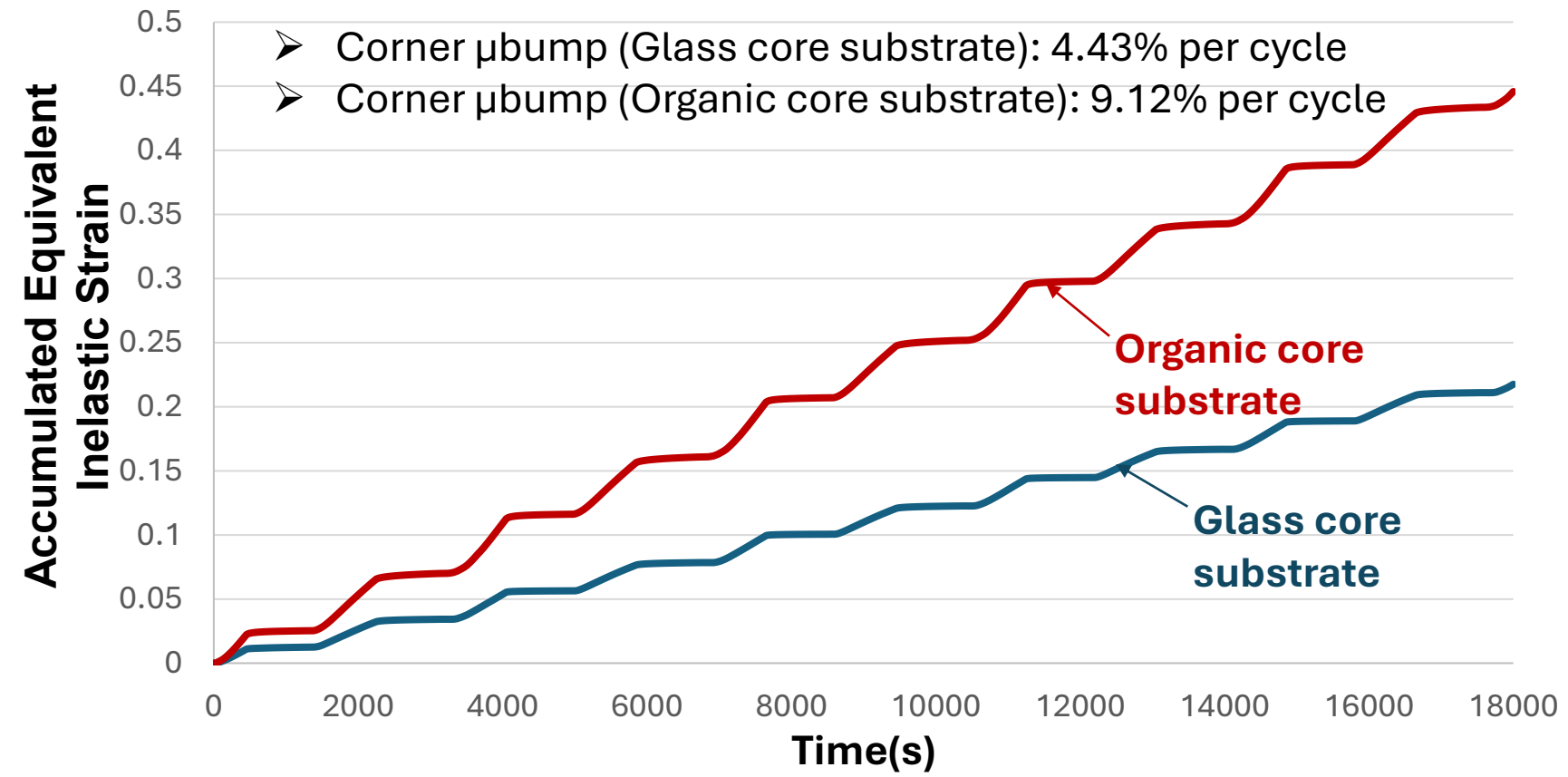
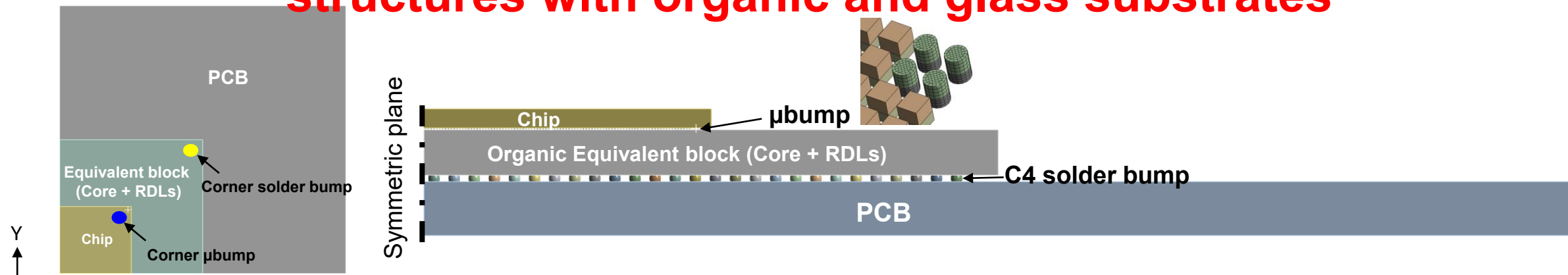
25°C (18000s)

0.21753 Max
0.19695
0.18098
0.16181
0.14323
0.12466
0.10608
0.087508
0.068934
0.050359 Min

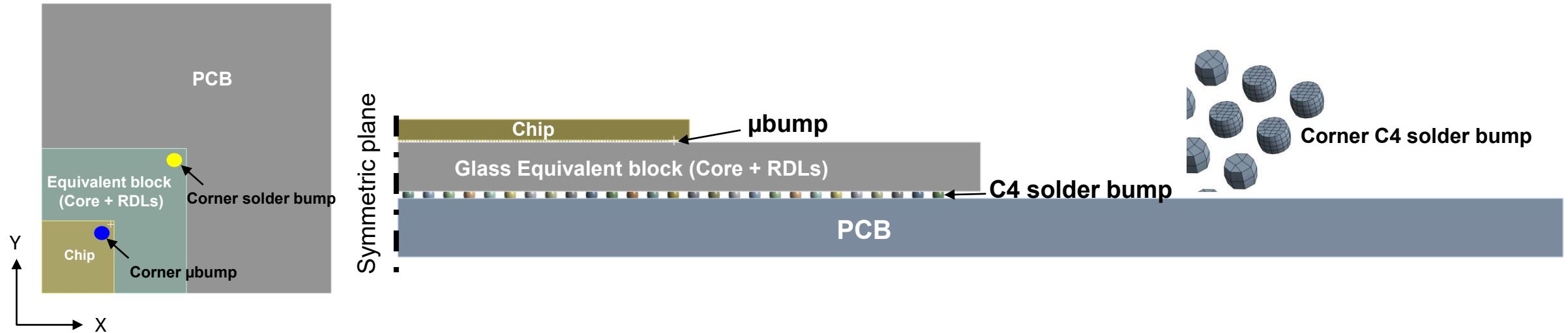


Corner μ bump

Maximum accumulated inelastic strain time-history in corner μ bump of structures with organic and glass substrates

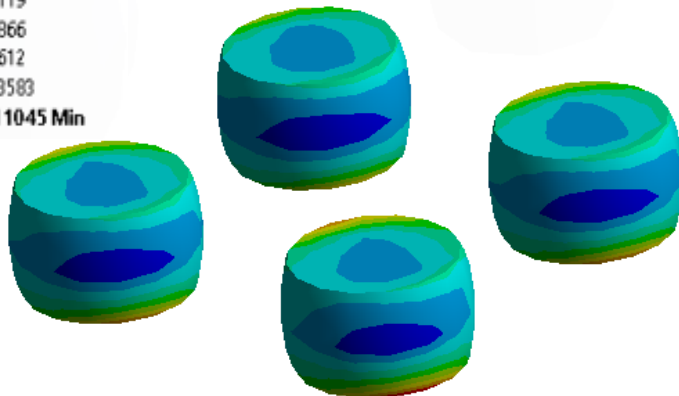


Maximum accumulated inelastic strain in corner C4 solder joint of structure with organic core substrate.



85°C (450s)

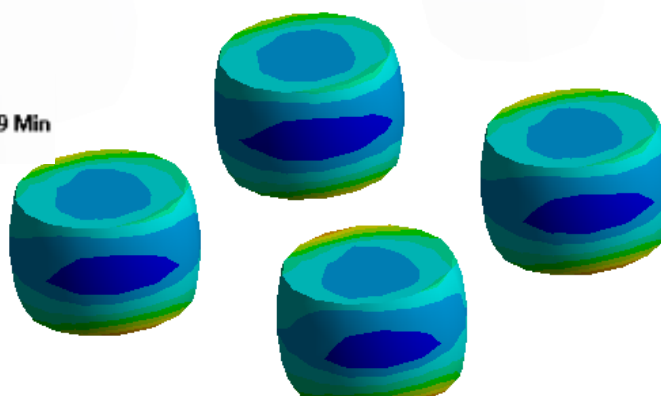
0.048388 Max
0.043134
0.037881
0.032627
0.027373
0.022119
0.016866
0.011612
0.0063583
0.0011045 Min



Corner solder bump

-40°C (2250s)

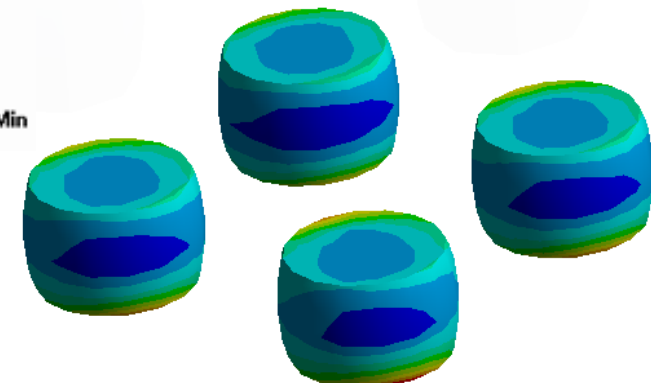
0.14988 Max
0.13351
0.11713
0.10075
0.084379
0.068003
0.051627
0.035251
0.018875
0.002499 Min



Corner solder bump

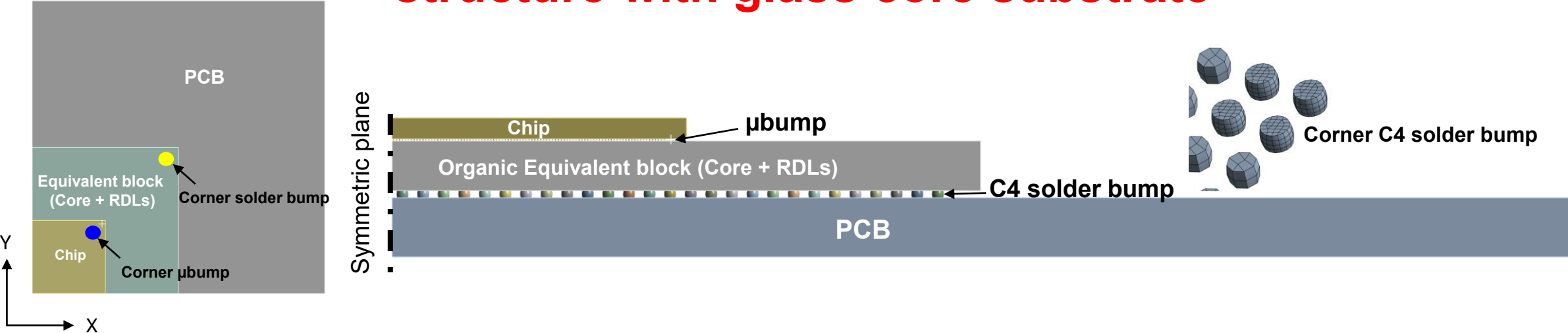
25°C (18000s)

0.9424 Max
0.83901
0.73562
0.63223
0.52884
0.42545
0.32206
0.21867
0.11528
0.011888 Min

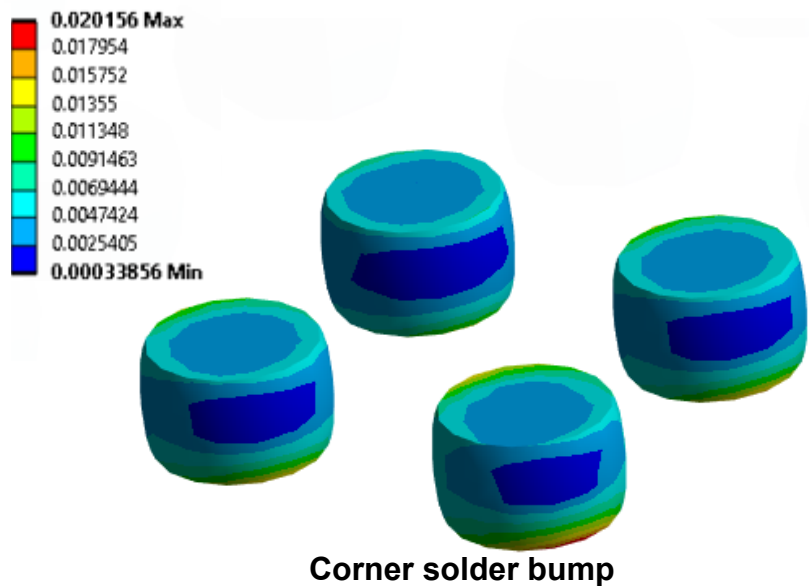


Corner solder bump

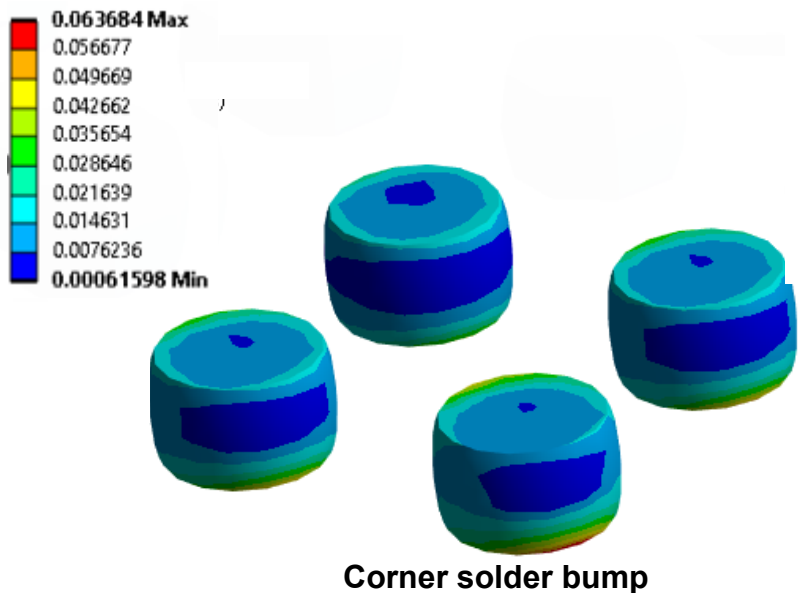
Maximum accumulated inelastic strain in corner C4 solder joint of structure with glass core substrate



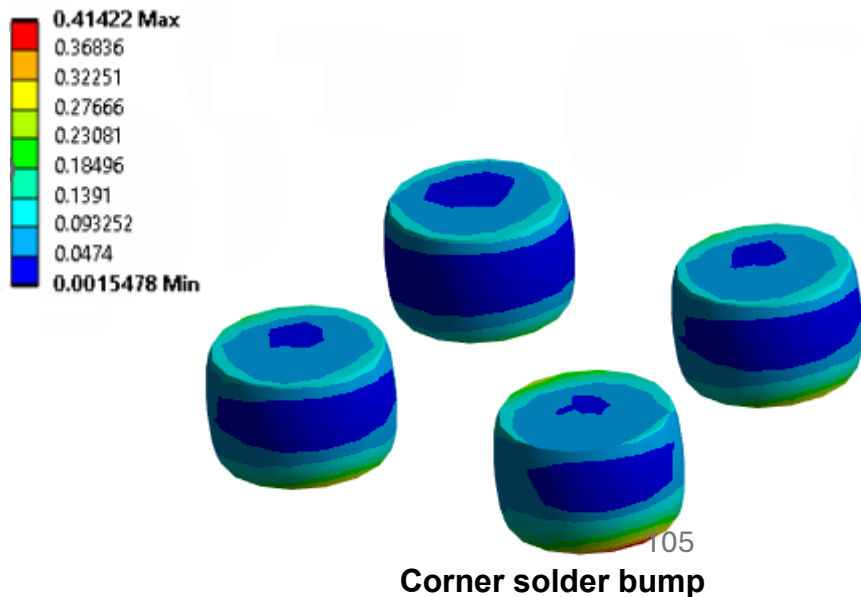
85°C (450s)



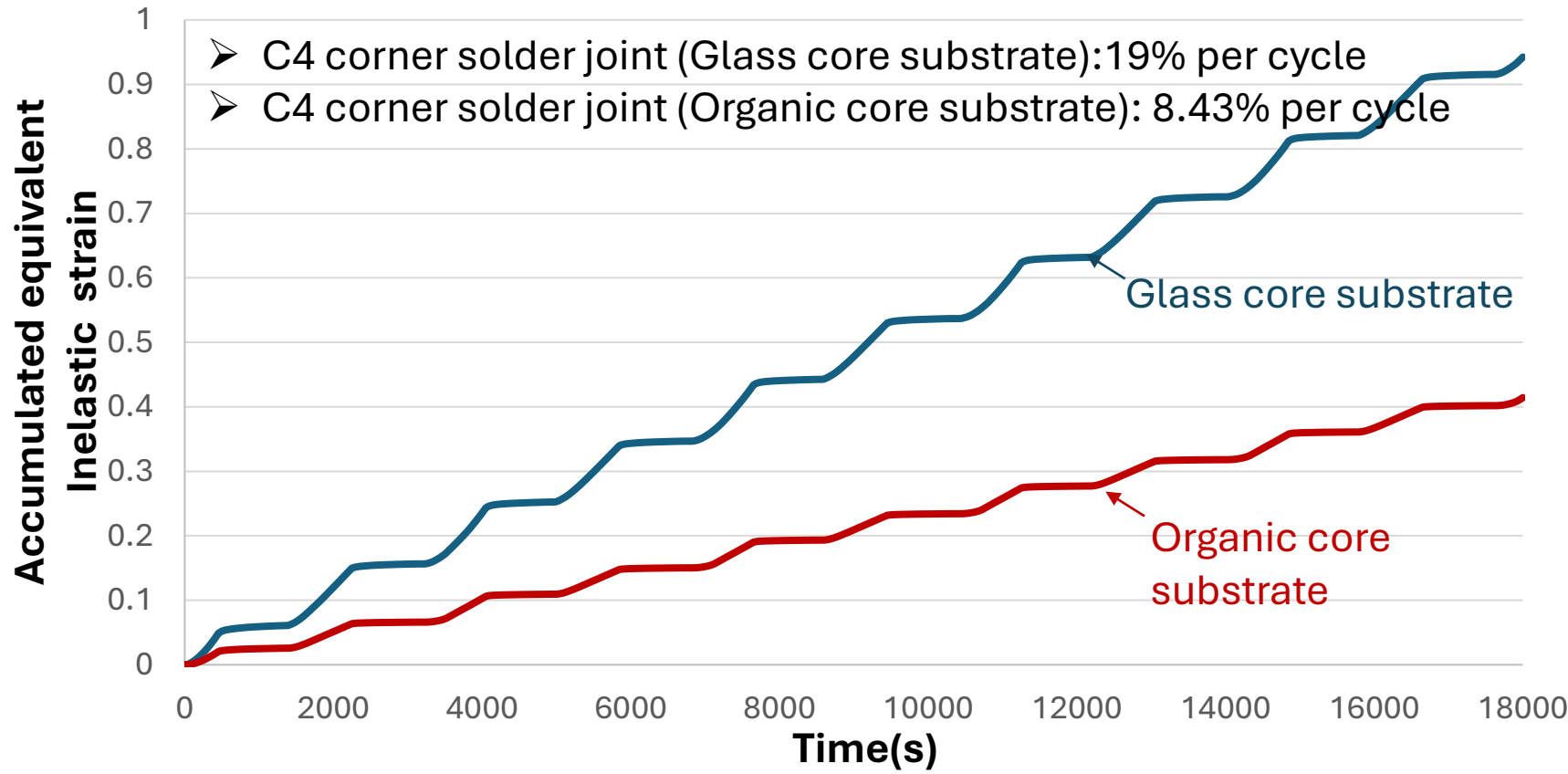
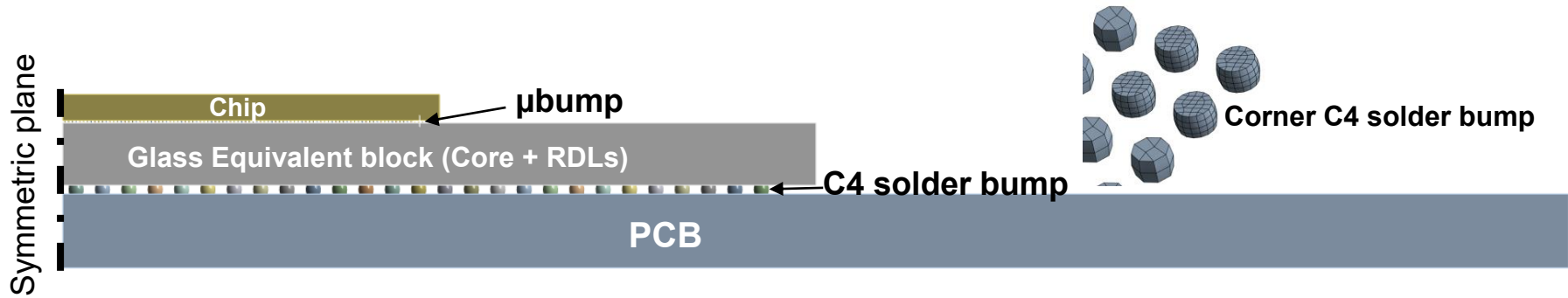
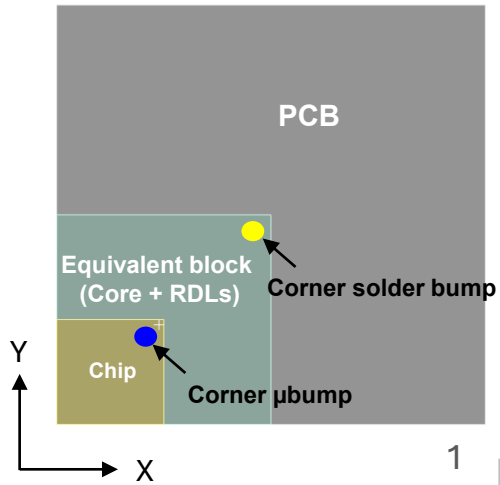
-40°C (2250s)



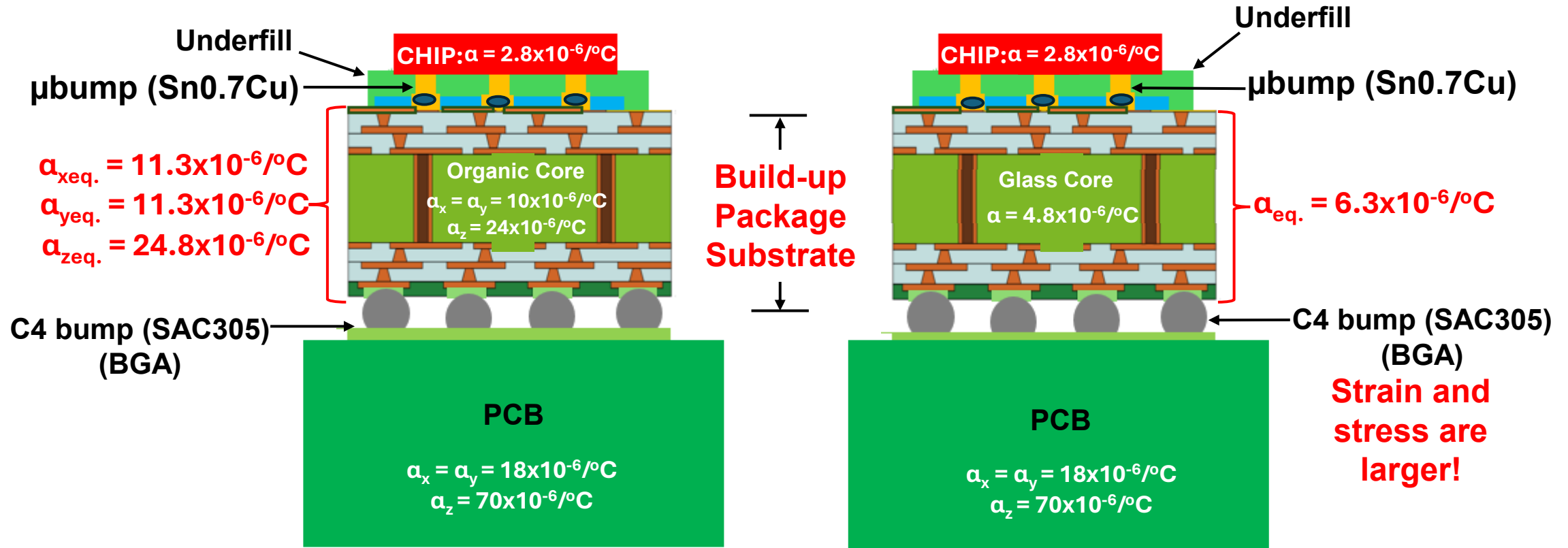
25°C (18000s)



Maximum accumulated inelastic strain time-history in corner C4 solder joint of structures with organic and glass substrates



C4 Solder Joint Reliability: Glass core vs. Organic Core



SUMMARY

As a matter of fact, the CTE of the glass substrate should be closer to the PCB CTE. Say $10 \times 10^{-6}/^{\circ}\text{C}$

Because there is underfill protection of the μ bump solder joint on the glass substrate but there is no underfill protection for the C4 or BGA solder joints on the PCB.

Especially for larger glass package substrates, especially housing the one trillion transistors..

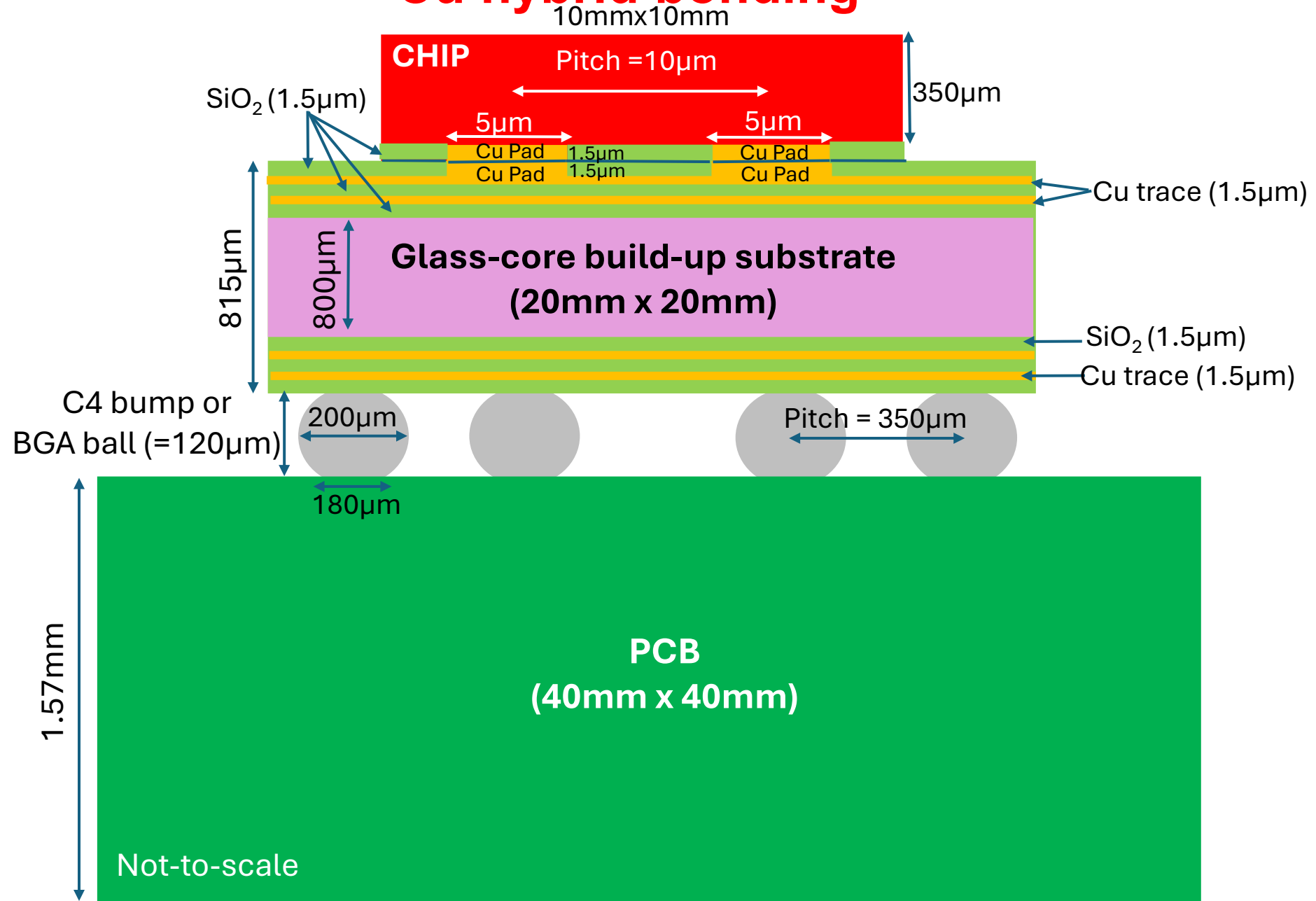
As a matter of fact, the CTE of the glass substrate should be closer to the PCB CTE

because there is underfill protection of the μ bump solder joint on the glass substrate but there is no underfill protection of the C4 or BGA solder joints on the PCB especially for larger glass package substrates.

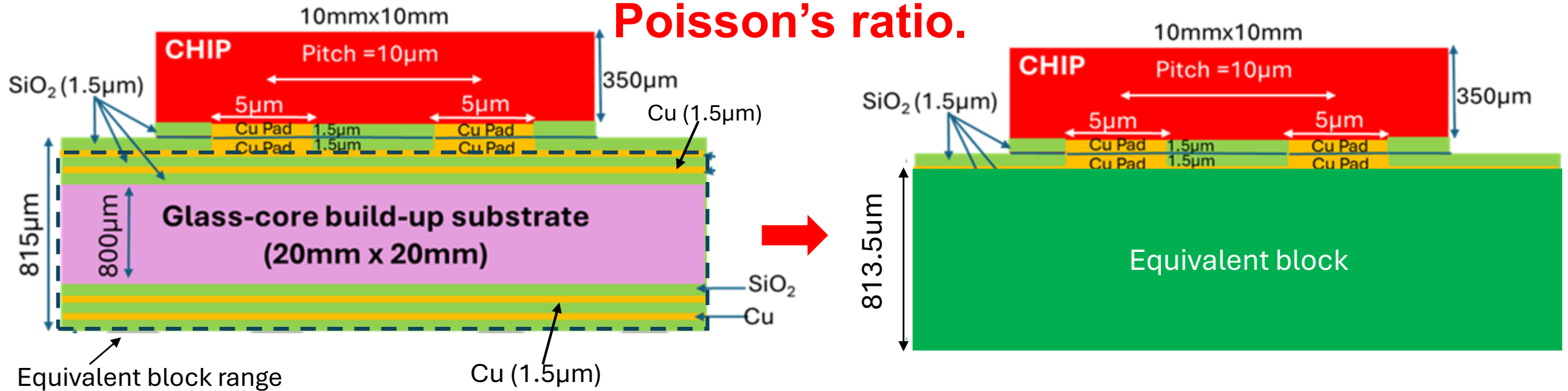
Flip Chip on Glass-core Substrate with Cu-Cu Hybrid Bonding

**(Effects of glass-core substrate on Solder Joint
Reliability)**

Cross section of flip chip on glass-core substrate with bumpless Cu-Cu hybrid bonding



Equivalent Young's modulus, equivalent CTE, and equivalent Poisson's ratio.



□ For Equivalent Young's modulus: **70.3GPa**

$$\frac{121 \times (1.5 \times 4) + 70 \times (1.5 \times 5) + 72 \times 800}{(1.5 \times 4) + (1.5 \times 5) + 800} = 70.3 \text{GPa}$$

□ For Equivalent Poisson's ratio: **0.29**

$$\frac{0.34 \times (1.5 \times 4) + 0.17 \times (1.5 \times 5) + 0.29 \times 800}{(1.5 \times 4) + (1.5 \times 5) + 800} = 0.29$$

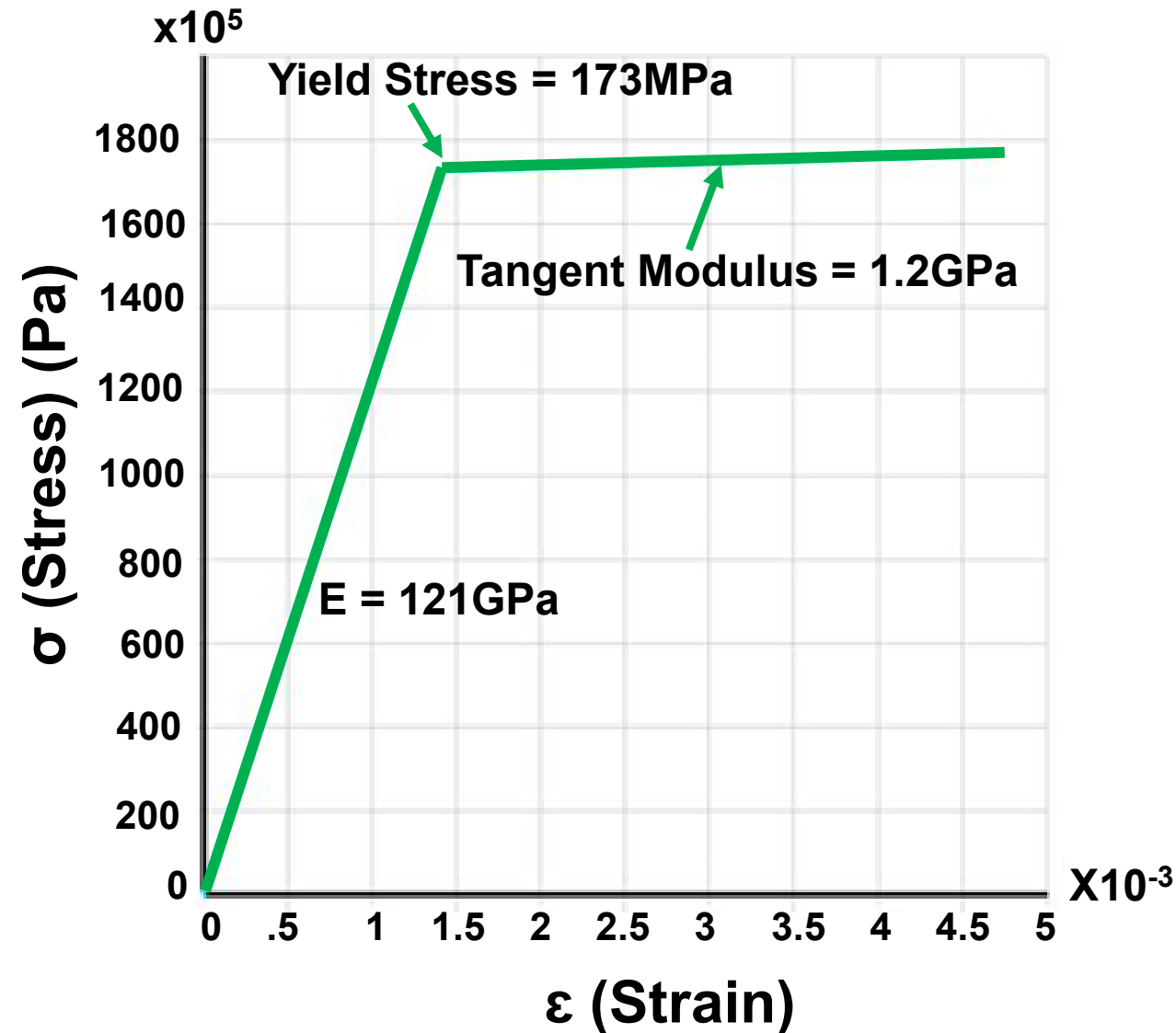
□ For Equivalent CTE (Glass = 4.8): **4.85x10⁻⁶/°C**

$$\frac{16.3 \times (1.5 \times 4) + 0.5 \times (1.5 \times 4) + 4.8 \times 800}{(1.5 \times 4) + (1.5 \times 5) + 800} = 4.85 \times 10^{-6} / ^\circ \text{C}$$

□ For Equivalent CTE (Glass = 10): **9.96x10⁻⁶/°C**

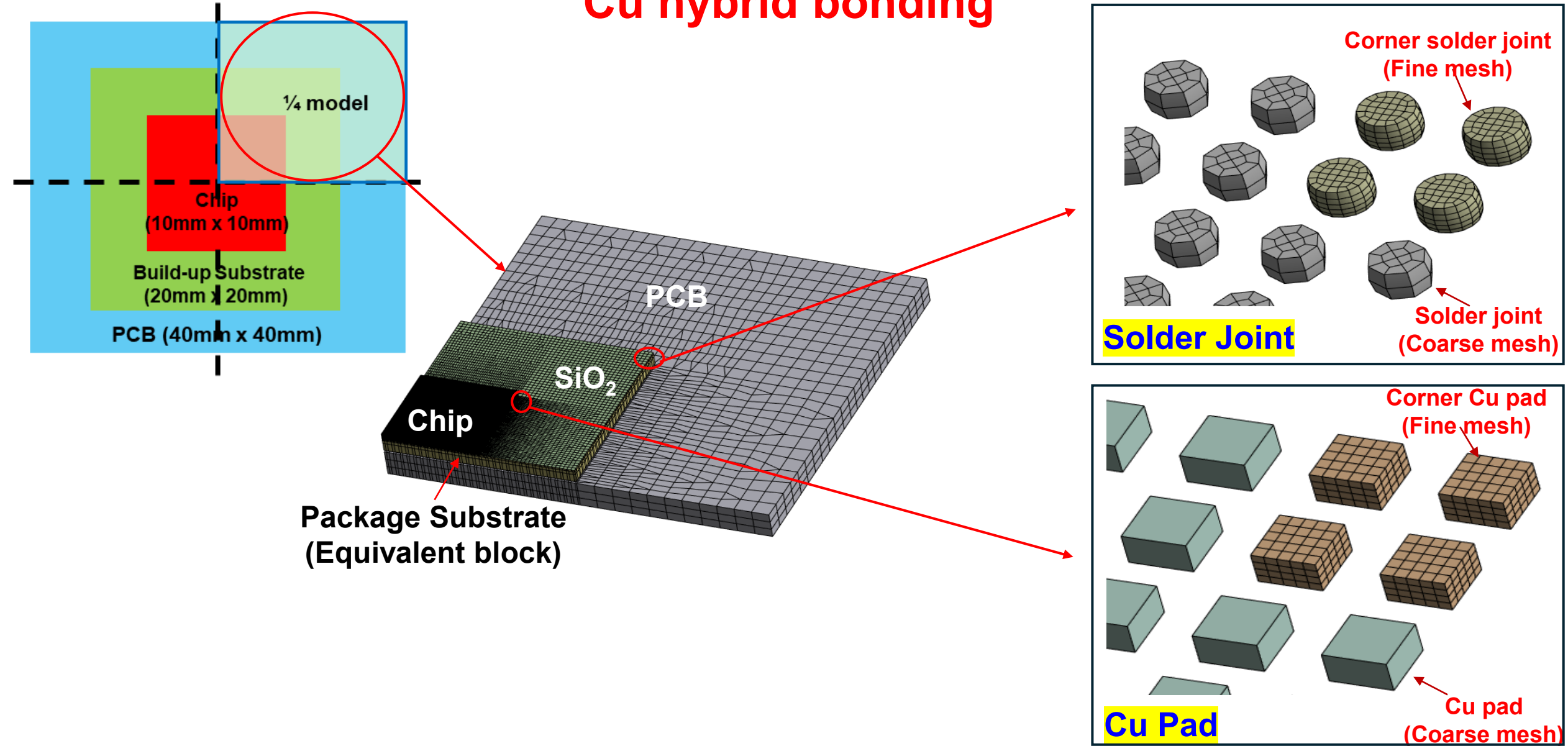
$$\frac{16.3 \times (1.5 \times 4) + 0.5 \times (1.5 \times 4) + 10 \times 800}{(1.5 \times 4) + (1.5 \times 5) + 800} = 9.96 \times 10^{-6} / ^\circ \text{C}$$

Elastoplastic of dual-damascene copper

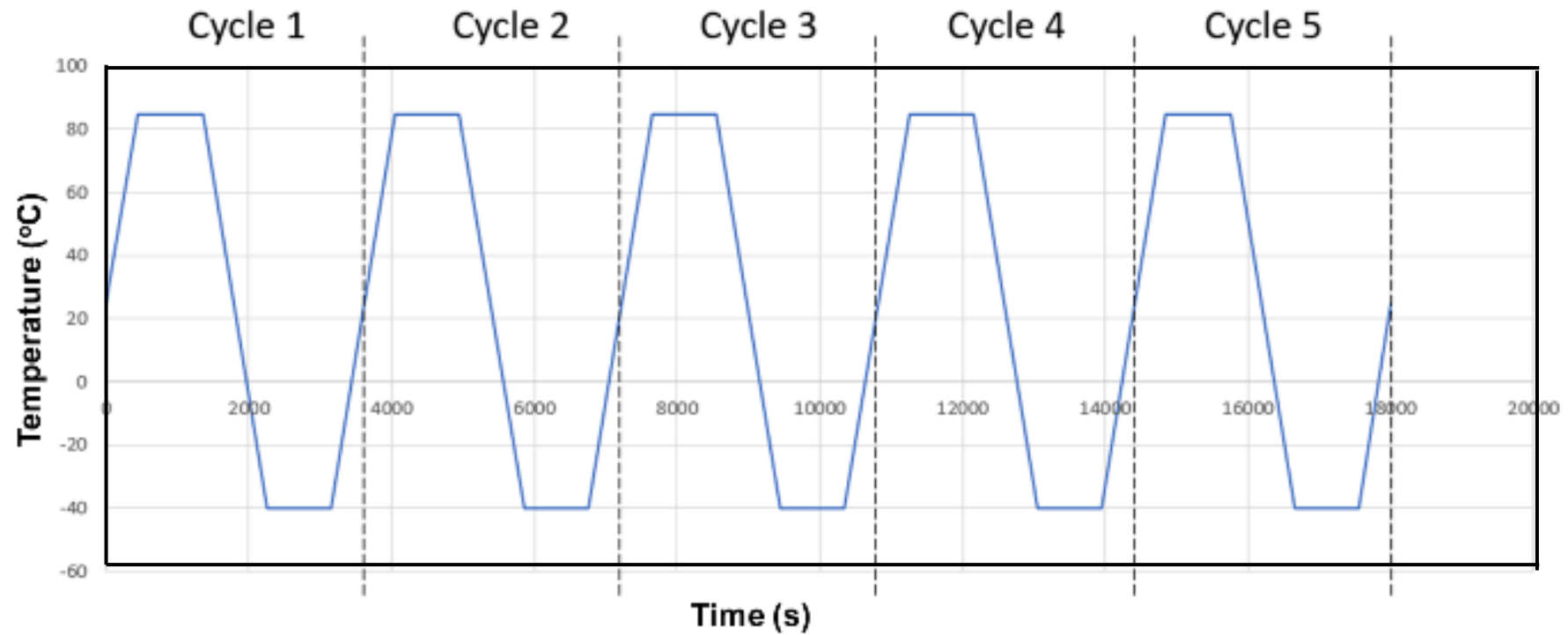


- Consider copper Bauschinger effect, Kinematic hardening is used in this material.

Finite element modeling of flip chip on glass-core substrate with Cu-Cu hybrid bonding

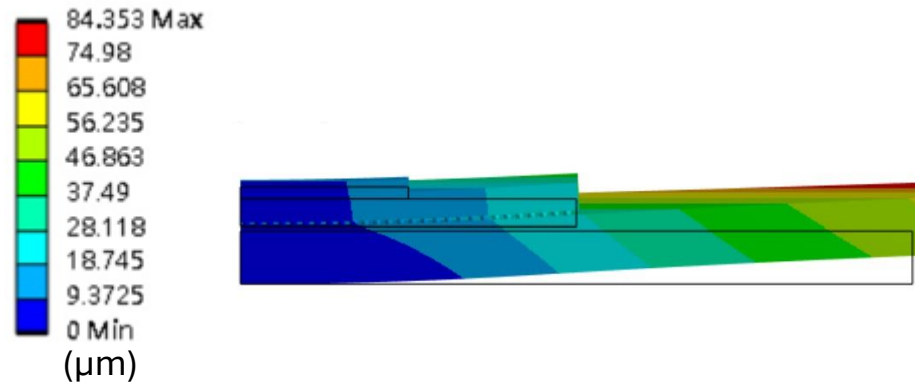


Thermal cycling boundary condition

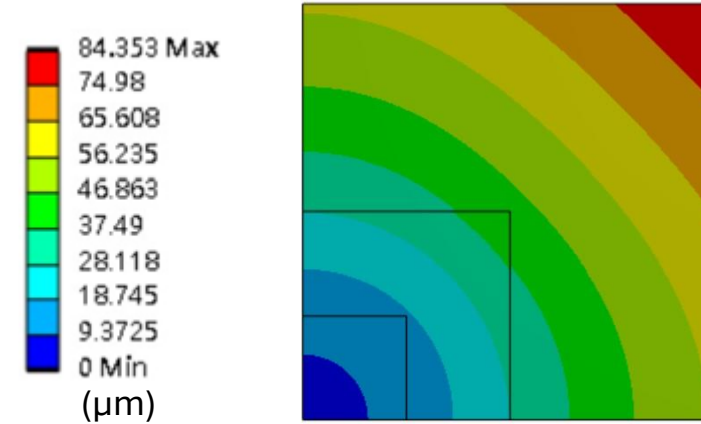


Deformation of structure with organic-core substrate.

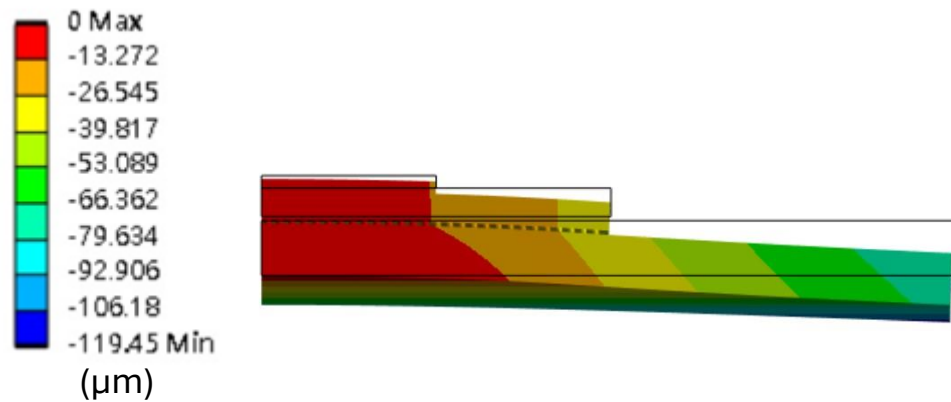
85°C (450s)_Side view



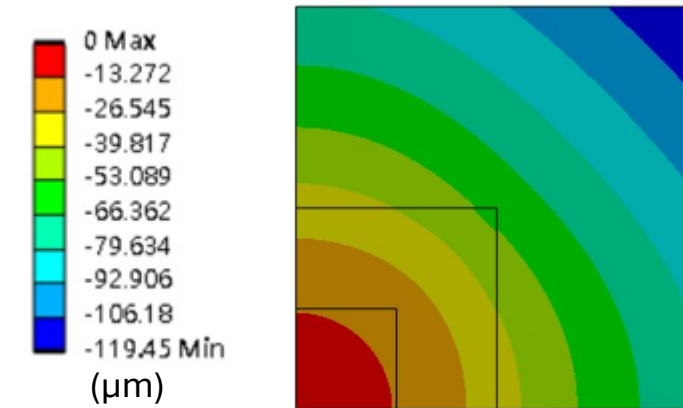
85°C (450s)_Top view



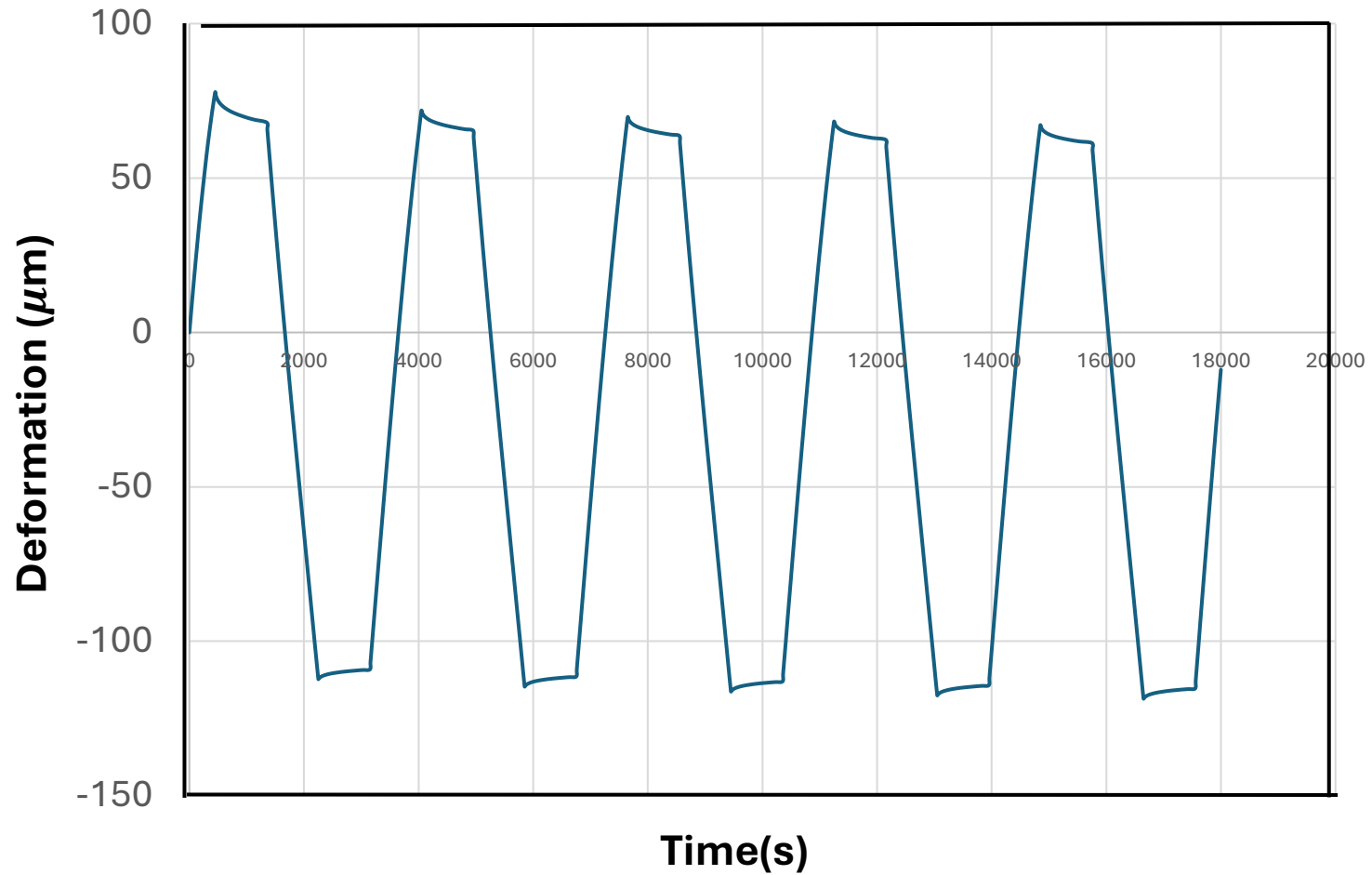
-40°C (2250s)_Side view



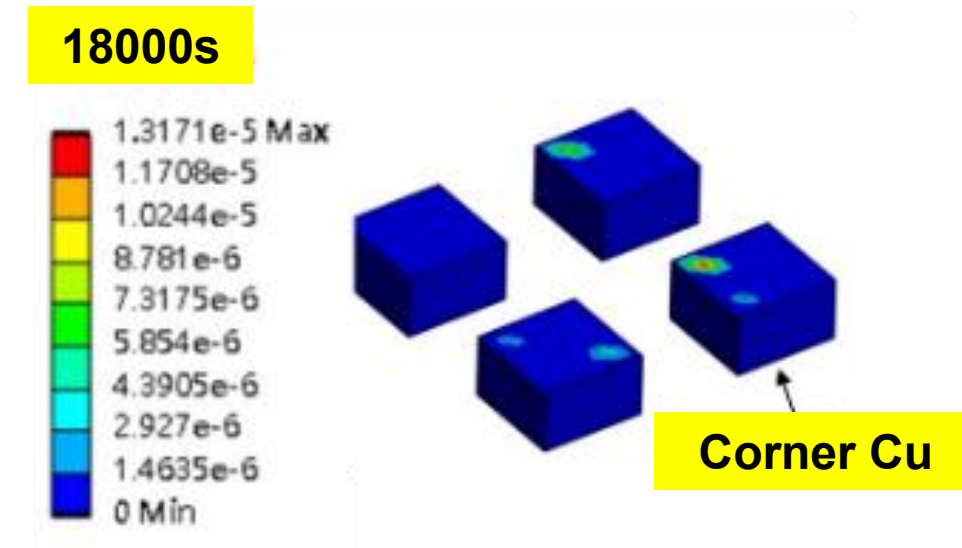
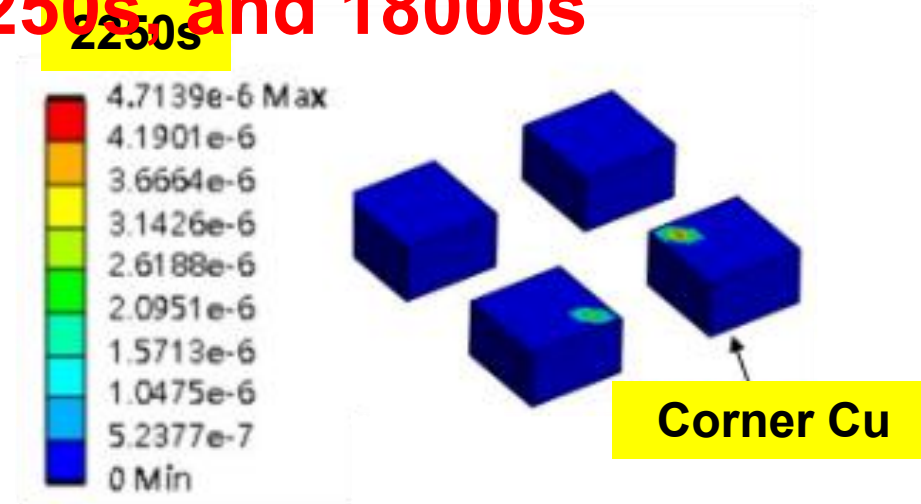
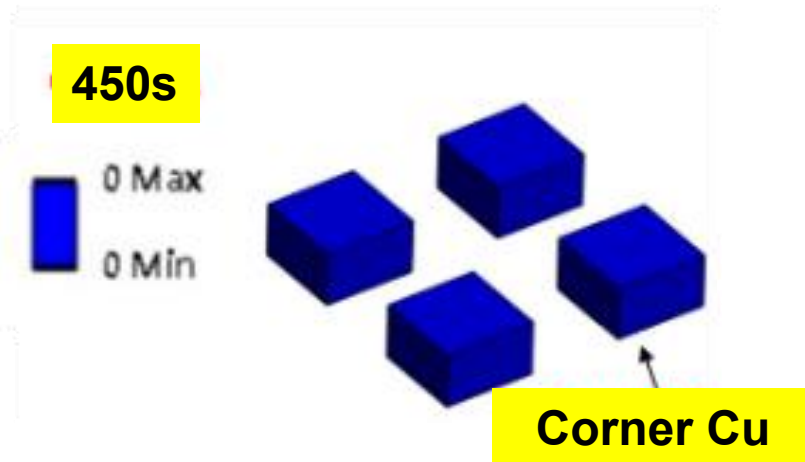
-40°C (2250s)_Top view



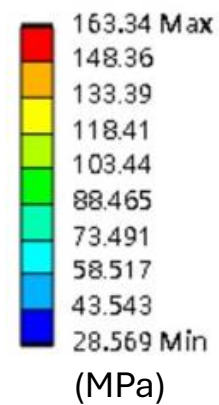
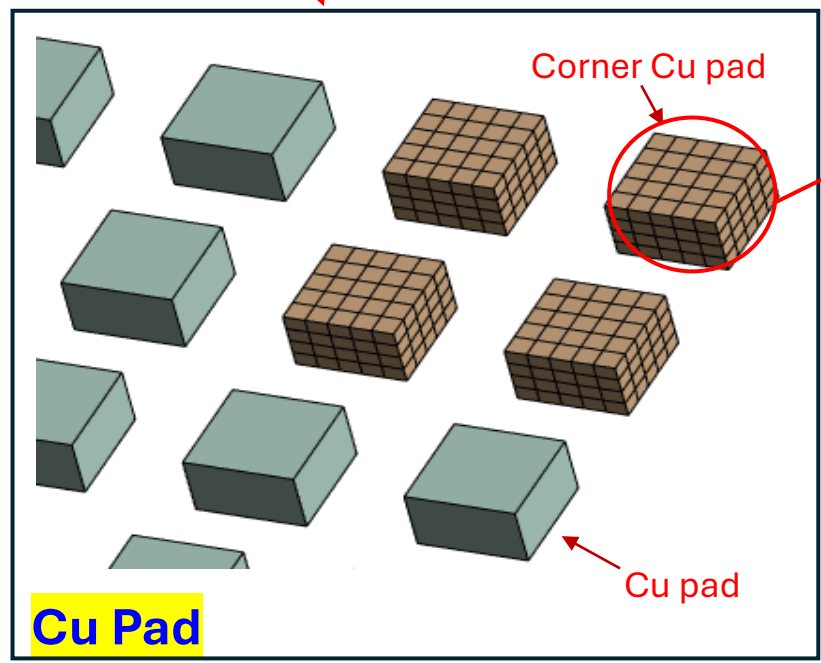
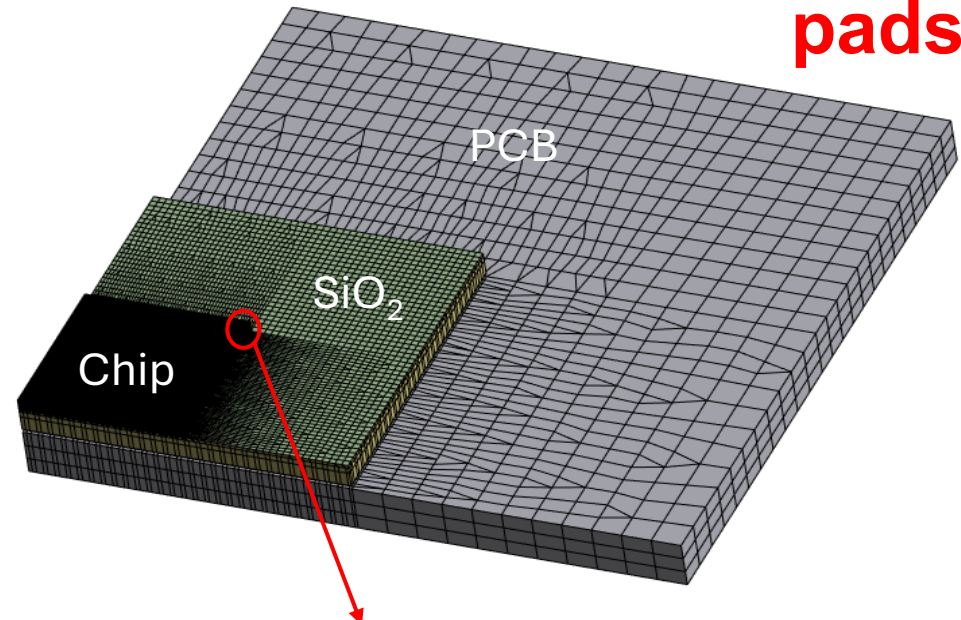
Time-history deformation of the structure



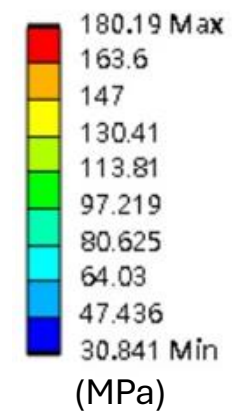
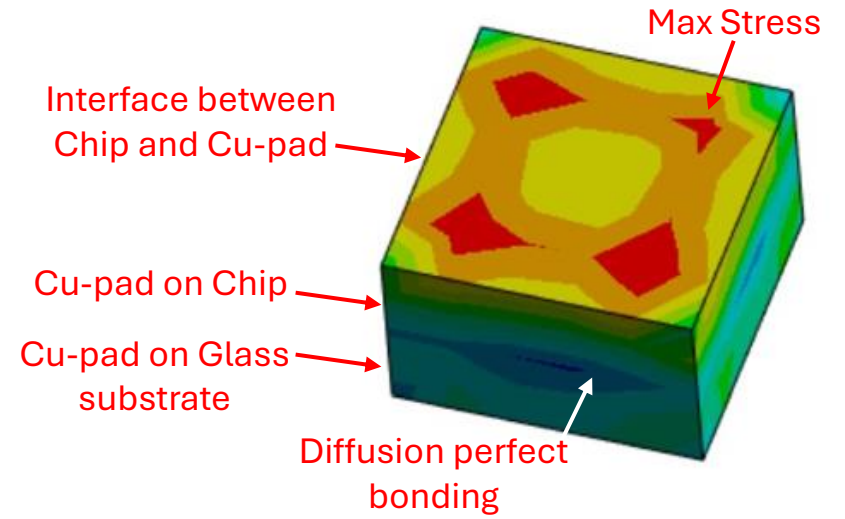
Accumulated equivalent inelastic strain contours at the corner Cu-pads at 450s, 2250s, and 18000s



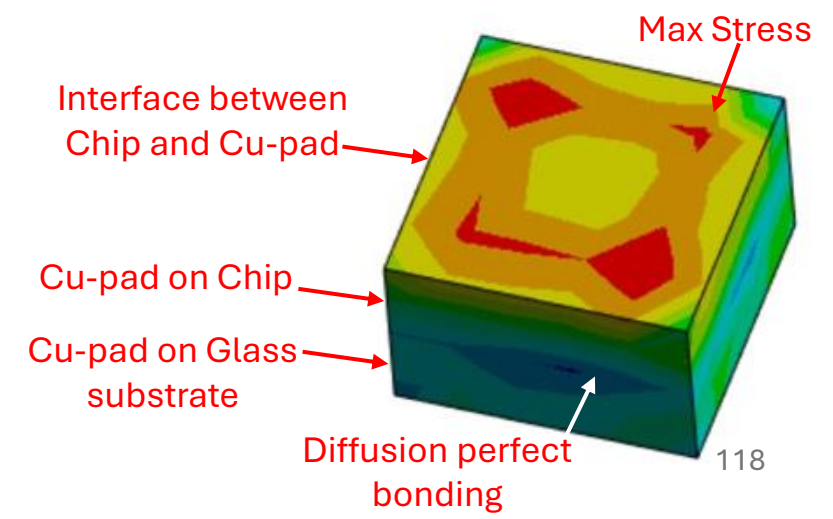
Accumulated equivalent (von Mises) stress contours at the corner Cu-pads at 450s and 2250s.



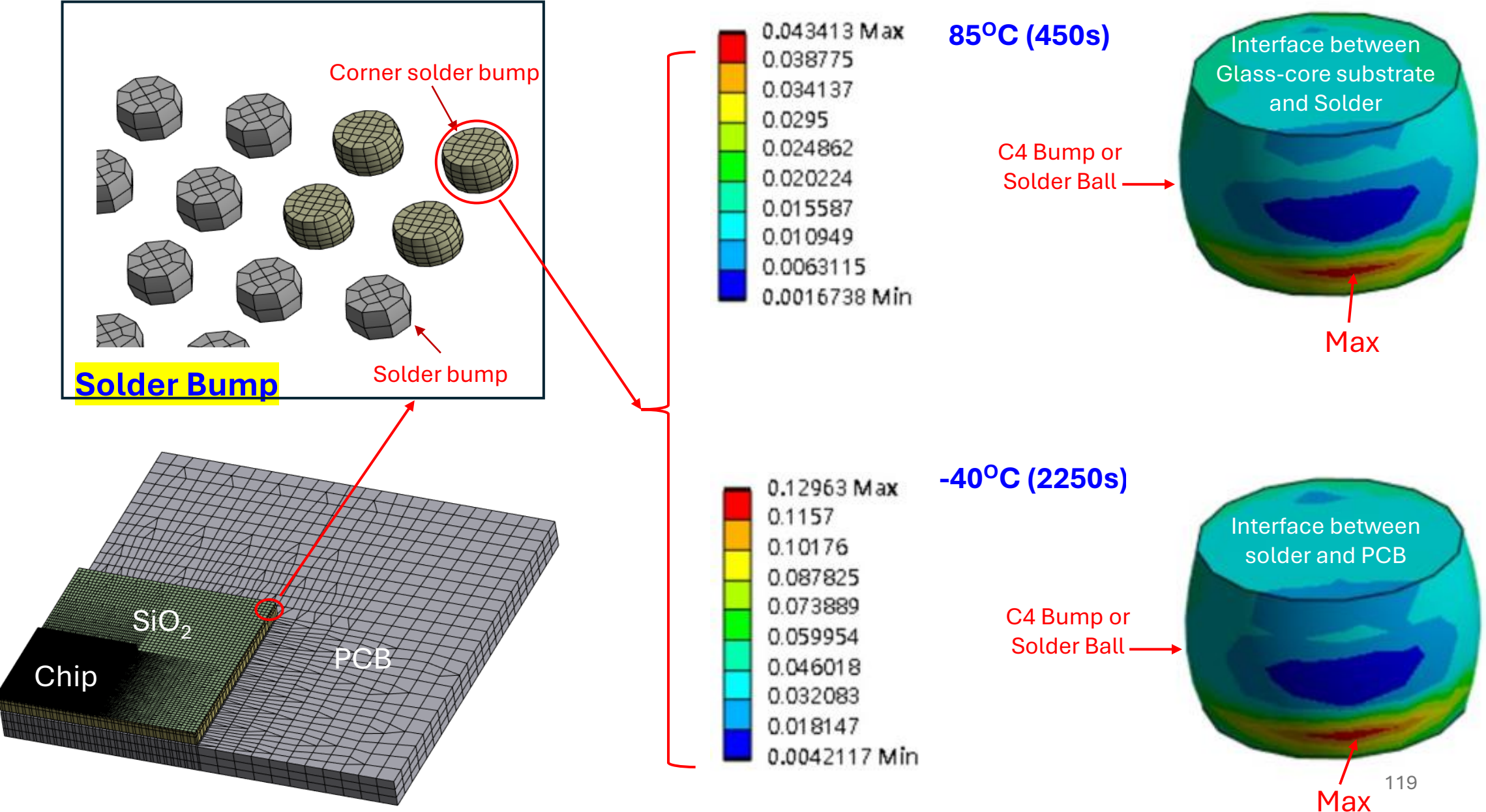
85°C (450s)



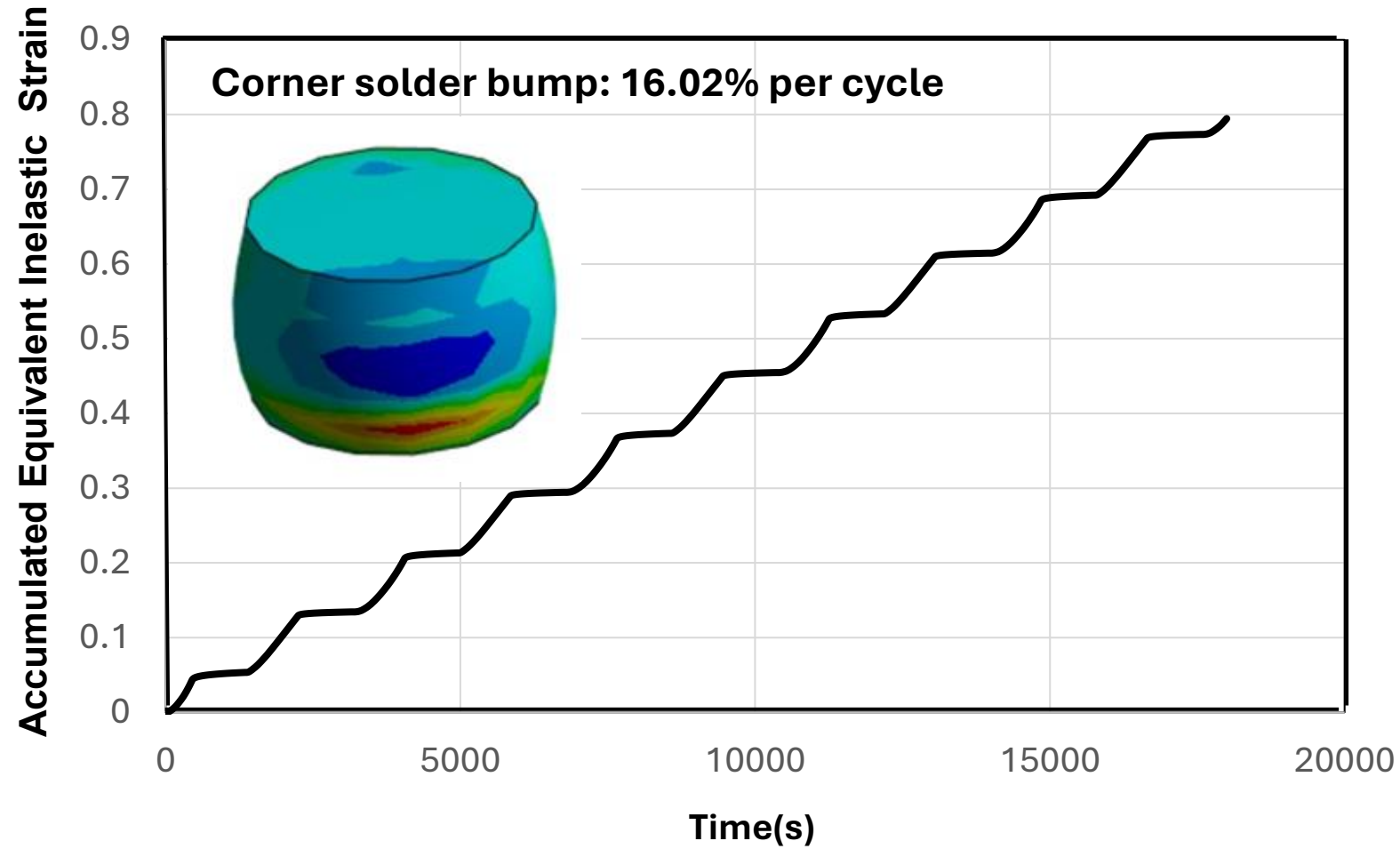
-40°C (2250s)



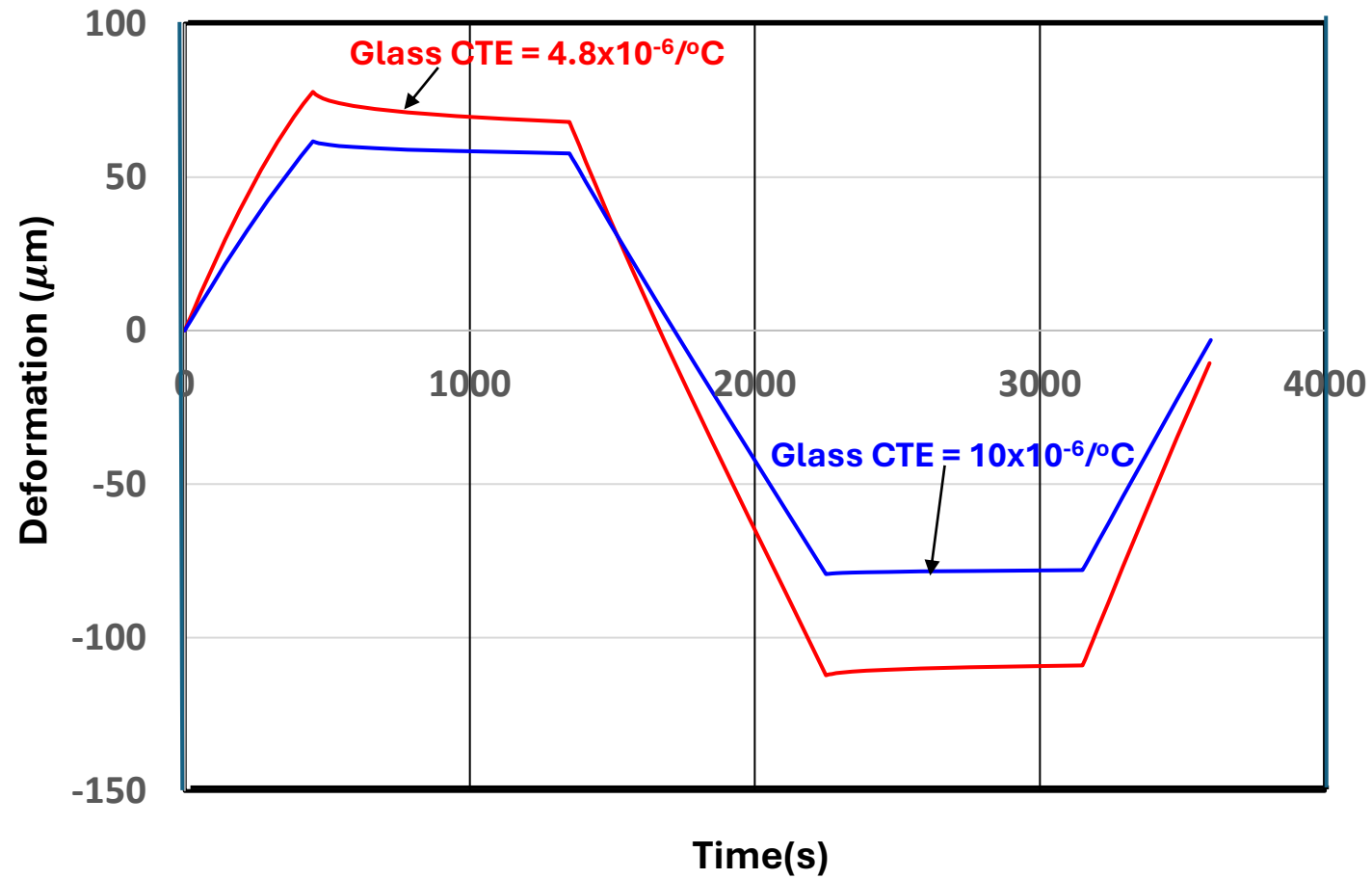
Accumulated equivalent inelastic strain contours at the corner solder ball at 450s and 2250s



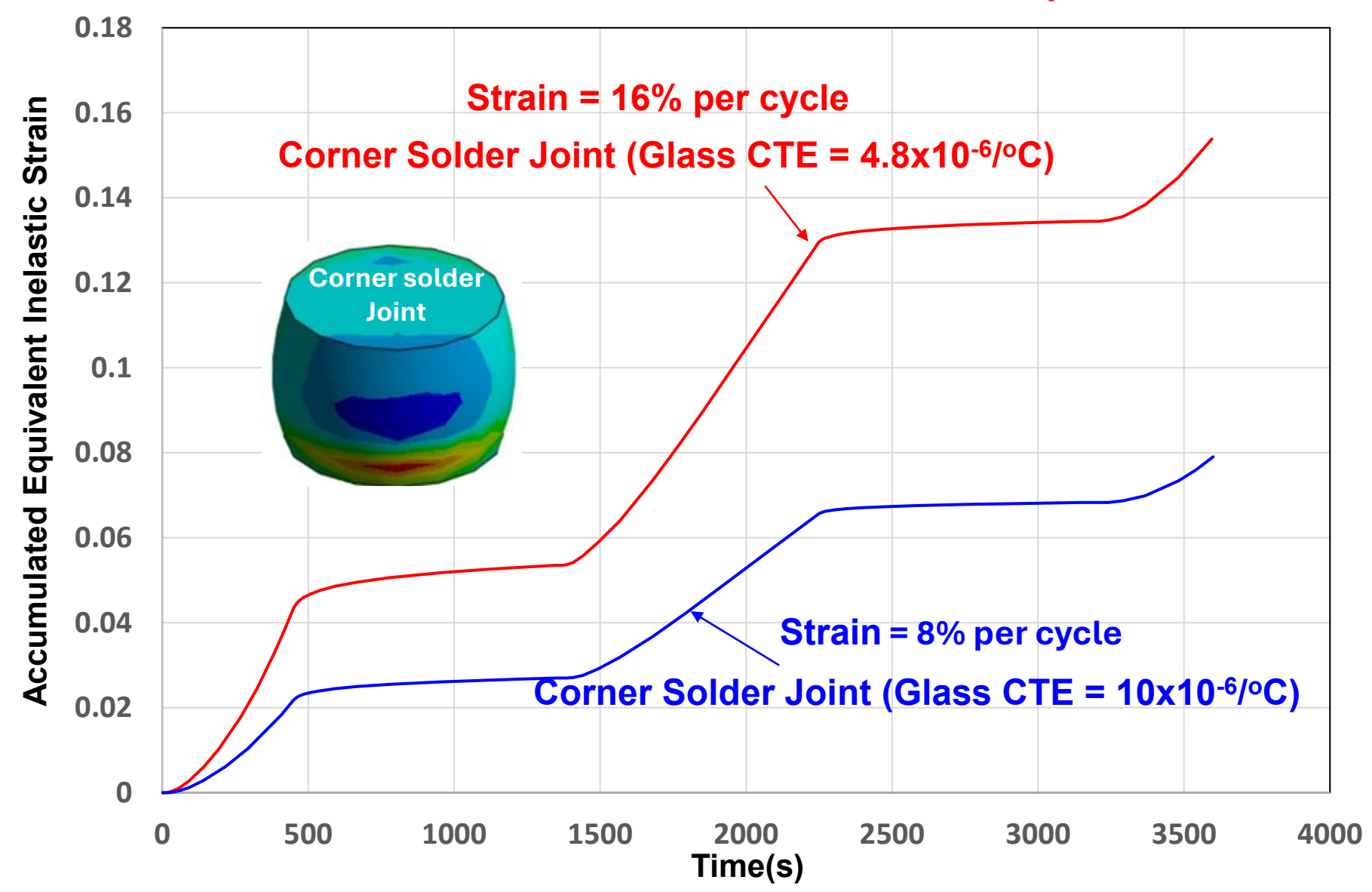
Time-history accumulated equivalent inelastic strain at the corner solder ball



Warpage for glass-core substrate with CTE = $4.8 \times 10^{-6}/^{\circ}\text{C}$ and $10 \times 10^{-6}/^{\circ}\text{C}$



Accumulated equivalent inelastic strain at the corner solder joint (CTE = $4.8 \times 10^{-6}/^{\circ}\text{C}$ and $10 \times 10^{-6}/^{\circ}\text{C}$).



RECOMMENDATION

The CTE of Glass should be as close as to the PCB, instead of the Silicon chip.

Some Recent Advanced Packaging Papers Published by the Lecturer and his Colleagues

1. Lau, J. H., N. Liu, T. Tseng, “Microbump Reliability of Silicon Bridges for Chiplets Heterogeneous Integration”, *Journal of Microelectronic Reliability*, Vol. 185, August 2026, pp. 116262.
2. Lau, J. H., “Current Advances and Outlook of Advanced Packaging”, *ASME Transactions, Journal of Electronic Packaging*, published online: February 11, 2026.
3. Lau, J. H., “State-of-the-art and Outlooks of Cu-Cu Hybrid Bonding”, *IEEE Transactions on CPMT*, Dec 2025, pp. 2575-2613.
4. Lau, J. H., “Co-Packaged Optics - Heterogeneous Integration of Chiplets (Switch, Photonic IC, and Electronic IC)”, *J. of Microelectronic Packaging*, V 22, Issue 4, Dec. 2025, pp. 93-104.
5. Lau, J. H., N. Liu, M. Ma, and T. Tseng, “Flip Chip on Glass-Core Substrates with Microbump and Cu-Cu Hybrid Bonding”, *J. of Microelectronic Packaging*, V. 22, I3, Sept.2025, pp. 44-60.
6. Lau, J. H., N. Liu, M. Ma, and T. Tseng, “Flip Chip on Glass-Core Substrates with Microbump and Cu-Cu Hybrid Bonding”, *Journal of Microelectronic Packaging*, 3rd Quarter, 2025.
7. Lau, J. H., N. Liu, M. Ma, and T. Tseng, “Solder joint reliability - glass core substrate versus organic core substrate”, *Journal of Microelectronic Reliability*, Vol. 168, May 2025, pp. 115701.
8. Lau, J. H., “Current Advances and Outlooks in Hybrid Bonding”, *IEEE Transactions on CPMT*, Vol. 15, No. 3, March 2025, pp. 651-681.
9. Lau, J. H., “Co-Packaged Optics - Heterogeneous Integration of Photonic IC and Electronic IC”, *ASME Transactions, J. of Electronic Packaging*, Vol. 147, March 2025, pp. 1-12.
10. Lau, J. H., “State-of-the-art of Cu-Cu Hybrid Bonding”, *IEEE Transactions on CPMT*, Vol. 14, No. 3, March 2024, pp. 376-396.
11. Lau, J. H., G. Chen, et al., “Hybrid Substrates for Heterogeneous Integration” *ASME Transactions, J. of Electronic Packaging*, published online: Aug 11, 2023.
12. Lau, J. H., C. Lin, et al., “Hybrid Substrate with Ultra-Large Organic Interposer for Heterogeneous Integration”, *IEEE Transactions on CPMT*, Vol. 13, No. 9, September 2023, pp. 1371-1379.
13. Lau, J. H., “Recent Advances and Trends in Chiplet Design and Heterogeneous Integration Packaging”, *ASME Trans., J. of Electronic Packaging*, published online: June 23, 2023.
14. Lau, J. H., “Recent Advanced and Trends in Cu-Cu Hybrid Bonding”, *IEEE Transactions on CPMT*, Vol. 13, No. 3, March 2023, pp. 399-425.
15. Lau, J. H., “Recent Advanced and Trends in Multiple system and Heterogenous Integration with TSV-Interposers”, *IEEE Transactions on CPMT*, Vol. 13, No. 1, January 2023, pp. 3-25.
16. Lau, J. H., “Recent Advanced and Trends in Multiple system and Heterogenous Integration with TSV-less Interposers”, *IEEE Trans. on CPMT*, Vol. 12, No. 8, August 2022, pp. 1271-1280.
17. Lau, J. H., “Recent Advances and Trends in Advanced Packaging”, *IEEE Transactions on CPMT*, Vol. 12, No. 2, February 2022, pp. 228-252.
18. Lau, J. H., G. Chen, J. Huang, et al., “Hybrid Substrate by Fan-Out RDL-First Panel-Level Packaging”, *IEEE Transactions on CPMT*, Vol. 11, No. 8, August 2021, pp. 1301-1309.
19. Lau, J. H., “State of the Art of Lead-Free Solder Joint Reliability”, *ASME Transactions, Journal of Electronic Packaging*, Vol. 143, June 2021, pp. 1-36.
20. Lau, J. H., C. Ko, C. Lin, et al., “Fan-Out Panel-Level Packaging of Mini-LED RGB Display”, *IEEE Transactions on CPMT*, Vol. 11, No. 5, May 2021, pp. 739-747.
21. Lau, J. H., C. Ko, K. Yang, et al., “Panel-Level Fan-Out RDL-first Packaging for Heterogeneous Integration”, *IEEE Transactions on CPMT*, Vol. 10, No. 7, July 2020, pp. 1125-1137.
22. Lau, J. H., C. Ko, T. Tseng, et al., “Panel-Level Chip-Scale Package with Multiple Diced Wafers”, *IEEE Transactions on CPMT*, Vol. 10, No. 7, July 2020, pp. 1110-1124.
23. Lau, J. H., “Recent Advances and Trends in Fan-Out Wafer/Panel-Level Packaging”, *ASME Transactions, Journal of Electronic Packaging*, Vol. 141, December 2019, pp. 1-27.
24. Lau, J. H., M. Li, M. Li, et al., “Fan-out wafer-level packaging for heterogeneous integration,” *IEEE Transactions on CPMT*, Vol. 8, Issue 9, September 2018, pp. 1544-1560.
25. Lau, J. H., M. Li, Q. Li, et al., “Design, Materials, Process, and Fabrication of Fan-Out Wafer-Level Packaging”, *IEEE Transactions on CPMT*. Vol. 8, Issue 6, June 2018, pp. 991-1002.
26. Lau, J. H., M. Li, Y. Li, et al., “Warpage Measurements and Characterizations of FOWLP with Large Chips and Multiple RDLs”, *IEEE Transactions on CPMT*, October 2018, pp. 1729-1737.
27. Lau, J. H., M. Li, D. Tian, et al., “Warpage and Thermal Characterization of Fan-Out Wafer-Level Packaging”, *IEEE Transactions on CPMT*, Vol. 7, Issue 10, October 2017, pp. 1729-1738.
28. Lau, J. H., “Recent Advances and New Trends in Flip Chip Technology”, *ASME Transactions, Journal of Electronic Packaging*, September 2016, Vol. 138, Issue 3, pp. 1-23.
29. Lau, J. H., Q. Zhang, M. Li, et al., “Stencil Printing of Underfill for Flip Chips on Organic-Panel and Si-Wafer Substrates”, *IEEE Trans. on CPMT*, Vol. 5, No. 7, July 2015, pp. 1027-1035.
30. Lau, J. H., “Overview and Outlook of 3D IC Packaging, 3D IC Integration, and 3D Si Integration”, *ASME Trans, Journal of Electronic Packaging*, Dec. 2014, Vol. 136, Issue 4, pp. 1-15.
31. Lau, J. H., C. Lee, C. Zhan, et al., “Low-Cost Through-Silicon Hole Interposers for 3D IC Integration”, *IEEE Transactions on CPMT*, Vol. 4, No. 9, September 2014, pp. 1407-1419.
32. Peng, C., J. H. Lau, C. Ko, et al., “High-Density Hybrid Substrate for Heterogeneous Integration”, *IEEE Transactions on CPMT*, Vol. 12, No.3, March 2022., pp. 469-478.
33. Lee, Z., J. H. Lau, CT Ko, et al., “Characterization of Low-Loss Dielectric Materials for High-Speed and High-Frequency Applications”, *Materials Journal*, 15, 2022, pp. 1-16.
34. Ko, CT, H. Yang, Lau, J. H., et al., “Chip-First Fan-Out Panel Level Packaging for Heterogeneous Integration”, *IEEE Transactions on CPMT*, 2018, V 8, Issue 9, Sept. 2018, pp. 1561-1572.

Some Packaging Books Published by the Lecturer

1. Lau, J. H., and K. Chiang, *Cu-Interconnects, Glass, and AI-Assisted Simulation for Chiplets and heterogeneous Integration*, Springer, New York, 2026.
2. Lau, J. H., and X. Fan, *Hybrid Bonding, Advanced Substrates, Failure Mechanisms, and Thermal Management for Chiplets and Heterogeneous Integration*, Springer, New York, April 2025.
3. Lau, J. H., *Flip Chip, Hybrid Bonding, Fan-in, and Fan-out Technology*, Springer, New York, 2024.
4. Lau, J. H., *Chiplet Design and Heterogeneous Integration Packaging*, Springer, New York, 2023.
5. Lau, J. H., *Semiconductor Advanced Packaging*, Springer, New York, 2021.
6. Lau, J. H., and N. C. Lee, *Assembly and Reliability of Lead-Free Solder Joints*, Springer, New York, 2020.
7. Lau, J. H., *Heterogeneous Integrations*, Springer, New York, 2019.
8. Lau, J. H., *Fan-Out Wafer-Level Packaging*, Springer, New York, 2018.
9. Lau, J. H., *3D IC Integration and Packaging*, McGraw-Hill, New York, 2016.
10. Lau, J. H., *Through-Silicon Via (TSV) for 3D Integration*, McGraw-Hill, New York, 2013.
11. Lau, J. H., *Reliability of RoHS compliant 2D & 3D IC Interconnects*, McGraw-Hill, New York, 2011.
12. Lau, J. H., C. K. Lee, C. S. Premachandran, and Yu Aibin, *Advanced MEMS Packaging*, McGraw-Hill, New York, 2010.
13. Lau, J. H., C. P. Wong, N. C. Lee, and R. Lee, *Electronics Manufacturing with Lead-Free, Halogen-Free, and Adhesive Materials*, McGraw-Hill, New York, 2003.
14. Lau, J. H., and R. Lee, *Microvias for Low Cost, High Density Interconnects*, McGraw-Hill, New York, 2001.
15. Lau, J. H., *Low Cost Flip Chip Technologies for DCA, WLCSP, and PBGA Assemblies*, McGraw-Hill, New York, 2000.
16. Lau, J. H., and R. Lee, *Chip Scale Package: Design, Materials, Process, Reliability, and Applications*, McGraw-Hill, New York, 1999.
17. Lau, J. H., C. P. Wong, J. Prince, and W. Nakayama, *Electronic Packaging: Design, Materials, Process, and Reliability*, McGraw-Hill, New York, 1998.
18. Lau, J. H., and Y. Pao, *Solder Joint Reliability of BGA, CSP, Flip Chip, and Fine Pitch SMT Assemblies*, McGraw-Hill, New York, 1997.
19. Lau, J. H., (editor) *Flip Chip Technologies*, McGraw-Hill, New York, 1996.
20. Lau, J. H., (editor) *Ball Grid Array Technology*, McGraw Hill, New York, 1995.
21. Lau, J. H., (editor) *Chip On Board Technologies for Multichip Modules*, Van Nostrand Reinhold, New York, March 1994.
22. Lau, J. H., (editor) *Handbook of Fine Pitch Surface Mount Technology*, Van Nostrand Reinhold, New York, 1994.
23. Lau, J. H., (editor) *Thermal Stress and Strain in Microelectronics Packaging*, Van Nostrand Reinhold, New York, 1993.
24. Lau, J. H., (editor) *Handbook of Tape Automated Bonding*, Van Nostrand Reinhold, New York, November 1992.
25. Lau, J. H., (editor) *Solder Joint Reliability: Theory and Applications*, Van Nostrand Reinhold, New York, April 1991.

**Thank You Very Much for Your
Attention!**

