

# ESTC PDC

## Flip-Chip Interconnect

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## Instructor: Eric Perfecto

ERIC PERFECTO (IEEE M'95, SM'01, F'17) has extensive experience working in microelectronics. At IBM, Eric led the development of RDL multi-level Cu-polyimide advanced packages for high-end systems, introduced of Pb-free solder interconnects and worked on 2.5D wafer finishing. Eric moved to GLOBALFOUNDRIES Si Photonics packaging development line. In 2019 he returned to IBM part time to establish a heterogeneous integration line in Albany including a new line for solder electroplating. He holds a M.S. in Chemical Engineering from the University of Illinois and a M.S. in Operations Research from Union College.

An author of more than 80 technical papers and three book chapters, Eric received two Best Conference Paper Awards (2006 ESTC and 2008 ICEPT-HDP) and the 1994 Prize Paper Award from CPMT Trans. on Adv. Packaging. He holds 55 US patents and has been honored with two IBM Outstanding Technical Achievement Awards.

Eric served as the 57th ECTC General Chair, the 55th ECTC Program Chair and is the current ECTC Publicity chair. For 12 years, Eric's popular Flip-Chip Fabrication and Interconnection course has been given at ECTC to great reviews. He is an EPS Distinguish Lecturer, an IEEE Fellow, and has achieved IMAPS and SPE senior membership.

Eric has represented the EPS members previously, elected 4 times to the BoG. For 3 years he served as the EPS Strategic Director of Global Chapters and Membership where he focused on enhancing the EPS membership value. For 8 years, he was the EPS Awards Program Director. Currently, Eric is the EPS Education V.P. At a local level, Eric is the membership Chair of the Mid-Hudson IEEE Section and the EPS Mid-Hudson EPS Chapter .



# Flip-Chip Interconnect

This PDC aims to provide a comprehensive overview of Flip-Chip technologies, including fabrication processes, materials, history, and assembly methods.

Part 1: Introduction to Flip-Chip Technologies

Part 2: UBM and Solder Deposition Methods

Part 3: Pattern Electroplating

Part 4: Cu-Pillar Fabrication and Applications

Part 5: Solders, Electromigration and Reliability

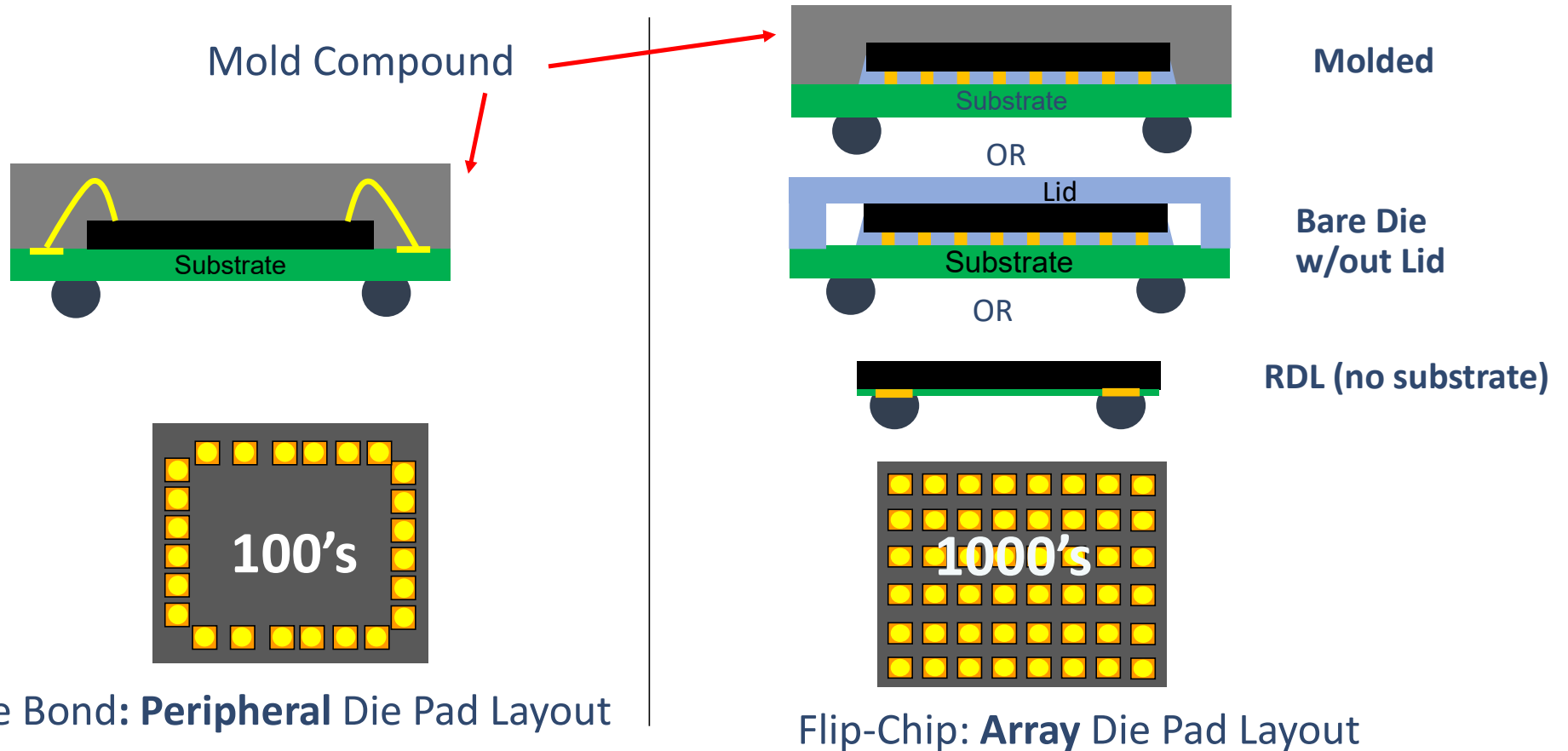
# Flip-Chip Interconnect

## Part 1: Introduction to Flip-Chip Technologies

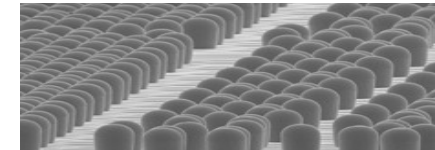
Part 1 provides a foundational understanding of flip-chip packaging, its terminology, and how it differs from traditional wire-bonding. It introduces the joining principles thru mass-reflow, thermal-compression, and hybrid-bonding assembly, including how flux, underfill, and intermetallic formation enable reliable solder or Cu-pillar joints.

- Key Topics:
- Introduction to Flip-Chip Technologies and Terminology
  - Wire Bonding vs Flip-Chip
  - Flip-Chip Joining by Mass Reflow Process
  - Flux and Underfill
  - Flip-Chip Joining by Thermal Compression
  - Flip-Chip Joining by Hybrid Bonding

# Flip-Chip and Wire Bond : Die Design



# Flip-Chip vs Wire Bond Comparison



|                              | Wire Bonding                              | Flip-Chip (Solder Bump)                                  |
|------------------------------|-------------------------------------------|----------------------------------------------------------|
| <b>Cost per die</b>          | <b>Lowest</b> (cheapest packaging method) | Higher (substrate + bumping + underfill)                 |
| <b>I/O Density</b>           | ~100–600 I/O typical                      | <b>Up to 5,000+ I/O</b> (u-bump: 10,000+)                |
| <b>Pitch</b>                 | 50–100 $\mu\text{m}$ wire pitch           | <b>150–20 <math>\mu\text{m}</math> bump pitch</b>        |
| <b>Electrical Inductance</b> | High (1–3 nH per wire)                    | <b>Very low</b> (50–200 pH per bump)                     |
| <b>Signal Speed</b>          | Limited (good for <1–2 GHz)               | <b>Excellent</b> (tens of GHz)                           |
| <b>Power Delivery</b>        | Moderate                                  | <b>Superior</b> (low IR drop, low L)                     |
| <b>Thermal Path</b>          | Poor – Chip backside on substrate         | <b>Excellent</b> (chip backside on lid or heat spreader) |
| <b>Reliability</b>           | Very high for low-stress apps             | <b>High</b> (underfill and CTE dependent)                |
| <b>Substrate Cost</b>        | <b>Low</b> (leadframe or simple laminate) | High (high-density substrate required)                   |
| <b>Package Size</b>          | Larger footprint                          | <b>Smallest footprint</b>                                |
| <b>Assembly Complexity</b>   | <b>Low</b>                                | High (bumping, reflow, underfill)                        |
| <b>Application</b>           | Analog, power, sensors, low-I/O MCUs      | <b>High-performance SoCs, RF, GPUs, CPUs, HBM</b>        |

# First Level Packaging

## Chip- 1st level interconnect

C4(solder) + Underfill

1st level packages  
organic, ceramic

1st-2nd level interconnect

Heat sinks

Cu, Al, complex design

Heat spreaders

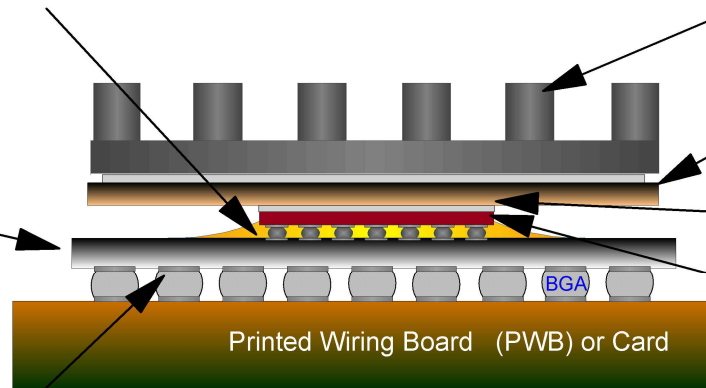
passive, active

Thermal Interface

Materials

paste, gels, metals

**Chip**

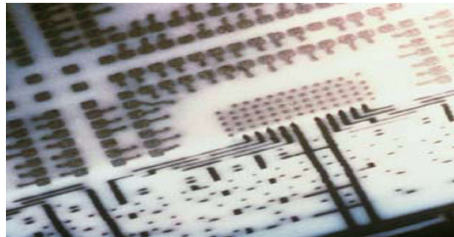


Chip

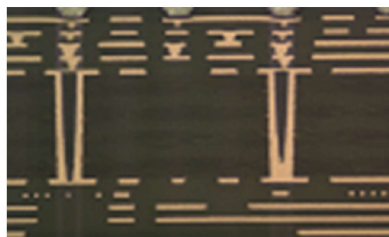
Carrier

Options:

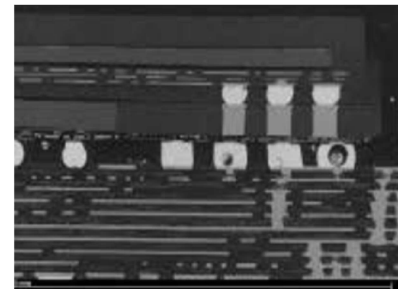
Ceramic



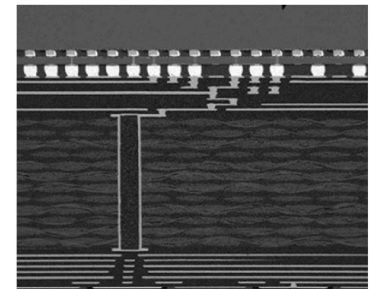
Laminates



Wafer Level Pkg



Interposer +  
Laminate



# Highlights of Flip-Chip (FC) History

Early 1960's – IBM soldered Cu u-ball between Solid Logic Transistors to ceramic substrate – the very first Flip-Chip assembly with only three bumps.

1964 – IBM introduced C4: Controlled-Collapse Chip Connection. It was the first fully reflowed solder interconnection.

1984 – Hitachi introduced flip-chip underfill – larger die size on ceramic substrate become common.

1989 – IBM Japan's Tsukada introduced first underfilled flip-chip device on organic substrate. It is instrumental for wide adoption of flip-chip from 1990's.

From 1960's to early 2000's – solder bump alloys were Lead based solders: 95PbSn or 97PbSn or 63PbSn (excellent Thermal fatigue performance).

**From middle of 2000's – bump alloys were gradually switched to Lead Free solder and Cu-pillar + lead free solder. Fully switched over to lead free from 2016 per EU requirement with minor exceptions. Pb-free consisted mainly of Sn with small Ag and Cu, known as SAC solder.**

# Solder Intermetallic

## C4 = Controlled Collapse Chip Connection

Back End of Line (BEOL) Wiring

Polymer Cushion

Underfill

Under Bump Metallization

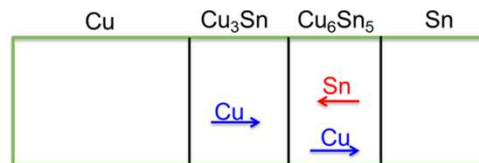
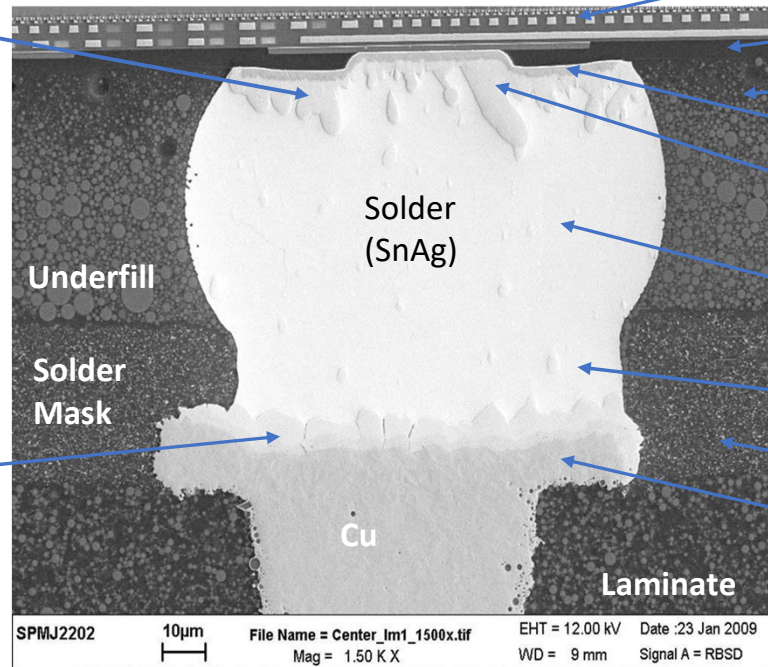
Intermetallic

C4 Solder

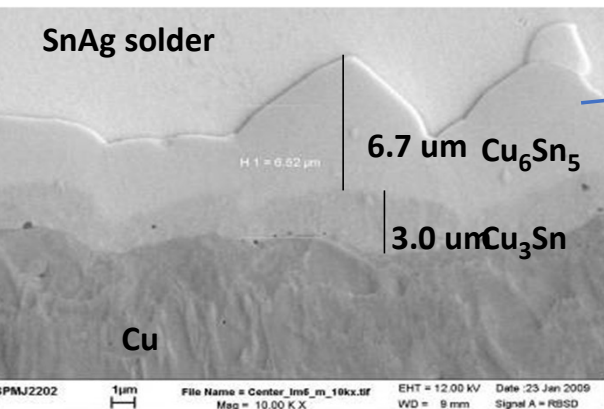
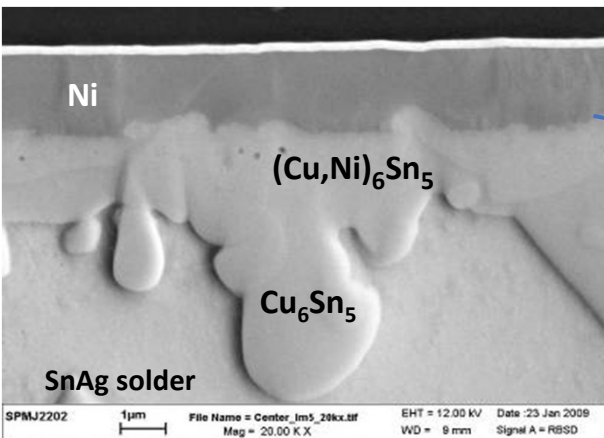
Laminate pre-solder

Solder mask

Laminate Pad/wiring

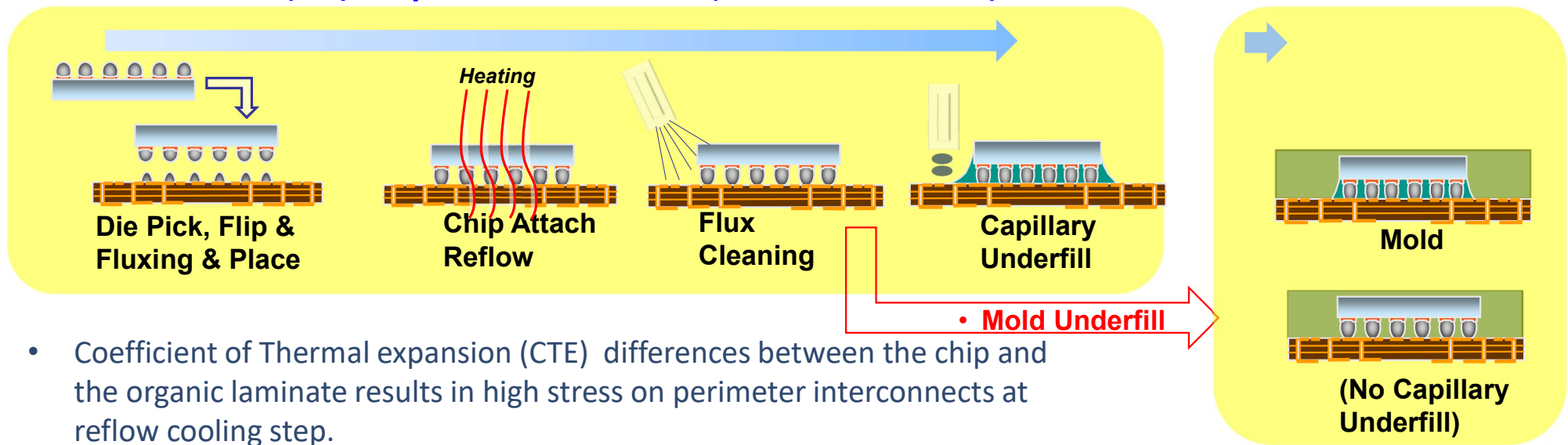


With Ni UBM the formed IMC is Ni<sub>3</sub>Sn<sub>4</sub>



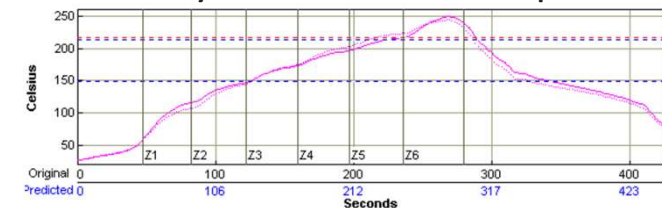
# Mass Reflow Assembly Process Steps

## Mass Reflow (MR) Chip Attach & Underfill (Solder or Cu-Pillar)



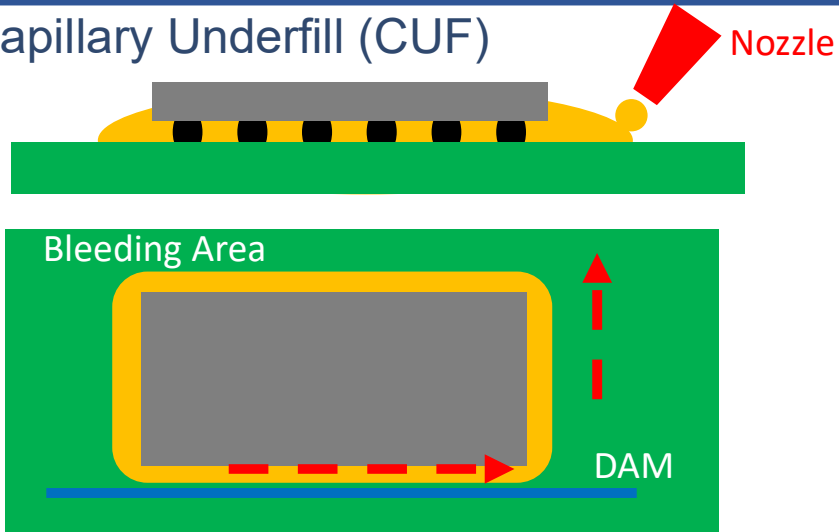
- Coefficient of Thermal expansion (CTE) differences between the chip and the organic laminate results in high stress on perimeter interconnects at reflow cooling step.
- Underfill fills the gap between chip and substrate, distributes stress from CTE mismatch:
  - Improves shock / vibration resistance
  - Reduces solder fatigue. Could extend solder connect lifetime by 2X.

Conveyorized belt reflow profile

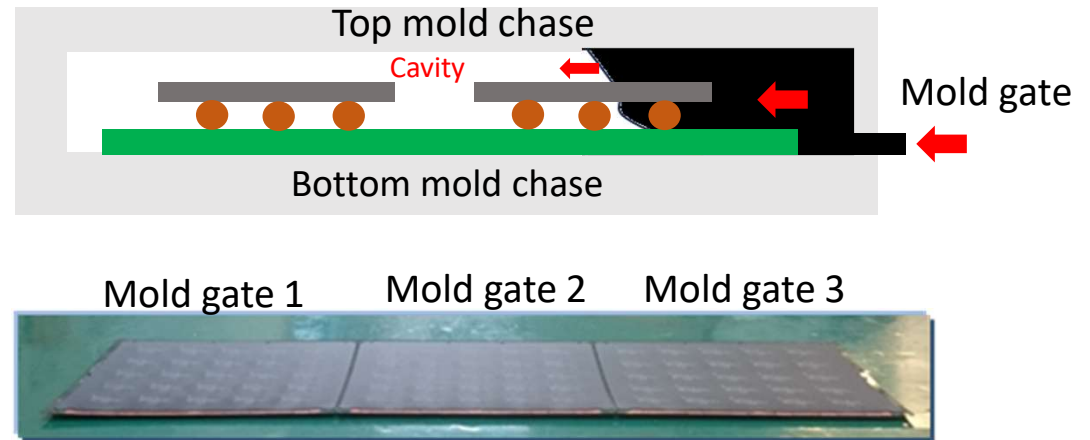


# Underfill Processes

## Capillary Underfill (CUF)



## Mold Underfill (MUF)

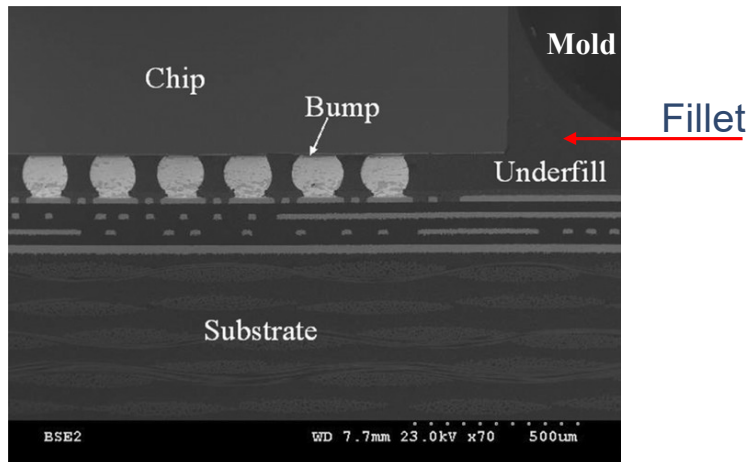


Key underfill parameters

|                               | Typical EMC | Typical Underfill |
|-------------------------------|-------------|-------------------|
| CTE1 (ppm, T)                 | 10 – 15     | 20 – 40           |
| CTE2 (ppm, T>T <sub>g</sub> ) | 30 – 45     | 80 – 120          |
| T <sub>g</sub> (°C, DMA)      | 140 – 170   | 80 – 165 (190)    |
| Filler size (um)              | 10 – 50     | 0.3 – 10          |
| Youngs Moduli (GPa)           | 15 – 25     | 5 – 17            |

# Underfill – CUF/MUF

## Capillary Underfill (CUF)



## Mold Underfill (MUF)

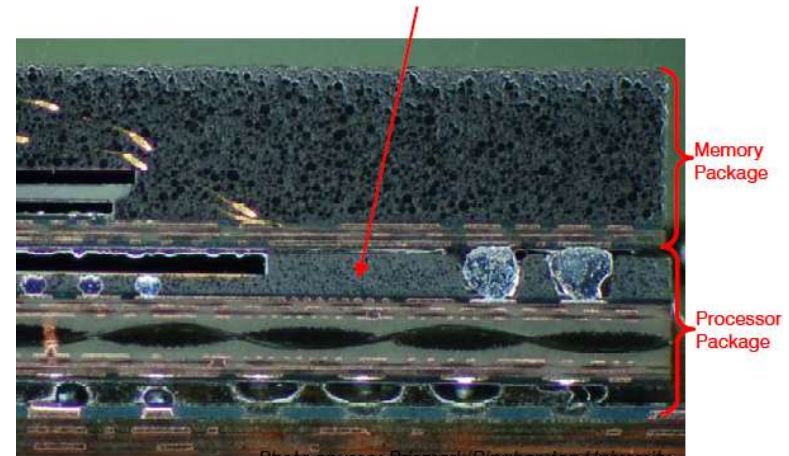
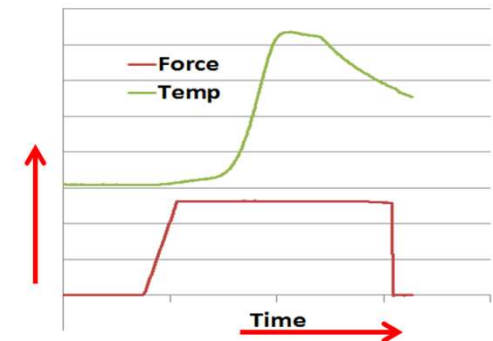
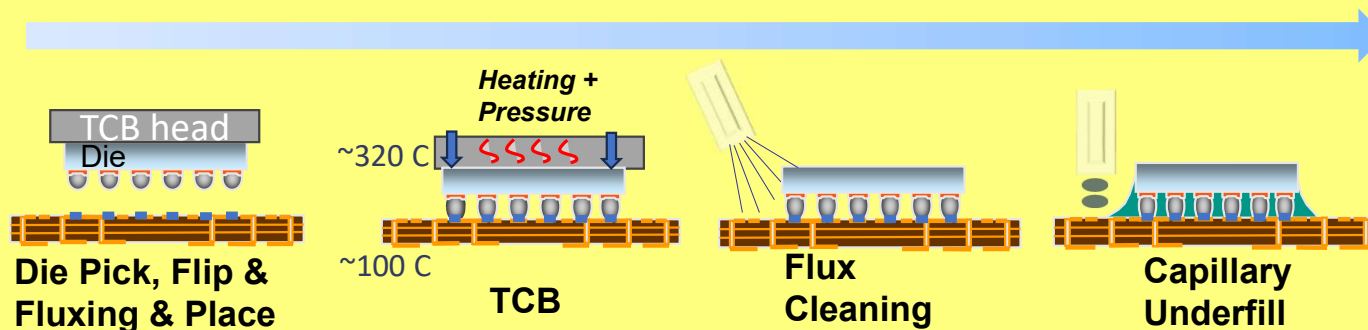


Photo source: Prismark/Binghamton University

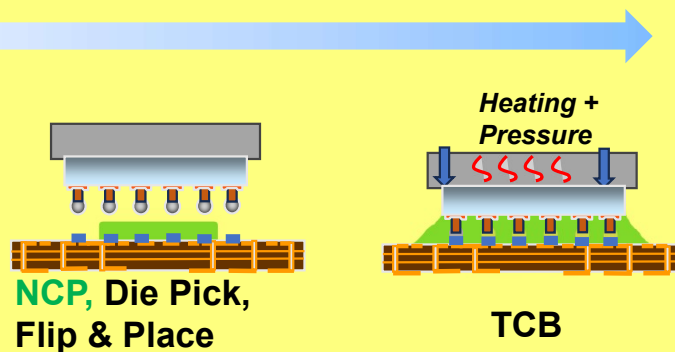
K. M. Chen, "Comparing the Impacts of the Capillary and the Molded Underfill Process on the Reliability of the Flip-Chip BGA," *IEEE Trans. Comp. Pack. Tech*, Vol 31, No 3, 2008.

# Thermal Conduction Bonding (TCB)

## TCB Chip Attach & Underfill for Fine Pitch (Cu-Pillar) Interconnect



## TCB Chip Attach w/NCP



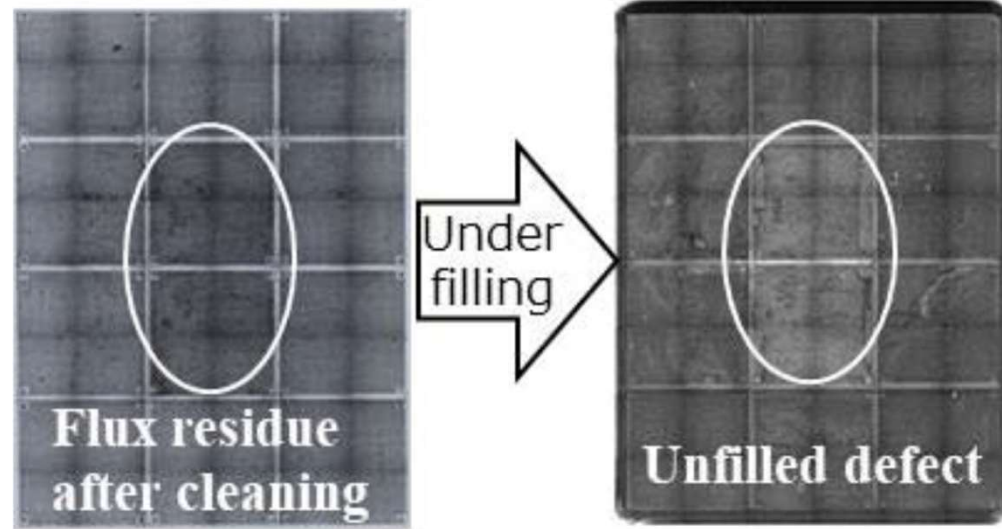
- TCB process is one die at a time.
- TCB combines precision die placement and reflow in one step.
- Non conductive Polymer (NCP) serves as a flux clean and as underfill. It requires Cu-Pillars.
- As the interconnect pitch decreases, formic acid treatment prior to TCB eliminates the need of Flux and Clean.

# Effect of Residual Flux in Underfill Delamination

Issue: Flux removal on tight pitch joints is very difficult to clean with flux residues causing underfill voids or underfill poor adhesion.

Sonoscan images:

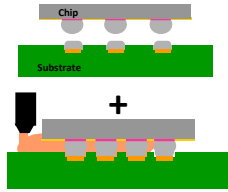
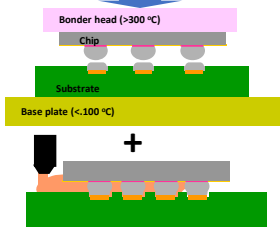
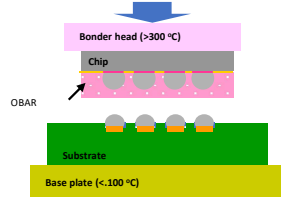
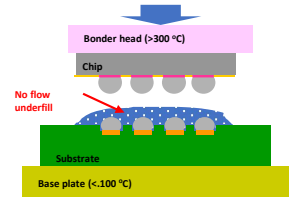
Top die: Cu / Ni / SnAg  
Interposer: Cu UBM



Solution: Implement a Formic Acid pretreatment prior to TCB

Sadaaki Katoh, et al, "Development of Fluxless Micro-Bonding and Narrow Gap Filling Process," 2023 ECTC

# Underfill Processes Comparison

|            | Reflow + Capillary                                                                                                                                                                                           | Diff. Heating/Cooling (TCB)                                                                                                                                                  | Wafer NCF (TCB)                                                                                                                                                                                    | Non-Conductive Paste (TCB)                                                                                                                                                    |
|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Technology |                                                                                                                             |                                                                                            |                                                                                                                 |                                                                                            |
| Advantage  | <ul style="list-style-type: none"> <li>No need big tooling investment.</li> <li>Industry standard</li> <li>Self alignment during solder joining.</li> </ul>                                                  | <ul style="list-style-type: none"> <li>Reduced CTE mismatch between die and laminate during assembly.</li> <li>Dicing &amp; alignment are same as reflow process.</li> </ul> | <ul style="list-style-type: none"> <li>TCB minimizes CTE mismatch effects.</li> <li>Lowest assembly C4s stress</li> <li>Enabled by Cu-pillar</li> <li>No need of flux / clean</li> </ul>           | <ul style="list-style-type: none"> <li>NCF advantages</li> <li>Dicing &amp; alignment are same as reflow process.</li> </ul>                                                  |
| Concerns   | <ul style="list-style-type: none"> <li>Laminate and chip CTE mismatch is high at reflow.</li> <li>u-Bump Cleaning flux residue</li> <li>Capillary underfill time &amp; small voids in fine pitch.</li> </ul> | <ul style="list-style-type: none"> <li>Single chip bonder w formic acid</li> <li>Capillary underfill time &amp; small voids.</li> </ul>                                      | <ul style="list-style-type: none"> <li>Wafer dicing w/ NCP or NCF</li> <li>Die Alignment through NCP.</li> <li>Underfill voids elimination requires vacuum laminator and pressure cure.</li> </ul> | <ul style="list-style-type: none"> <li>Underfill life-time after dispensing before joining.</li> <li>Filler trapped between bumps.</li> <li>Pressure cure required</li> </ul> |

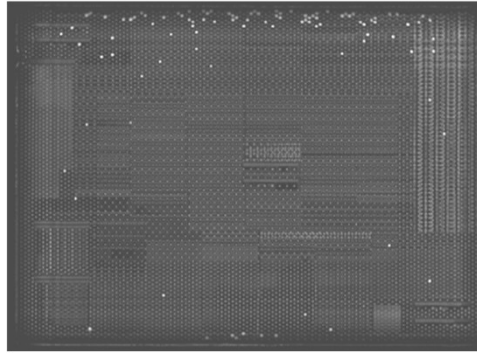
# NCP Assembly Implementation

## NCP with TCB Eliminates the white bump defect

Sonoscan  
defect 1:

White dots →  
BEOL crack  
failure

Reflow with slow cooling



Thermal compression bonding with NCP

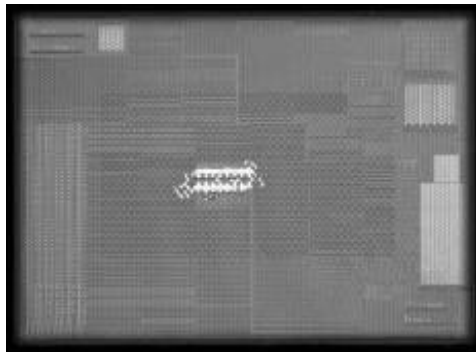


## Hydrostatic pressurized cure eliminates underfill voids

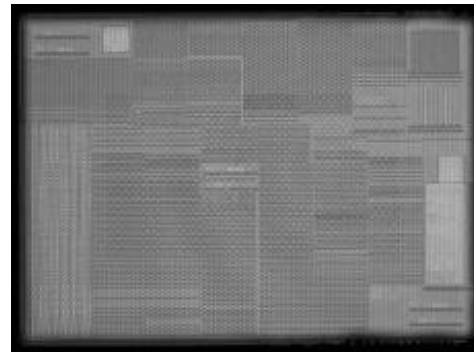
Sonoscan  
defect 2:

Voids → Air  
entrapment

• After pressure cure under 2 atm



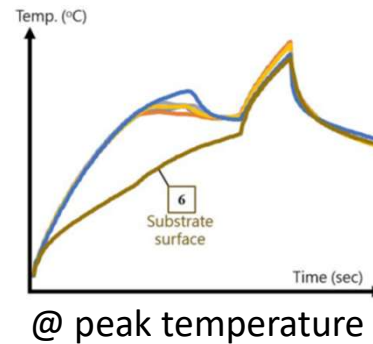
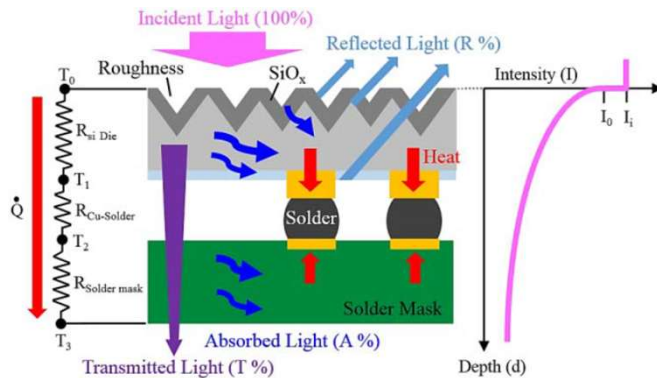
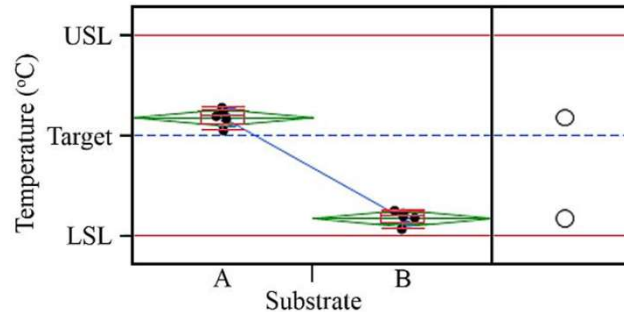
• After pressure cure under 4 atm



JW Nah, et al, "Wafer Level Underfill for Area Array Cu Pillar Flip-Chip Packaging of Ultra Low-k Chips on Organic Substrates," 2012 ECTC

# Laser Assisted Bonding (LAB) Temperature Uniformity

LAB laminate temperature is depended on the substrate reflectivity. This can result in varied temperatures in the die, ie. Center vs edge



| Technology |               | MR                                                                     | TCB               | LAB                |                               |
|------------|---------------|------------------------------------------------------------------------|-------------------|--------------------|-------------------------------|
|            |               |                                                                        |                   |                    |                               |
| Process    | Heat transfer | Heat source                                                            | Heat blast        | TCB Head           | Photothermal Conversion       |
|            |               | Thermal conduction                                                     | Die/Sub.          | Die                | Die/Sub.                      |
|            |               |                                                                        | Cu Pillar         | Cu Pillar          | Cu Pillar                     |
|            |               | Melting                                                                | Solder welding    | Solder welding     | Solder welding                |
|            | Reflow time   | ~4 min                                                                 | 20 sec / pcs      | < 3 sec / pcs      |                               |
|            | Thermal budge | High                                                                   | Middle            | Low                |                               |
|            | Stress        | Heating zone/time                                                      | Die & Sub. / Long | Die & Sub. / Short | Die & Sub. local / Very short |
|            |               | CTE no match                                                           | Die & Sub.        | Die & Sub.         | Die & Sub. local              |
|            |               | Die / Sub. Warpage                                                     | Large             | Middle             | Low                           |
|            |               | Stress                                                                 | High              | Middle             | Low                           |
| Defect     |               | 1. Solder (crack, wicking)<br>2. Chip damage (Node failure, ELK crack) | Solder (crack)    | No                 |                               |
| Quality    | IMC Thk. (μm) | < 10                                                                   | < 5               | < 2                |                               |

# Chip Pull Testing Failure Modes

## Purpose

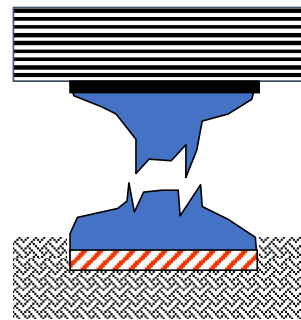
- Destructive test to check for process robustness and stability misplacement errors
- Chip is attached to the organic carrier and pulled with an Instron tool. Fail interface and pull strength is examined.

## Sample Chip Pulls (destructive)

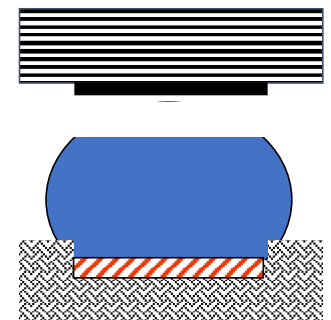
- Verify solder wetting;
- Verify non-contact fails
- Large I/O chips require proper chip pull set up (support substrate to prevent erroneous results) due to the high force

## Failure modes

In the solder



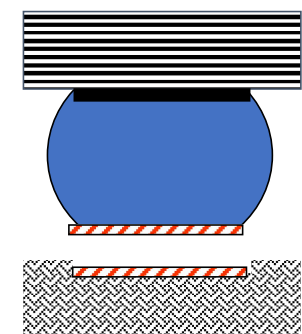
Within the UBM



In the BEOL



At the Intermetallic

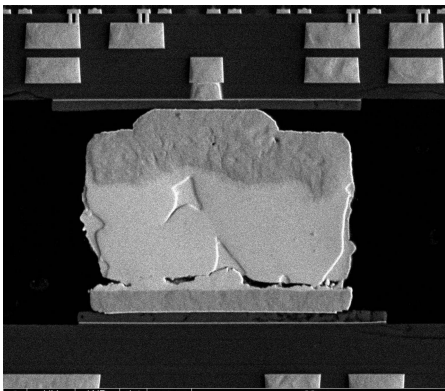


## u-Pillar Joining Defects , continue

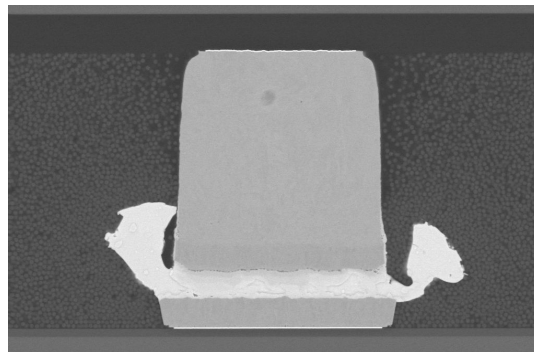
### Joining Defect:

1. Residual Sn at Joining
2. Pad contaminant preventing full wetting
3. Excessive TCB force
4. Mis-alignment

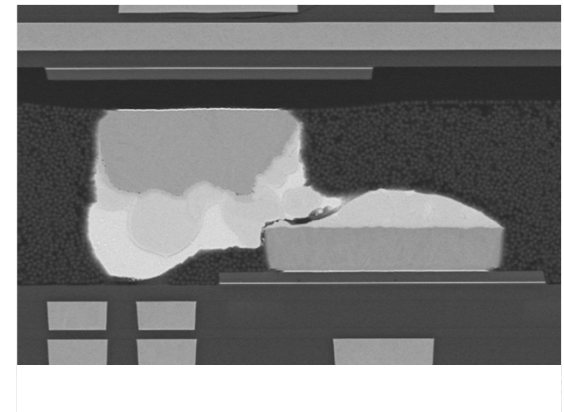
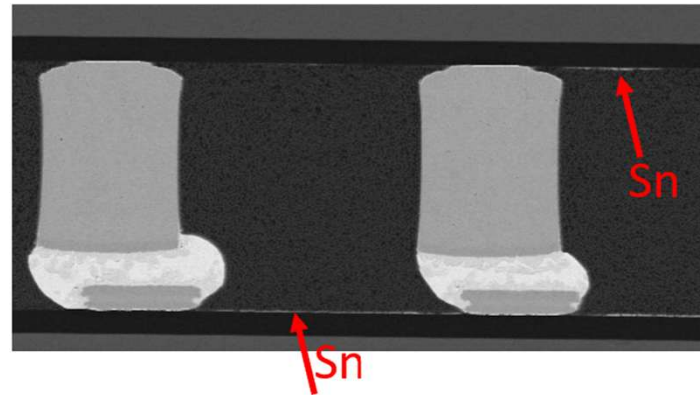
Defect 2



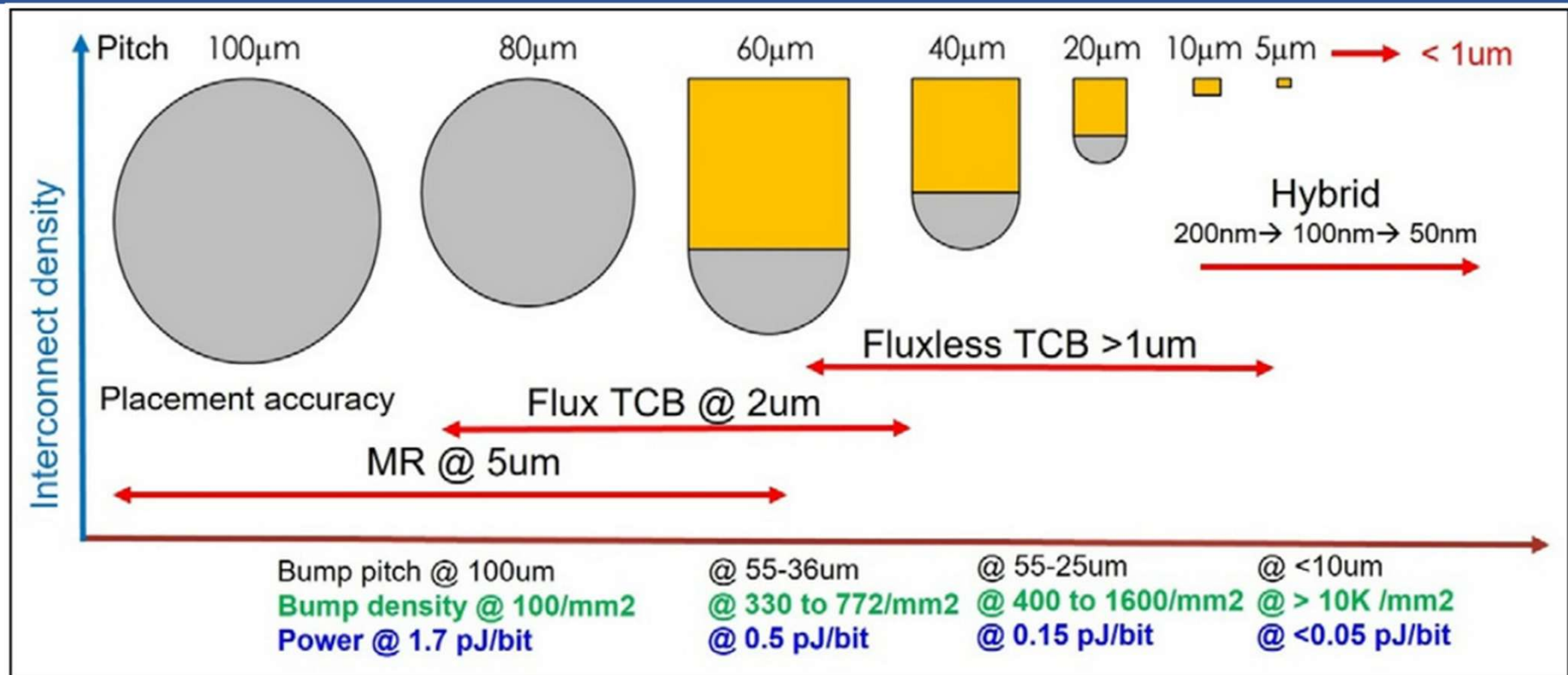
Defect 3



Defect 1



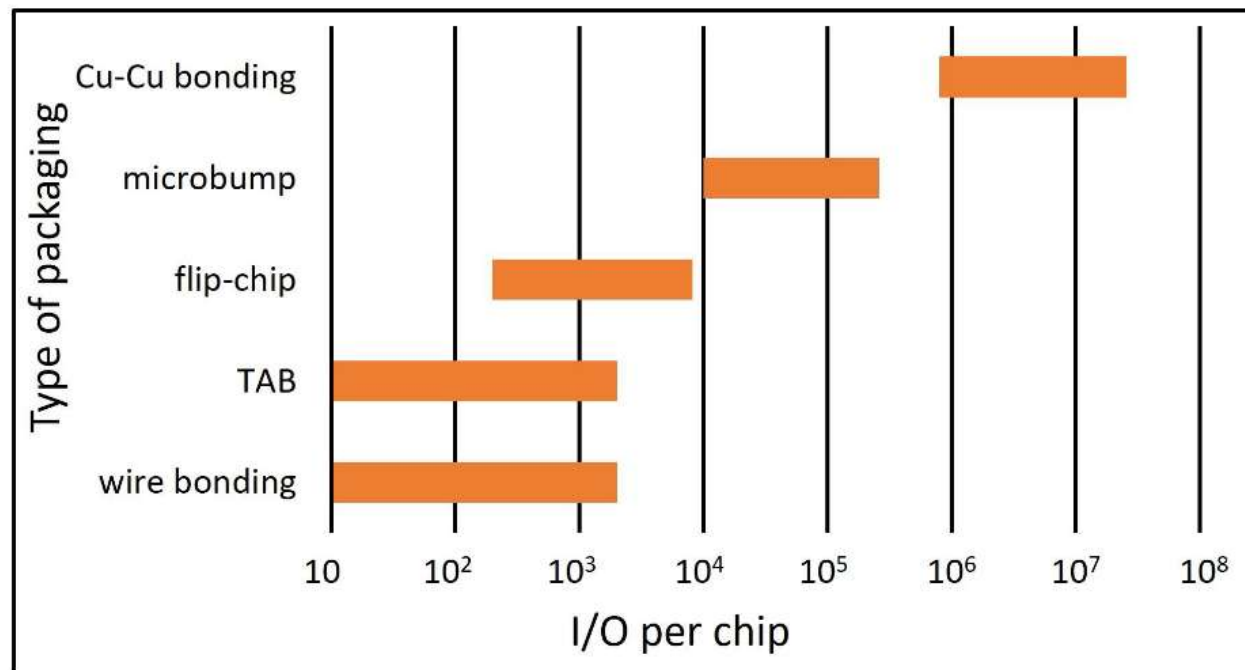
# Flux vs Fluxless , MR vs TCB Guideline



\* Fluxless refers to no flux. Here Formic clean or wet Acid clean can be used just prior to bonding. Another option is No-Clean flux (but it may have adhesion/reliability issues) or NCP.

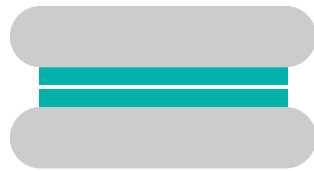
# Packaging Scaling

**Cu-Cu bonding has become the 5<sup>th</sup> generation Chip-Connection Technology**



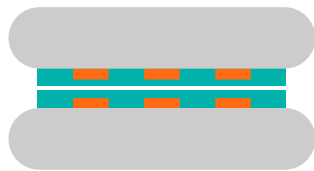
Electronic Packaging Science and Technology, King-Ning Tu, Chih Chen, H.M. Chen, Wiley 2021.

# Types of Wafer – to - Wafer Bonding



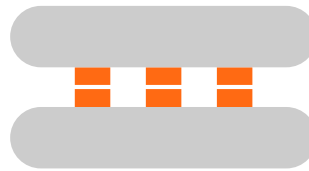
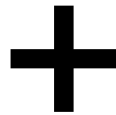
## Fusion Bonding

- Dielectric bonding
- Van der Waals → Covalent
- Mechanical connection
- Non-Patterned wafers



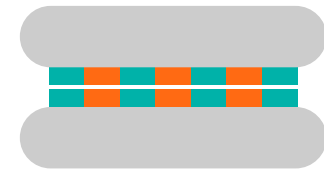
## Fusion Bonding

- Patterned wafers



## Metal Bonding

- Cu bonding
- Thermal compression (TC)
- Electrical connection
- Patterned wafers



## Hybrid Bonding

- Dielectric + Cu bonding
- Covalent + TC
- Mechanical + Electrical connection
- Patterned wafers

### Possible defects:

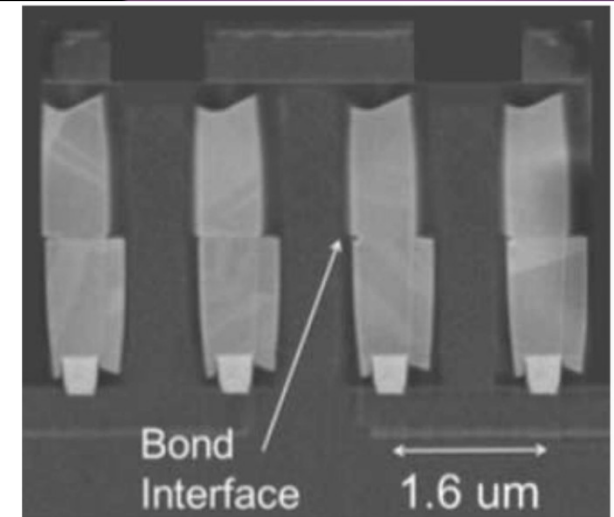
- Alignment Error
- Cu Voids
- Dielectric Voids
- Distortion
- Contamination induced defects

# Hybrid Bonding Process



Hybrid bonding is a Si to Si interconnect. Initially started at Wafer level with Sony camera but new die to wafer applications are currently surfacing.

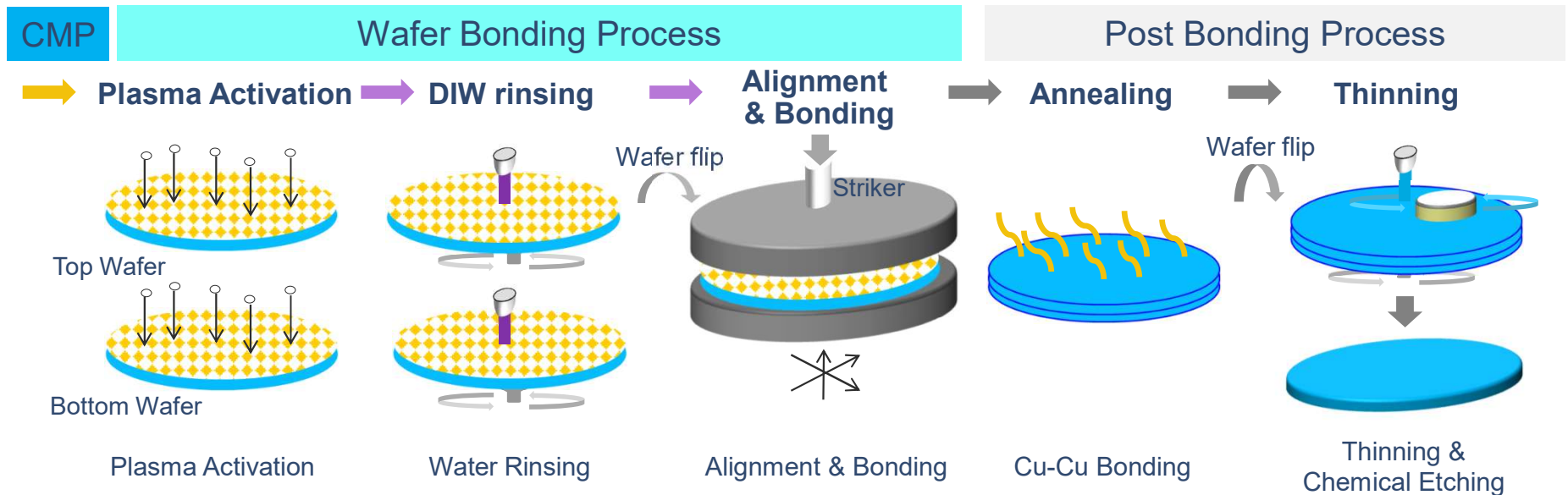
Main issues are contamination, Cu recess, surface treatment, TCB accuracy and voids. The process works best at <10  $\mu\text{m}$  pitch and joined diameter of  $\leq 5\mu\text{m}$  since it relies on tight control the recessed Cu gap.



<https://4sense.medium.com/hybrid-bonding-technologies-info-f547fd0dc7c5>,

L. Wang, et al., "Direct Bond Interconnect (DBI®) for fine-pitch bonding in 3D and 2.5D integrated circuits," 2017 Pan Pacific Microelectronics Symposium

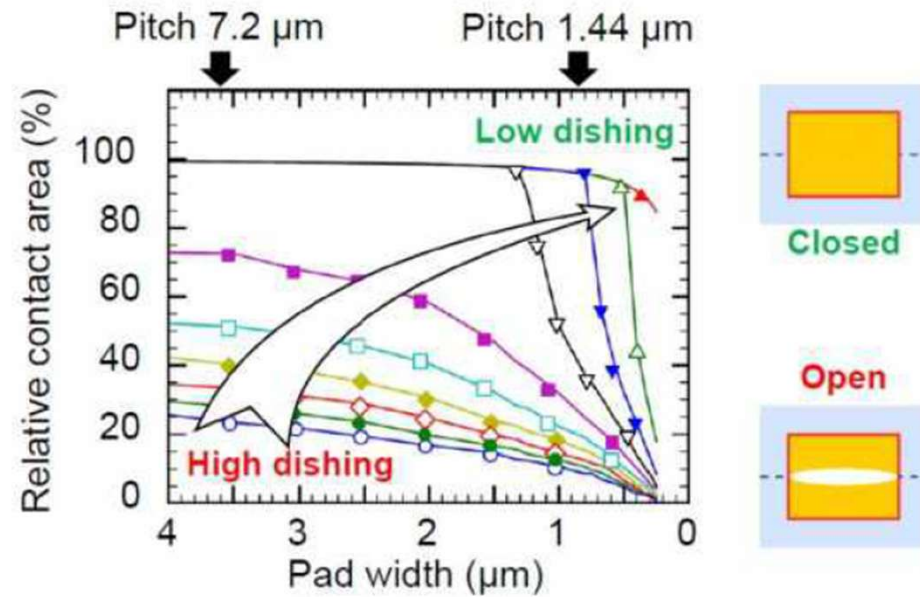
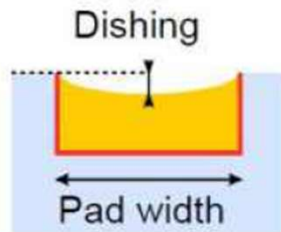
# Bonding Process Flow



- The quality of the bonding surface is mediated by the pre-bond processes of CMP, plasma activation and H<sub>2</sub>O rinsing
- After the wafers are bonded the anneal will condense the dielectric bonds and copper expansion will make contacts between the metal pads on each wafer in hybrid bonding.

# Cu Dishing

Simulation of Cu/Cu interface closure at 400 °C



The smaller the pad diameter the less dishing during the CMP process.

→ Mixed pad diameter or pitch not recommended.

# Alignment and Total Overlay Measurement

## Measured Data

Displacement  $(x_i, y_i)$

**Conversion**

**4 Parameter Model**

## Calculated Data

Translation  $(x,y)$  + Scaling + Rotation



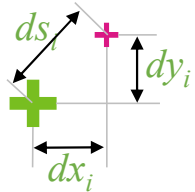
Residual  $(x,y)$

Linear component (Recipe input) –  
correction or compensation

Non-linear component  
(Incoming, HW)



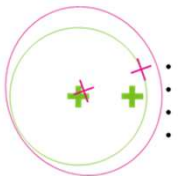
Misalignment



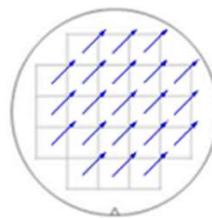
Alignment/ overlay  
mark on top wafer



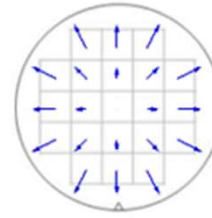
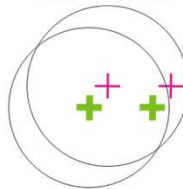
Alignment/ overlay  
mark on Bottom wafer



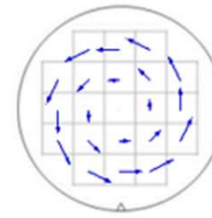
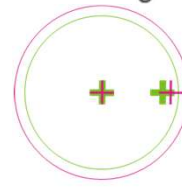
- $ds_{max} \neq 0$ ,
- $Tx \neq 0, Ty \neq 0$
- Rotation  $\neq 0$
- Scaling  $\neq 0$



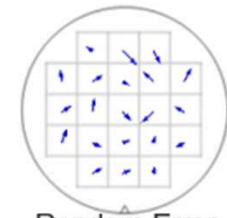
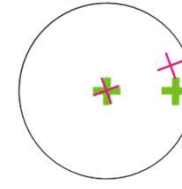
Translation



Scaling



Rotation



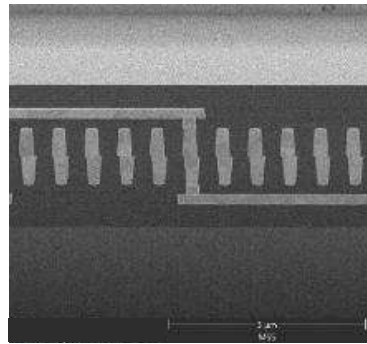
Random Error  
Residual (Distortion)

Source: Netzband, C. IEEE ECTC 2023

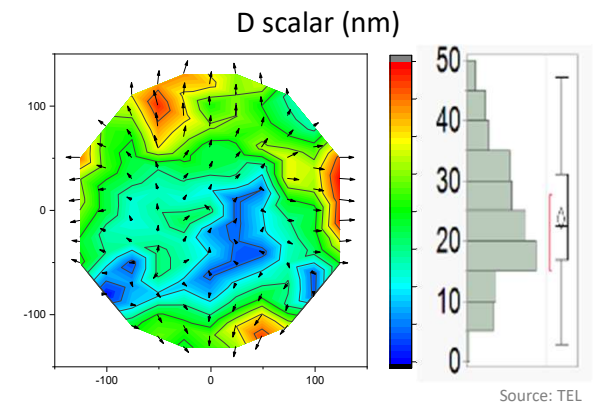
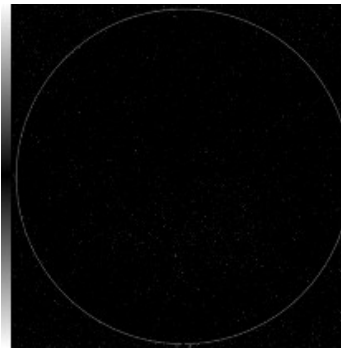
# 0.5 $\mu\text{m}$ Narrow Pitch Hybrid Bonding at TEL

Industry-first demonstration of void free bonding of 0.5 $\mu\text{m}$  pitch with  $D_s < 50\text{nm}$  across 100% of the wafer (<40nm across 90%)

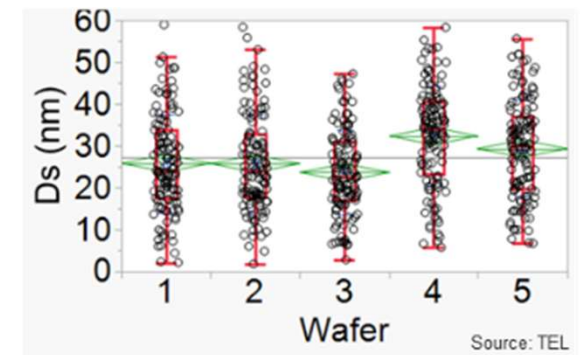
This alignment was stable across multiple wafers run without changes to the tool



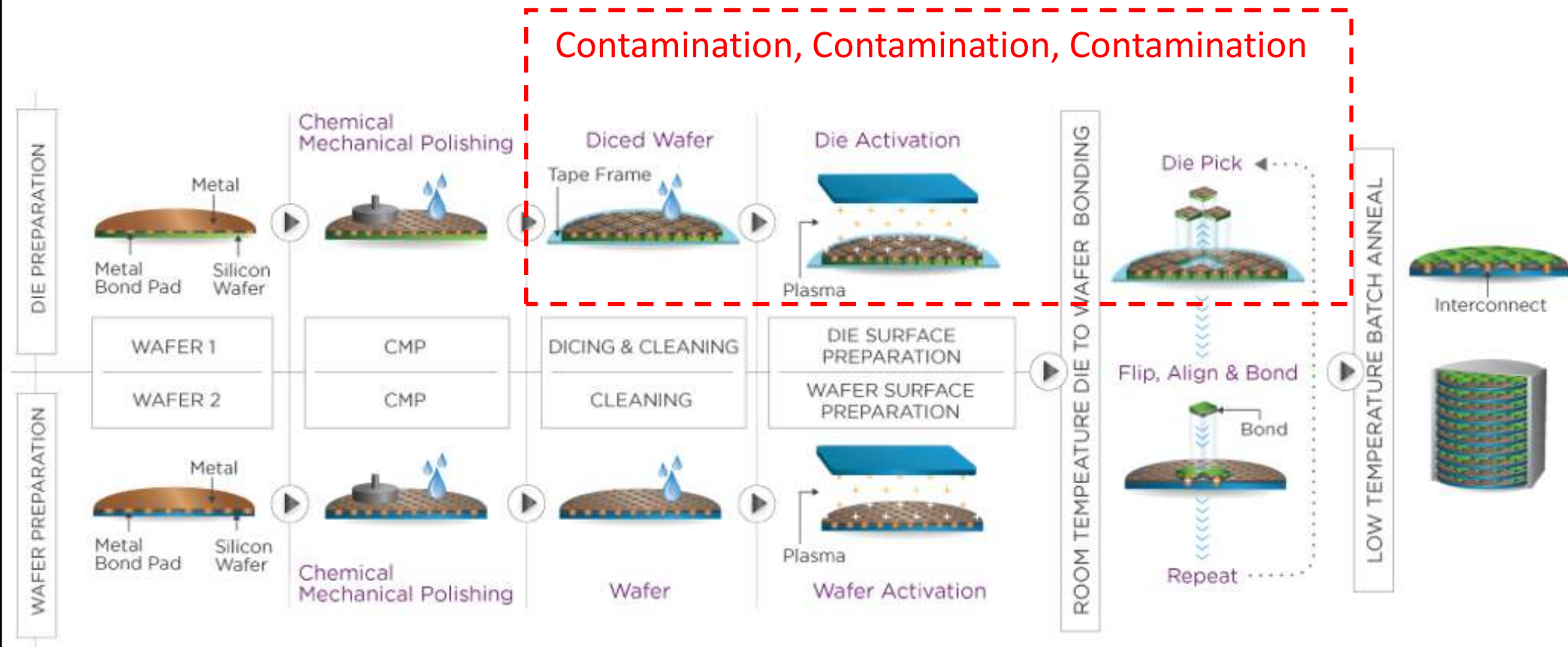
Source: Netzband, C. IEEE ECTC 2023



| TEL | D scalar (nm) |      | Residual scalar (nm) |      |
|-----|---------------|------|----------------------|------|
|     | 100%          | 90%  | 100%                 | 90%  |
|     | 47.2          | 37.6 | 37.9                 | 23.3 |



# Hybrid Bonding: D2W

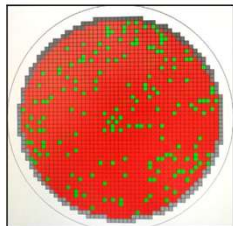


# D2W: Dicing protective Layer

## Dicing Protective layer

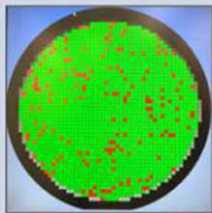
- Ensures that dicing debris does not contaminate the Cu/Dielectric surface.

No Protective layer



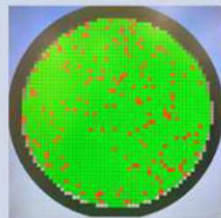
9.7% Yield

Photo-definable liquid film

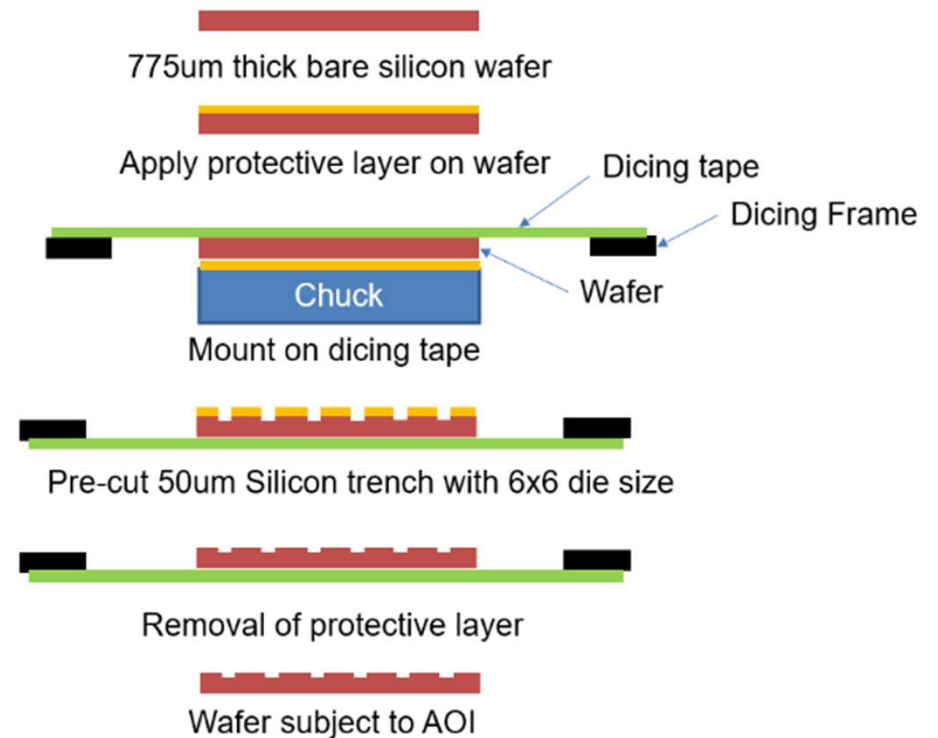


90.9% Yield

Non Photo-definable liquid film

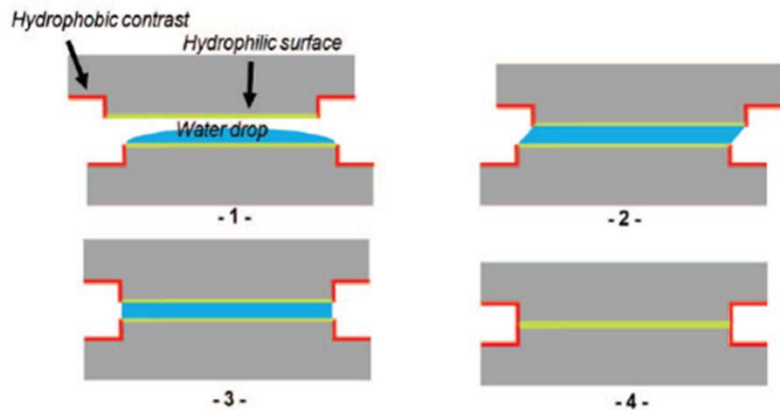


90.73% Yield

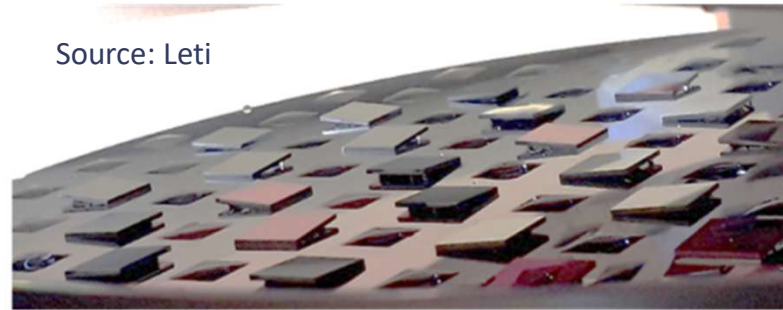


S. Choong, et. al, "Yield Improvements in Chip to Wafers Hybrid Bonding," 2022 ECTC

# Hybrid Bonding D2W Fast Alignment



Source: Leti



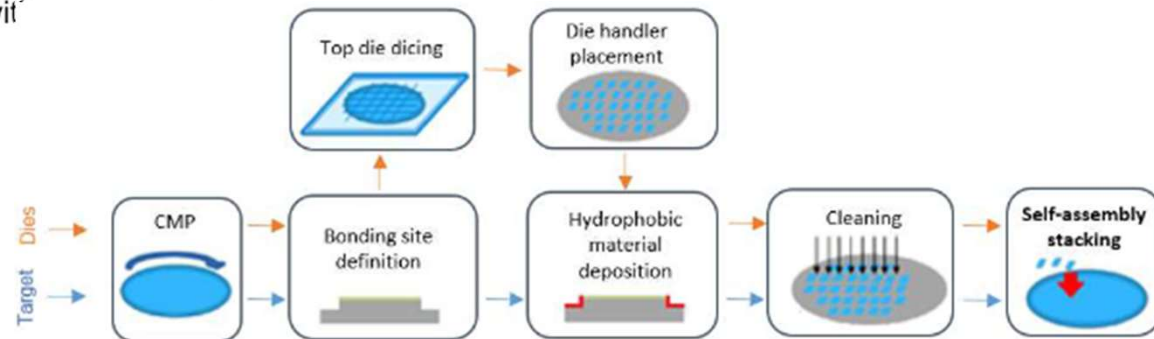
u-Pipet is able to control droplets placement and volume



The different steps of self-assembly process

1. Inaccurate pre-alignment ( $>200\ \mu\text{m}$ )
2. Drop spreading and chip is realigned with submicron accuracy (around  $400\text{nm}$ )
3. Drop evaporation
4. Direct bonding

Collective bonding by self-assembly  
Dies deposited on water droplet



A. Bond, et al., "Collective Die-to-Wafer Self-Assembly for High Alignment Accuracy and High Throughput 3D Integration," 2022 ECTC

# AMD Example: Hybrid Bonding + u-Pillars + Std C4

## AMD INSTINCT™ MI300 FAMILY

### 3.5D Advanced Packaging Elements

Unique Thermal architecture  
→ ~750W TDP

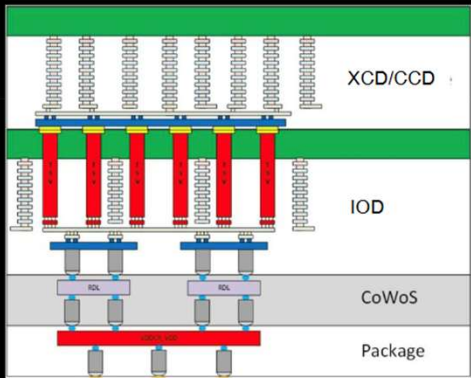
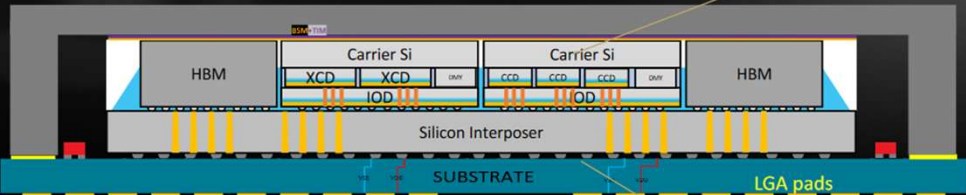
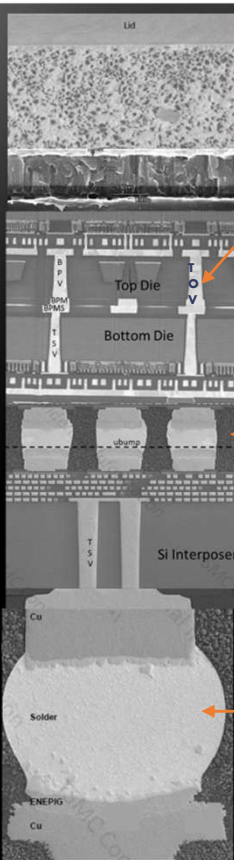


Illustration purposes only

Advanced 3D Hybrid Bonding → Compute density and perf/W

Advanced 2.5D Arch → Ultra high BW IOD-IOD and HBM3 integration

Large module Attach on Advanced 2D Substrate



TOV (or Through Oxide Via) for chip-to-chip interconnect

u-Pillar for chip-to-Si interposer interconnect

Cu-pillar for interposer to substrate interconnect

AMD  
together we advance

Sam Naffziger, HIR Symposium, "Future of AI Hardware Enabled by Advanced Packaging," 2024 ECTC

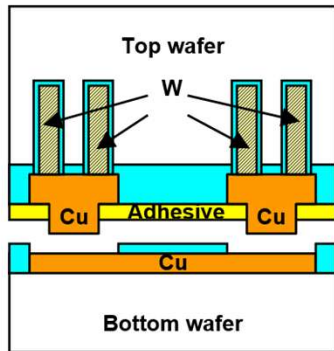
# Chip Joining Methods Comparison

Tradeoffs, Applications, and Selection Criteria:

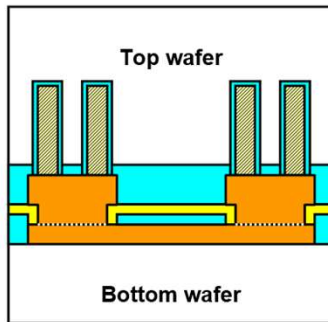
| Parameter / Metric        | C4<br>(Standard Flip-Chip)            | Cu-Pillar (u-bump)                   | TCB (Thermal<br>Compression Bonding) | Hybrid Bonding (DBI)                   |
|---------------------------|---------------------------------------|--------------------------------------|--------------------------------------|----------------------------------------|
| Interconnect Material     | Solder Ball (SnAg)                    | Cu-Pillar + Solder Cap               | Cu-Pillar + Solder Cap               | Direct Cu-to-Cu & SiO <sub>2</sub>     |
| Typical Pitch Range       | 90 $\mu\text{m}$ – 150+ $\mu\text{m}$ | 40 $\mu\text{m}$ – 100 $\mu\text{m}$ | 10 $\mu\text{m}$ – 40 $\mu\text{m}$  | < 0.5 $\mu\text{m}$ – 10 $\mu\text{m}$ |
| I/O Density               | Low                                   | Moderate                             | High                                 | Ultra-High                             |
| Underfill Method          | Capillary (CUF)                       | Capillary or Molded                  | NCP /NCF                             | None (Fluxless)                        |
| Relative Assembly<br>Cost | Lowest                                | Low to Moderate                      | Moderate to High                     | Highest                                |
| Primary Advantage         | High throughput                       | Better thermal path                  | Controls thin die warping            | Near-zero parasitics                   |
| Primary Drawback          | Solder bridging risk                  | Stresses low-k dies                  | Low tool throughput                  | Particle sensitive                     |
| Target Application        | Legacy CPUs, PMICs                    | Mobile APs, Mid GPUs                 | HBM3/HBM4 stacks                     | AI accelerators                        |

# Cu-Cu/Polymer-SiO<sub>2</sub> Hybrid Bonding

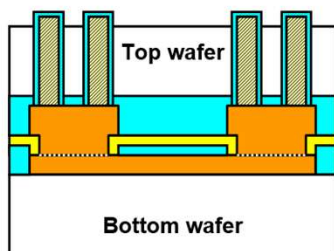
(a) Top/Bottom Wafers



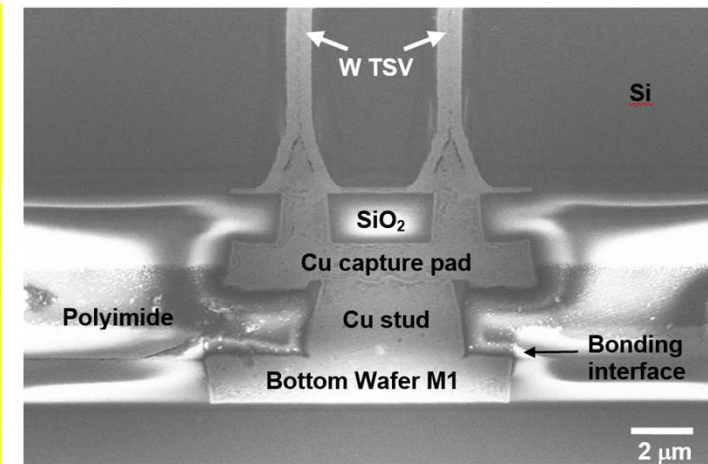
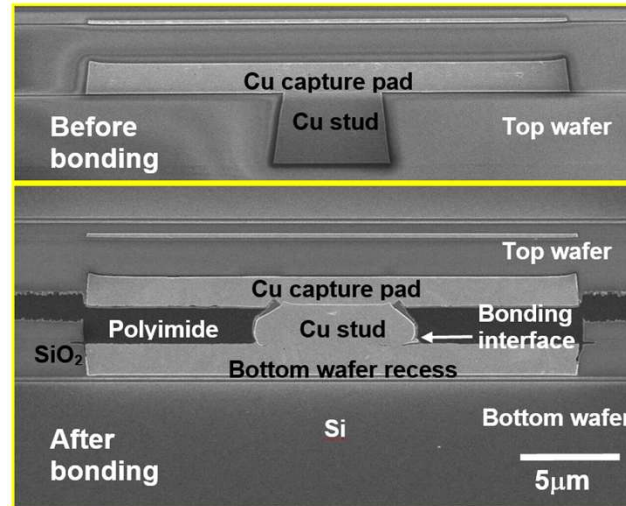
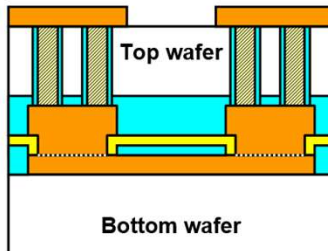
(b) Bonding



(c) Thinning



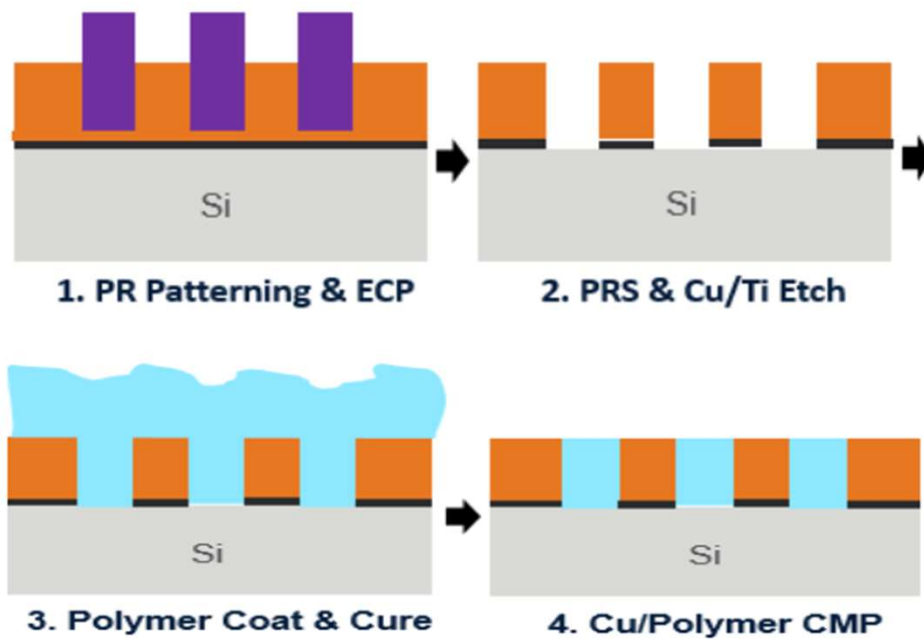
(d) Backside



Wafer to wafer bonding utilizing Cu/Polyimide on Top wafer and Cu/SiO<sub>2</sub> on bottom wafer in a “lock and Key” structure.

Cu/Polymer-SiN hybrid bonding requires more time in TCB tool since it needs polymer flow and Cu-Cu join during bonding.

# Cu/Polymer Hybrid Bonding – In Development



Cu/Polymer hybrid bonding is less sensitive to contamination causing bonding defect.

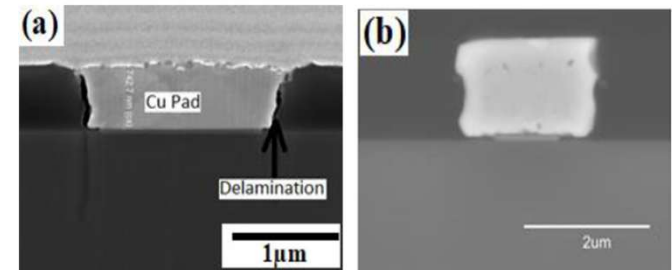


Fig. 5. Polymer CMP (a) Cu pad sidewall delamination (b) No sidewall delamination with improved CMP process.

FullVision® endpoint technique was used to achieve accurate remaining polymer thickness with reduced stress imposed on the Cu sidewall after Cu reveal.

# Part 1: Introduction to Flip-Chip Technologies Summary

## Why Flip-Chip?

- ✓ Ultra-high I/O density (5,000+; u-bump >10,000)
- ✓ Fine pitch (150–20  $\mu\text{m}$ )
- ✓ Very low inductance (50–200 pH) → high-speed signaling
- ✓ Superior thermal path & smallest footprint
- ✓ Enables Heterogeneous Integration – needed for advanced packages

## Key Interconnect Processes

- **Mass Reflow (MR):** Flux → reflow joining → flux clean → bake → capillary underfill
- **Thermal Compression Bonding (TCB):** Precision placement + heat + pressure
- **Hybrid Bonding:** oxide-to-oxide + Cu-to-Cu ; no solder; enables <10  $\mu\text{m}$  pitch & 3D stacking

## Materials & Reliability

- Flux improves wetting, removes oxides; residues must be cleaned
- Underfill manages CTE stress, warpage, toughness
- NCP can replace Flux and Underfill processes for fine pitch Cu-Pillar joining
- Intermetallic secures solder joining; Cu-Sn ( $\text{Cu}_6\text{Sn}_5$ ,  $\text{Cu}_3\text{Sn}$ ); Ni UBM →  $\text{Ni}_3\text{Sn}_4$

# Flip-Chip Interconnect

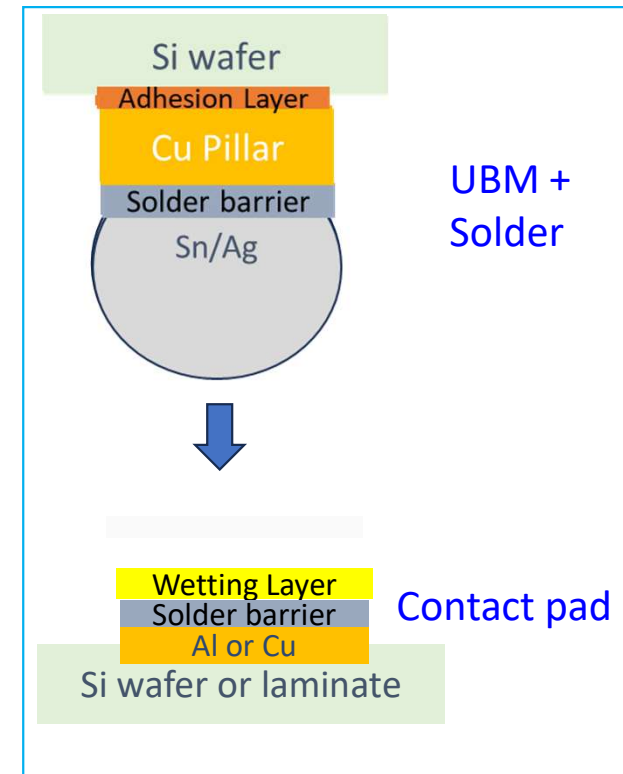
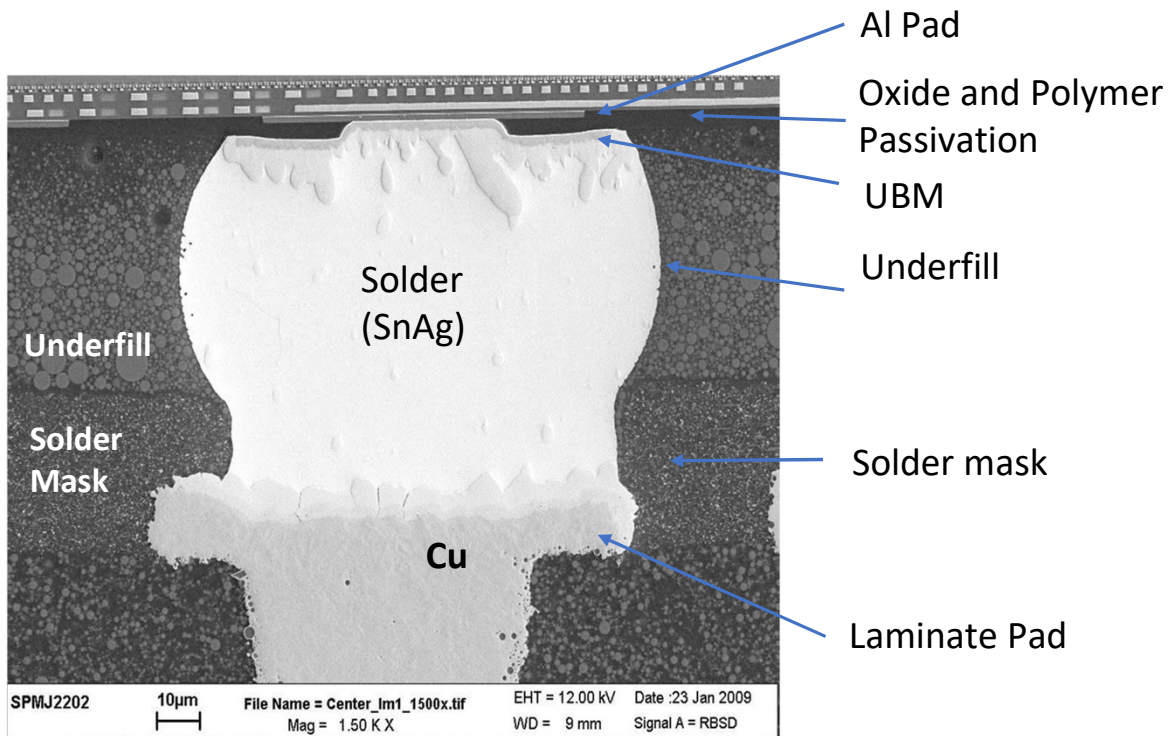
## Part 2: UBM and Solder Deposition Methods

Part 2 details the structure and function of under-bump metallurgy, including adhesion, barrier, and wetting layers, and issues such as  $\text{Ni}_3\text{P}$  formation and Black Pad. It will compare major solder-deposition methods—ball drop, stencil printing, electroplating, C4NP, laser bumping, Au stud, and ACA—and learn when each is best applied.

- Key Topics:
- Under-Bump Metal (UBM) and Intermetallic
  - Flip-Chip Solder Deposition Processes

# Solder Join Elements

## C4 = Controlled Collapse Chip Connection

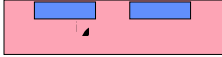
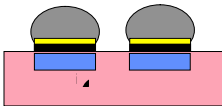


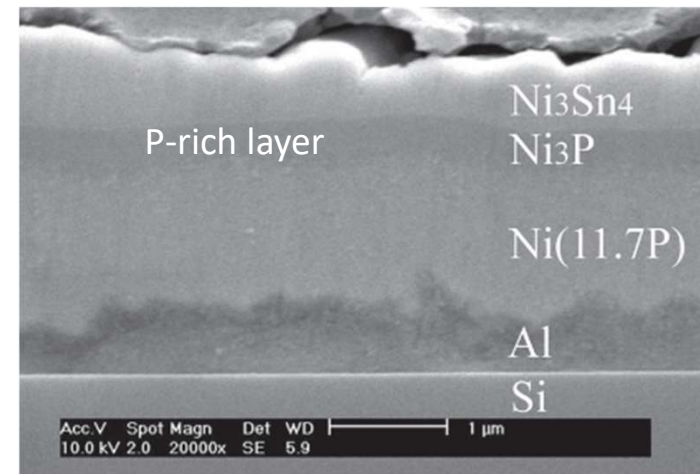
Solder provides (power and signal) electrical connectivity from the laminate to the chip.

# UBM Function

- UBM provides the connection between the solder and device, and between the solder and chip carrier.
- UBM provides a reliable solder joint to withstand electrical, thermal, mechanical and environmental stressing.
- UBM has 3 layers with unique functions
  - **Adhesion Layer** – Provides adhesion to Polyimide and Oxides:
    - Ti, TiW, Cr, Al
  - **Solder Barrier Layer** - Creates the solder metallurgical connection
    - Prevents/slows undesirable interdiffusion of metal layers
    - Ni, NiX for Pb and Si Based solder, or Co or thick Cu
  - **Wetting Layer** – Provides solder wetting
    - Au, Cu

# Electroless Ni(P) UBM

| Electroless Ni(P) Etch Process                            |                                                                                    |
|-----------------------------------------------------------|------------------------------------------------------------------------------------|
| Incomming Substrate<br>Ceramic or Organic laminate        |  |
| Electroless Ni(P) + Au<br>High Temp Diffuse               |  |
| Solder Deposition by<br>Solder Screen, C4NP, Ball<br>Drop |  |



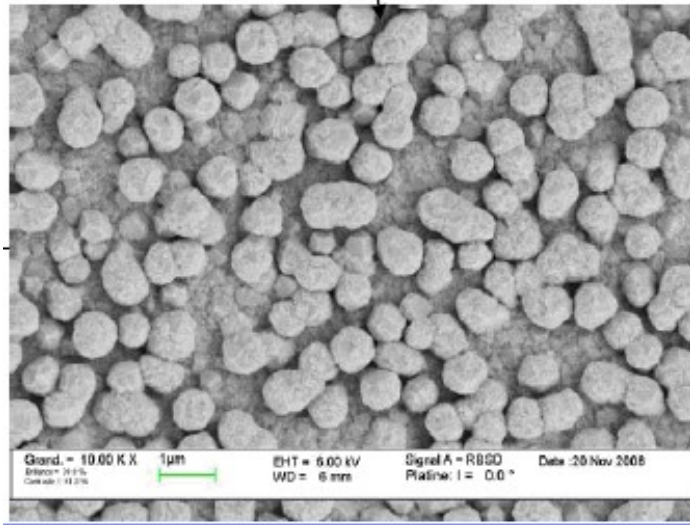
Electroless Ni(P) is practiced mainly on Organic and Ceramic substrate with incoming Cu surface.

- Ni(P)/Au is used for Flip-Chip application on the laminate bottom side for Ball Grid Array (BGA) or Land Grid Array (LGA) connection.

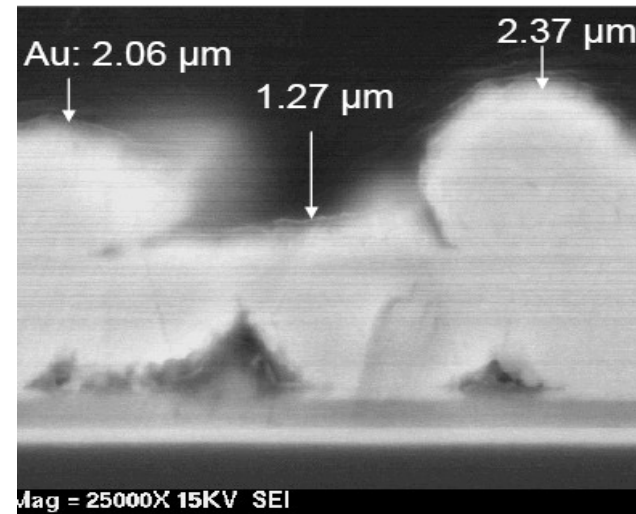
Ni(P) has the same problem as NiV, NiW and NiSi: A crystalline  $\text{Ni}_3\text{P}$  forms when the Ni diffuses and reacts with the solder to form  $\text{Ni}_3\text{Sn}_4$  intermetallic - known as reaction-assisted crystallization.

# Immersion Au Control

Top View



X-section

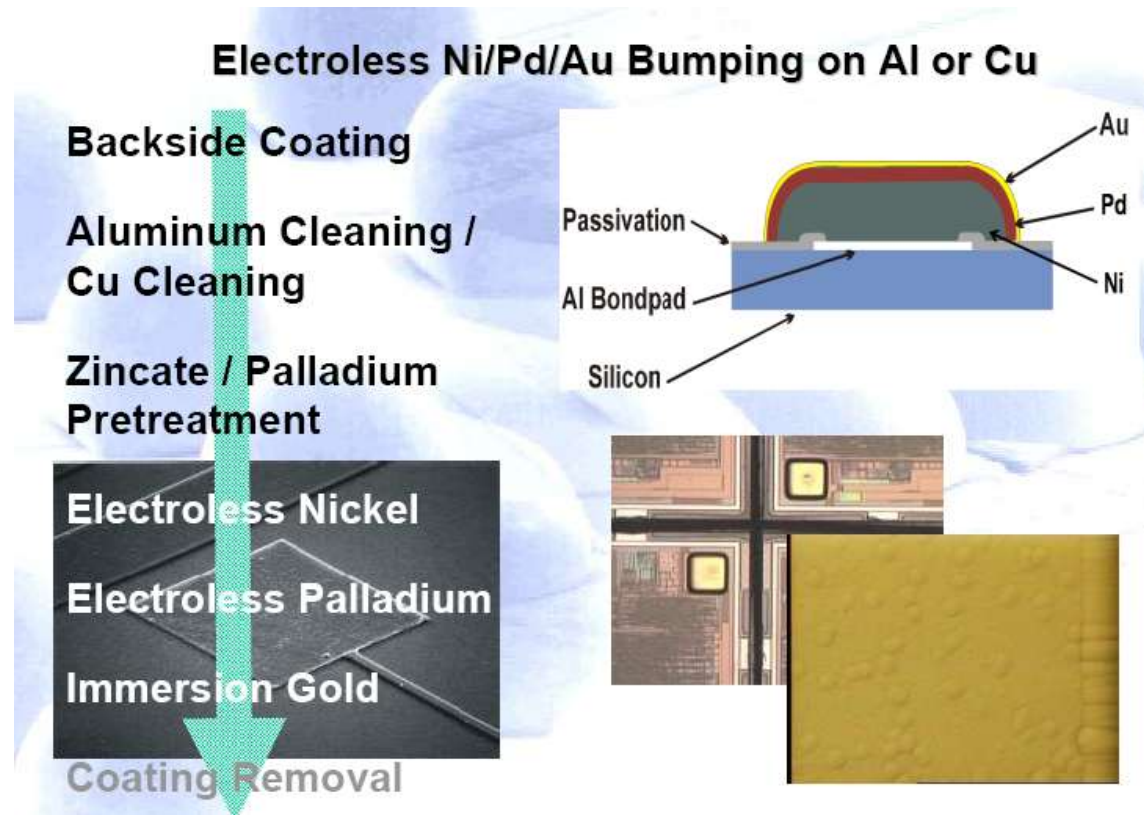


“Black Pad” problem can occur when Imm Au plating attacks or corrodes the Ni(P) surface.

Root Cause:

- Oxidized / Non-uniform incoming Ni surface
- Poor Imm Au chemistry control

# Addition of Palladium Between Ni and Au

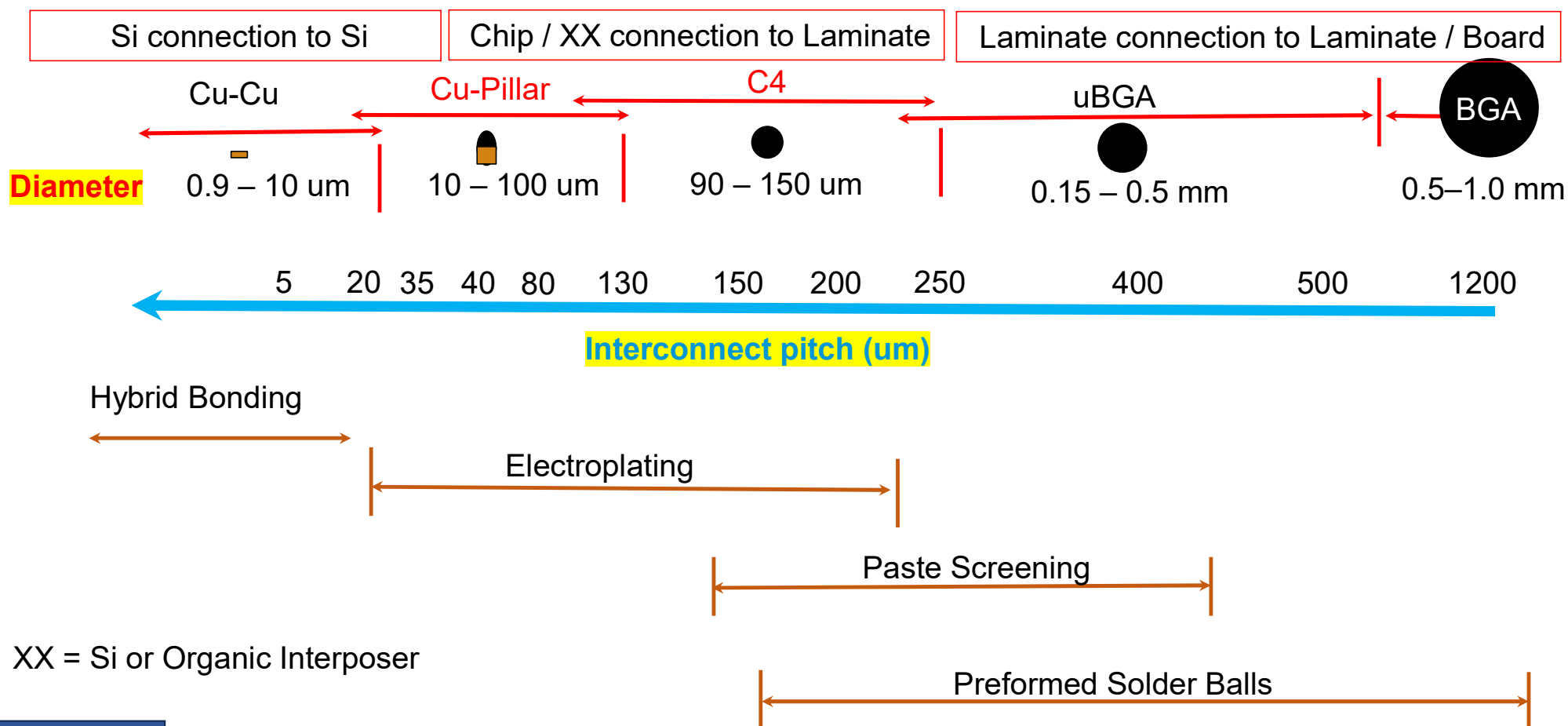


PacTech developed robust process for UBM on laminate substrates

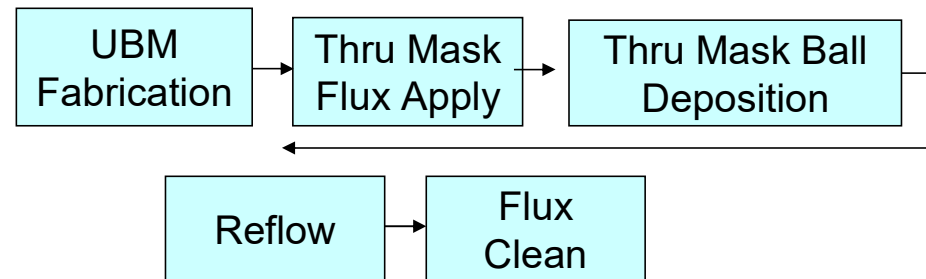
# UBM: Barrier Fabrication and Options

- There are two main fabrication Methods: Pattern electroplating or Electroless deposition:
  - **Pattern electroplating**
    - Thich Cu, Ni, or Ni with top Cu
    - Other element reported in the literature are Co, Fe, or NiCo, NiFe or NiCu
  - **Electroless Deposition**
    - Ni(P) or Ni(P) + Palladium with Immersion Au (ENIPIG)
    - Ni(Boron) practiced by IBM on ceramic substrates - needs high diffusion temp.
  - **Others: Subtractive etching of sputtered film**
    - Ni, NiV, NiSi, NiW, NiTi, NiZn
    - Subtractive etching is not practical since Au wetting surface needs to be deposited after etching since barriers layers have high oxidation levels.

# Bumping Method Selection



# Ball Drop: Direct Ball Deposition



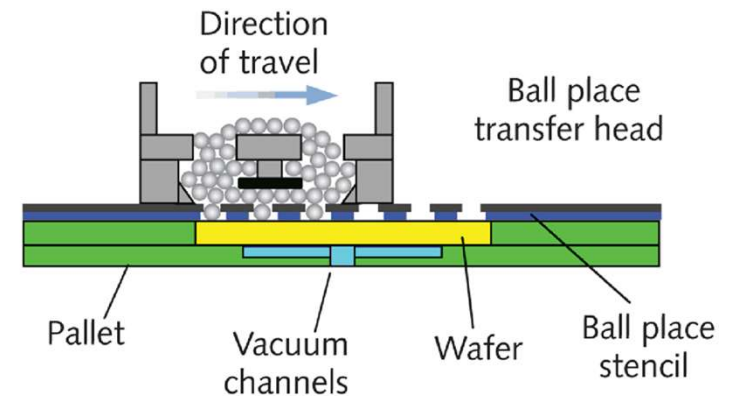
Ball-drop is a high-volume method for attaching pre-formed solder spheres to BGA or wafer-level packages. It supports a wide range of ball diameters and I/O counts while maintaining tight coplanarity.

- Uses pre-formed solder balls with controlled alloy composition
- Achieves uniform ball height through precise sphere diameter and flux thickness
- Suitable for BGA, CSP, and wafer-level packaging

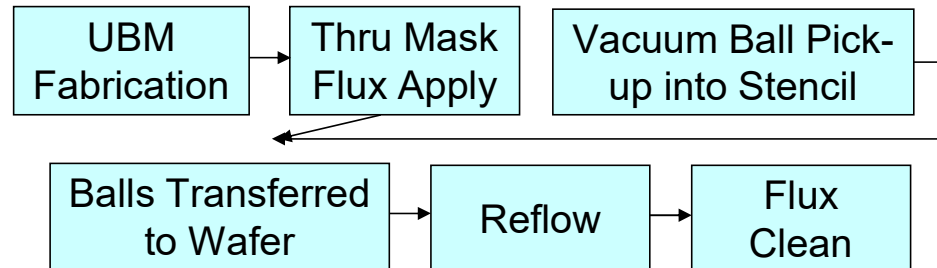
Direct Ball deposition method requires two stencils:

- one for the flux and one for the solder.

Inspection and repair can be done prior to, or post reflow.



# Ball Drop: Vacuum Ball Process

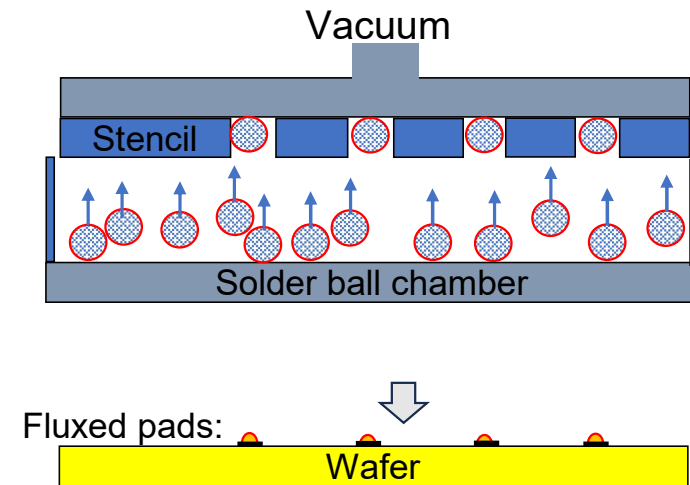


Vacuum Ball Drop use a laser cut stainless still plate that matches the wafer or substrate design. It also can provide:

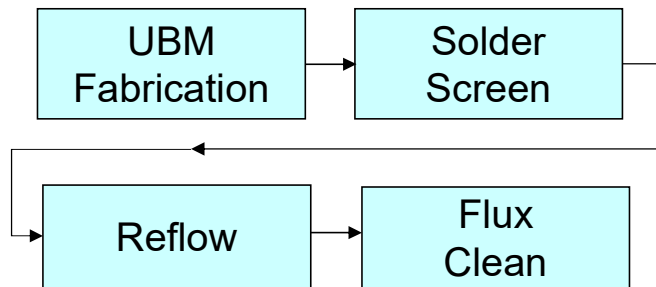
- Varied solder composition
- Uniform solder height (tight coplanarity)

Vacuum Ball drop is the preferred method for CSP and WLP since it is more suitable for fine pitch u-BGAs (150um to 250um).

- Flux dots are deposited within the metal pad
- Vibration of the head forces the loosed balls to dislodge
- Inspection and repair can be done prior to, or post reflow.

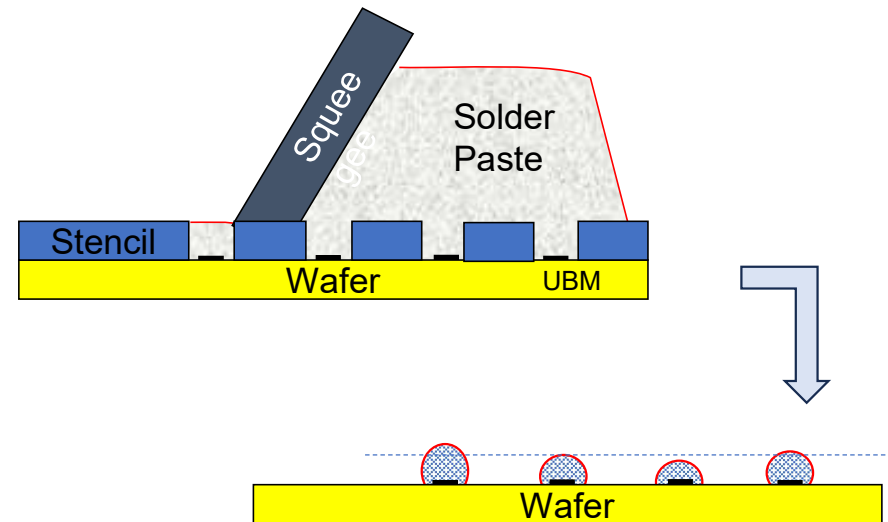


# Stencil Printing



## Solder screening:

- Low-cost solder deposition method
- High flexibility on solder composition
- High coplanarity and volume variation as the ball size decreases.
- Coining (flattening) process is used after reflow on organic substrates to compensate for poor solder coplanarity.



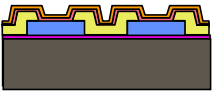
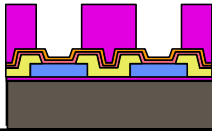
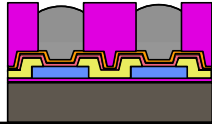
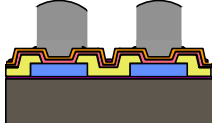
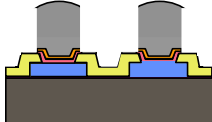
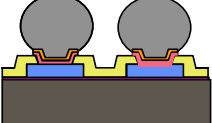
| Stencil Technology | Area Ratio | Aspect Ratio |
|--------------------|------------|--------------|
| Chemical Etched    | > 0.66     | > 1.5        |
| Laser Cut          | > 0.6      | > 1.2        |
| E-formed           | > 0.5      | > 1.1        |
| Micro Stencil      | >0.45      | > 1.1        |

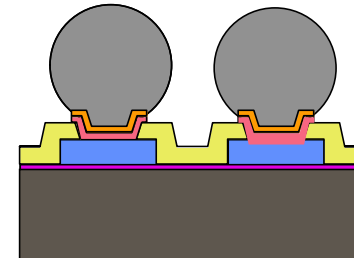
*Heraeus literature*

Area Ratio =  
Pad Area / Wall Area

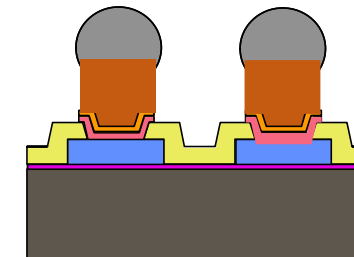
Aspect ratio =  
Narrowest aperture / Stencil thickness

# Pattern Electroplating Process – Lead Free

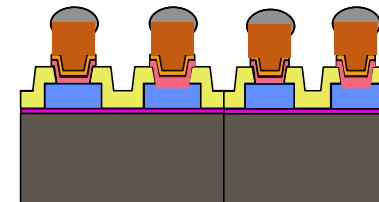
| Electroplated Pb-free Process                                                                                |                                                                                      |
|--------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------|
| Bake/ Sputter Clean / Sputter Seed<br><b>TiW / Cu or Ti / Cu</b>                                             |    |
| <b>Resist Apply:</b> Dry Film or Liquid<br>+ <b>Expose</b> (+,- mask) + <b>Develop</b><br>+ <b>O2 Plasma</b> |    |
| <b>SnAg or Ni / SnAg</b><br>or <b>Cu-Pillar / SnAg</b>                                                       |    |
| <b>Resist Strip:</b> Aqueous or Solvent                                                                      |   |
| <b>Cu Etch:</b> Amonium Persulphate<br><b>TiW or Ti:</b> Hydrogent persulfate or HF<br>+ O2 Plasma           |  |
| <b>Reflow</b><br>- Flux / Belt Furnace / Clean<br>- Formic Acid Reflow                                       |  |



Traditional C4 Bump  
165 to 130 um pitch  
150 to 80 um diameter

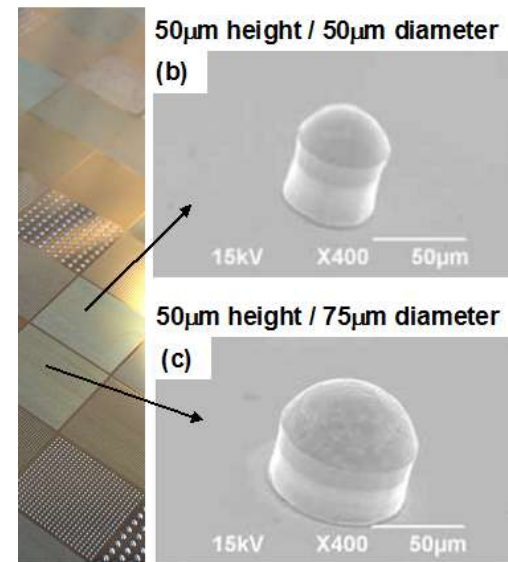
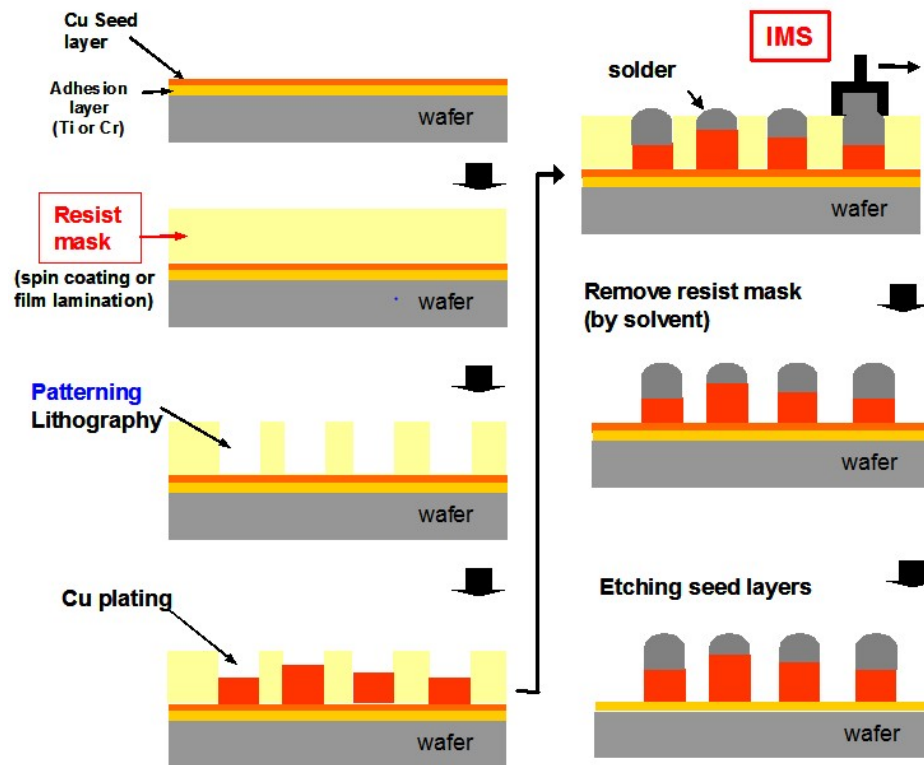


Advanced Cu-Pillar  
130 to 90um pitch  
90 to 50 um diameter



Advanced u-Pillar  
55 to 35 um pitch  
30 to 16 um diameter

# Immersion Molded Solder (IMS) Method

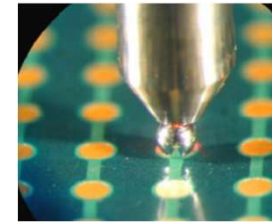
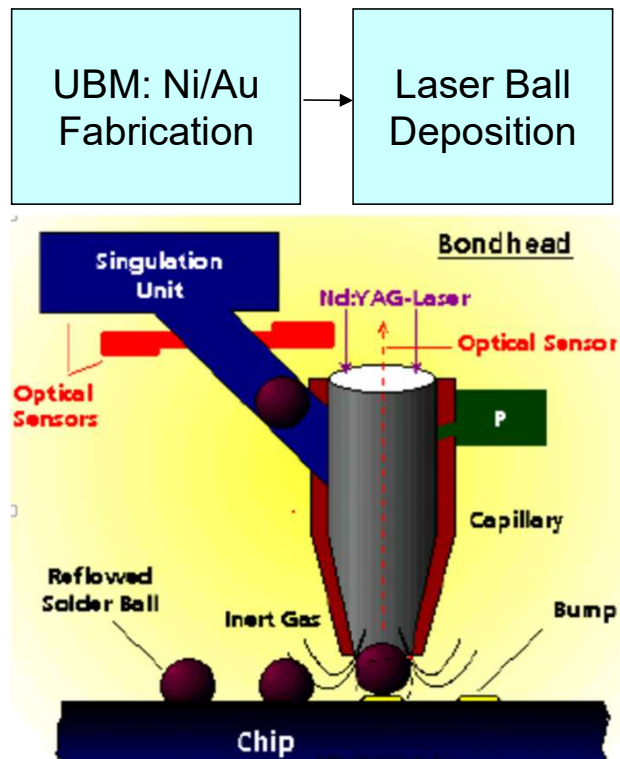


As in solder plating, IMS utilizes the resist pattern used to deposit the resist to deposit the solder.

- results in excellent coplanarity

IMS is a spin-off the C4NP process which can be utilized for traditional C4s, Cu-pillar, or on laminates (w/solder masks).

# Laser Solder Ball Bumper (SB<sup>2</sup>)



- Utilizes a Nd: YAG laser reflow
  - 40 Hz, 400 mJ
- Solder balls are deposited and reflowed one at a time
  - 3,000 balls / sec
  - 80  $\mu$ m to 760  $\mu$ m diam.
  - Pb and Pb-Free solders
- UBM is required
- Flux is not required
- Flexible bump placement (No mask)
- Localized heating (Only solder melts)

SB<sup>2</sup> can be used as a solder ball repair tool for missing balls.

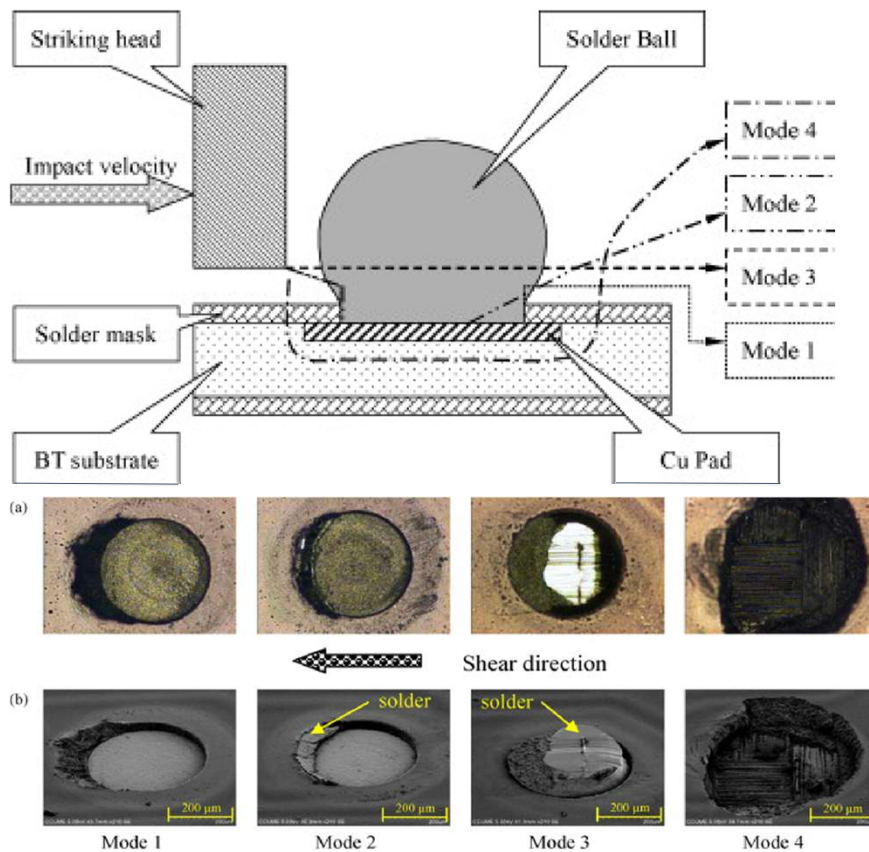
# Solder Deposition and Application Summary

|                  | Applications       | UBM Required | Composition Flexibility | High # of C4s | Volume Control | Flux Required | Propensity for Voids | Underfill Required |
|------------------|--------------------|--------------|-------------------------|---------------|----------------|---------------|----------------------|--------------------|
| Ball Drop        | BGA and CSP        | Y            | Y                       | N             | Y              | Y             | Y                    | Y                  |
| Laser Ball Bump  | Sensors            | Y            | Y                       | N             | Y              | N             | N                    | Y                  |
| Solder Screening | PWB componets      | Y            | Y                       | Y             | N              | N             | Y                    | Y                  |
| IMS              | Flip-Chip, 3D      | Y            | Y                       | Y             | Y              | N             | N                    | Y                  |
| Electroplating   | Flip-Chip, 3D      | Integrated   | N                       | Y             | Y              | Y             | N                    | Y                  |
| Au Stud Bump     | Sensors, High Temp | N            | N                       | N             | Y              | N             | N                    | N                  |
| ACA              | Displays           | Y            | Y                       | N             | N              | N             | Y                    | N                  |

The driver for process section is cost and application specific need:

- Ball drop is effective on BGA and CSP where large solder volume is not practical for plating or solder paste. Oxidation problems with low ball size.
- Solder screening results in high volume variation and is used for non-volume-critical applications.
- Au stud and laser bumping is used on sensor that demand clean optics.
- ACA are use on displays. Underfill integration makes ACA a low-cost solution.
- C4 plating has the widest pitch range for flip-chip connection but has limited solder composition selection.
- IMS provides large solder material selection and highly co-planar structures but high cost.

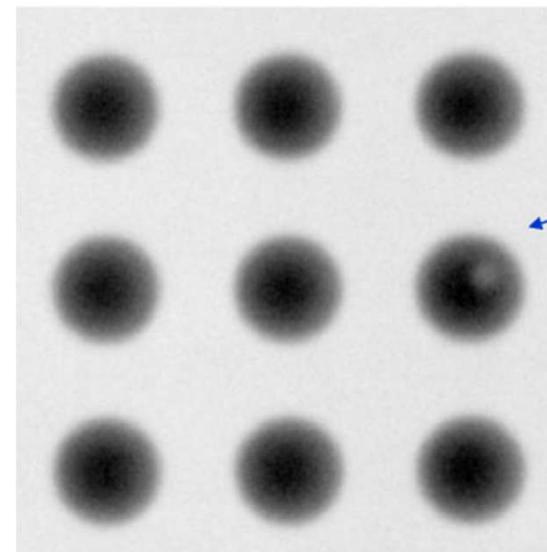
# Bumping Characterization



Two outgoing test for bump integrity are:

1. Shear Test – for failure mode and value
2. X-ray Inspection for solder voids

Solder alloy & reflow profile can influence failure mode.



# Nanoparticle Interconnect Development

- Cu nanoparticle (Cu inks) are placed between the Cu-pillar and the receiving Cu pad.
- Low joining temperatures minimizes the CTE miss-match between the die and the substrate.
- Tested on 150  $\mu\text{m}$  pitch, but extendible to finer pitch.

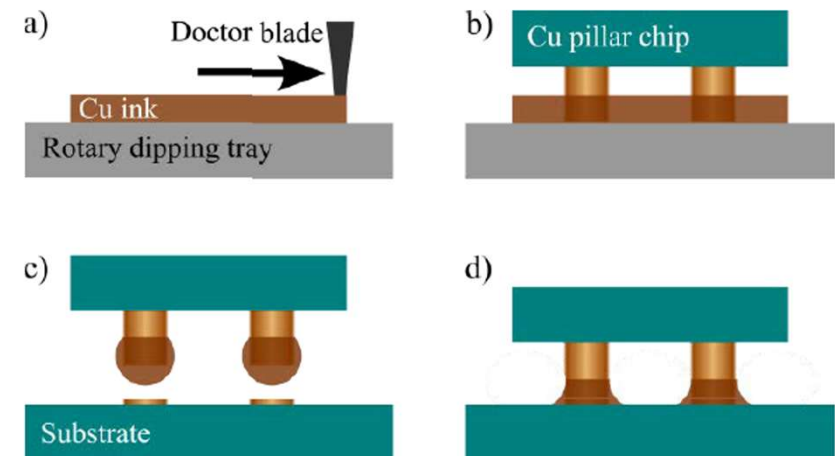
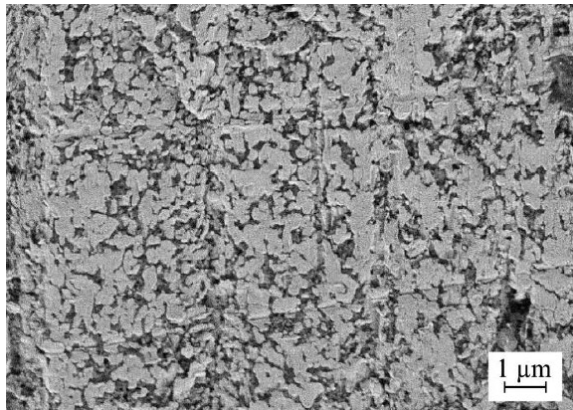


**Figure 6** Process sequence of the dipping method:  
a) preparation of a Cu ink film; b) dip into Cu ink film by Cu pillar chip; c) ink transfer and alignment to substrate; d) joint formed by Cu pillar chip placement and NP self-assembly.

# Part 2: UBM and Solder Deposition Methods Summary

## Module 2: Solder Bumping — Core Concepts

### 1. Under-Bump Metallurgy (UBM)

- 3 functional layers: **Adhesion (Ti), Barrier (Ni-based), Wetting (Cu/Au)**
- Prevents dissolution, ensures wetting, controls IMC formation
- Key issues: **Ni consumption, Ni<sub>3</sub>P formation, Black Pad, IMC growth control**
- Improvements: **Add Cu on top of Ni to create a robust IMC when in contact with the solder**

### 2. Solder Deposition Methods

- **Electroplating (C4, Cu-Pillar):** Fine-pitch; high uniformity; industry standard
- **Ball Drop / Vacuum Ball Drop:** Large-pitch BGA/CSP; high coplanarity; flux + stencil
- **Stencil Printing:** Low-cost; flexible alloy; used on laminates with coining
- **Laser Solder Ball Bumper (SB<sup>2</sup>):** Fluxless, localized heating; can be used for ball rework

# Flip-Chip Interconnect

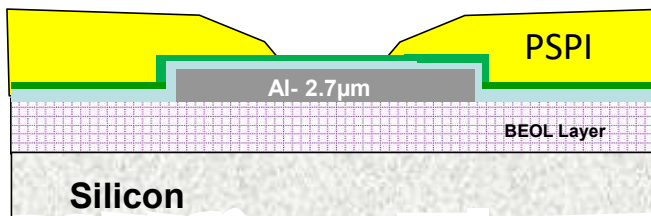
## Part 3: Pattern Electroplating

Part 3 provides deeper look of the pattern-electroplating process; from passivation and seed deposition to thick-resist lithography, Cu/Ni/SnAg plating, and final reflow. It identifies key defect mechanisms such as  $\text{Ag}_3\text{Sn}$  needles, interfacial voids, Kirkendall voids, seed undercut, and solder wicking, and learn mitigation strategies to ensure uniform, reliable C4 and Cu-pillar structures.

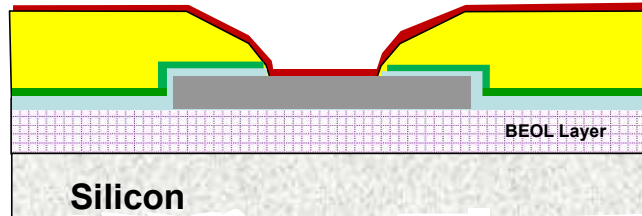
- Key Topics:
- Polyimide Passivation
  - Pattern Electroplating Process Details
  - Pattern Electroplating Processing Issues and Yield Detractors

# Pattern Electroplating Process

Photosensitive Polyimide (PSPI) Lithography

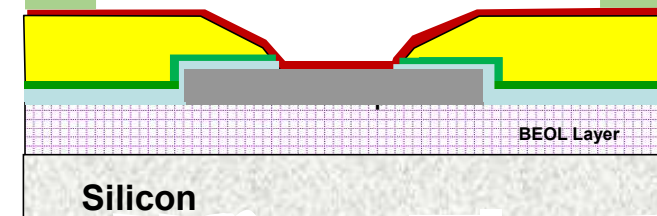


Reactive Ion Etch (RIE) of SiN/SiO<sub>2</sub>,  
Sputter Seed Liner: Ti/Cu seed

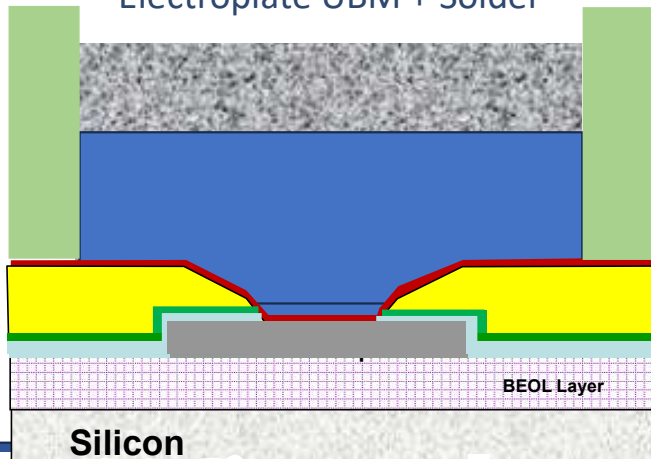


Resist

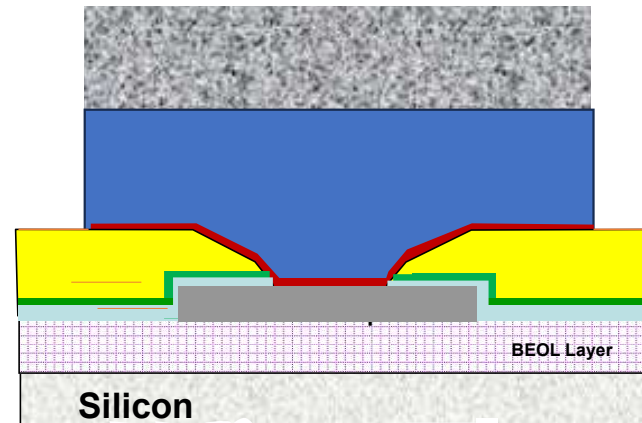
Thick Resist Litho / O<sub>2</sub> RIE



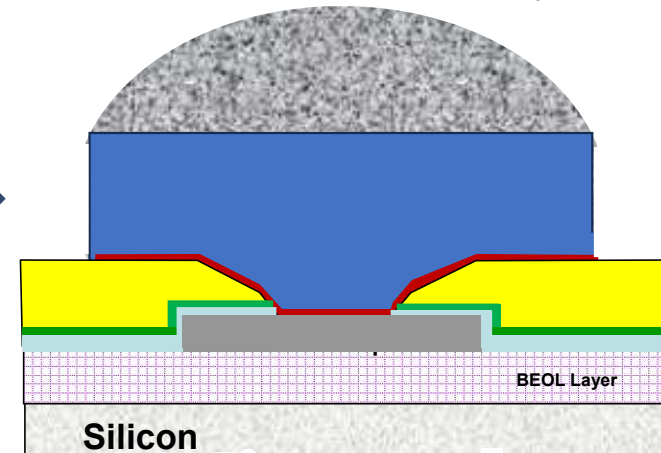
Electroplate UBM + Solder



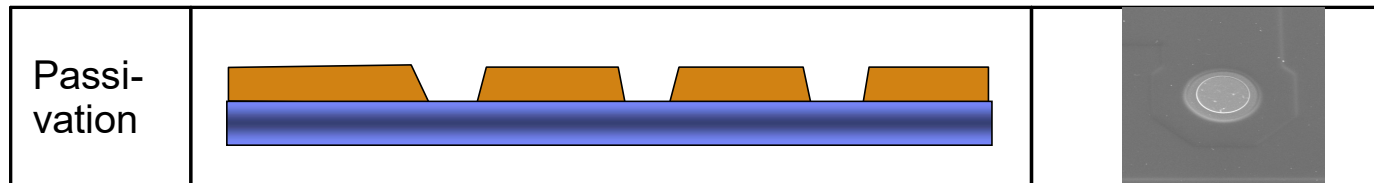
Wet Resist Strip + Seed Etch



O<sub>2</sub> RIE + Reflow / Final Inspection



# Wafer Passivation and Clean



- Passivation films serve as stress buffer between the solder and the BEOL
- Inorganic passivation films such as SiO<sub>2</sub> and SiN eliminate Cu diffusion issues.
- Typical Chip passivation materials are Polyimides, PBO or BCB

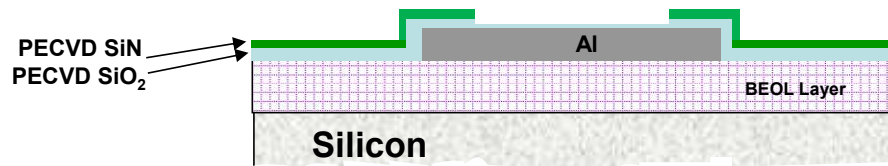
Current stress buffer passivation layer needs:

- High temperature stability for reflow (260°C)
- High elongation for die stresses
- Low outgassing
- Adhesion to SiN, SiO<sub>2</sub> and Al

Future needs for redistribution layer (RDL) and 3D:

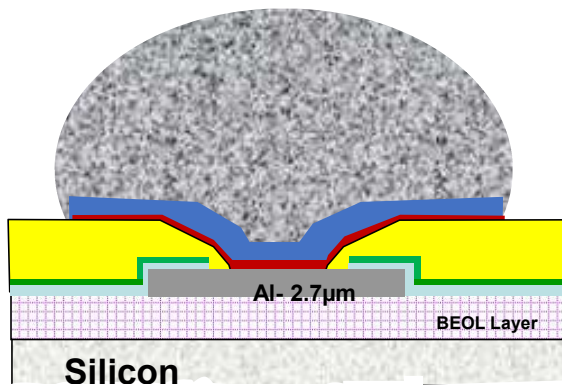
- High resolution: 2 um Line, 5 to 8 um vias
- Low stress for multi-layer applications
- Low temperature curing for sensitive devices (< 240°C)
- Chemical resistance to develop solvents and etchants
- Photosensitive and water based develop
- Fast curing for multiple layer throughput (> 50 WPH)

# Design Options for Passivation Layers

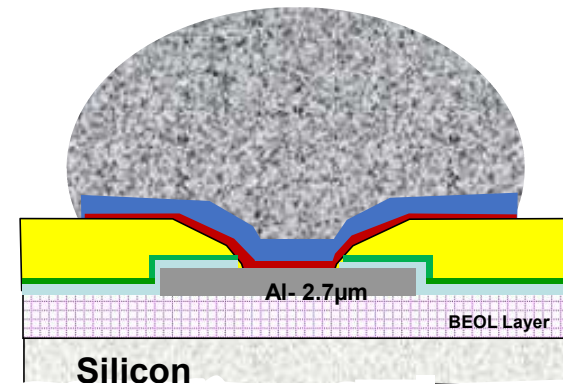


BEOL uses Cu for wiring and then Al layer as the contact pad for electrical test.

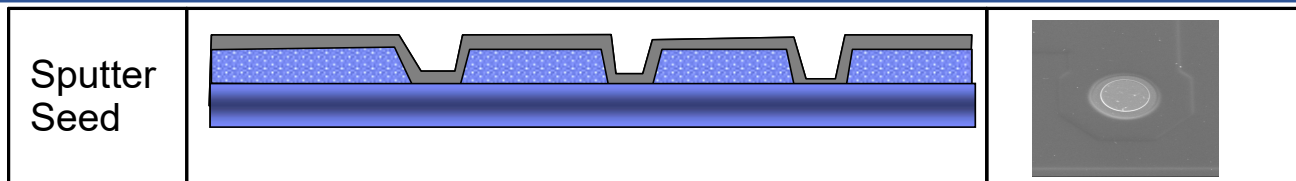
Hard dielectric opening done prior to PSPI;  
PSPI via within the Hard dielectric opening



PSPI used to define the Hard dielectric opening



# Seed (Liner) Deposition



- Wafer Pre-bake to remove moisture on the organic dielectric.
  - Before sputtering or In situ at sputtering
- RF Sputter clean
  - Removes Al oxides for a clean metallurgical bonding
  - Enhances Ti adhesion to PSPI
  - Creates a carbonized conductive layer on PSPI surface
- Sputtered Seed:
  - Ti, or TiW or Cr adhesion layer      ~ 1000 Å
  - Cu conductive seed layer              ~ 2000 Å

# Sputter Deposition Film Stress

Power, Temperature, Pressure and RF Bias at sputter influences:

- 1) Film Stress → wafer bow
- 2) Film Microstructure
- 3) Film Adhesion

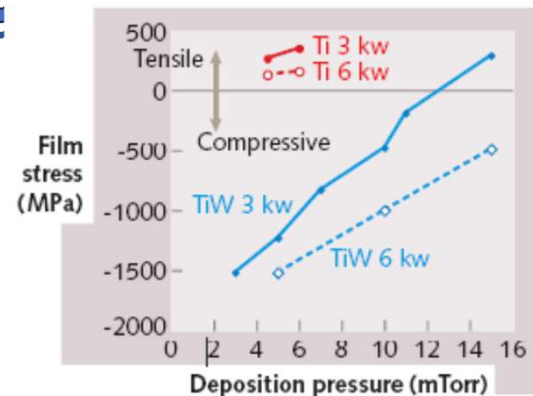
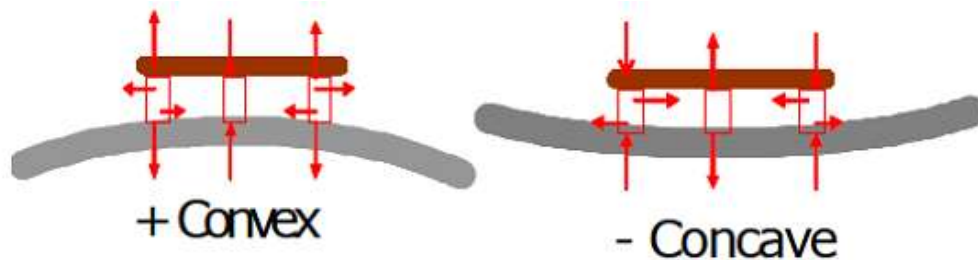


**FIGURE 1.** TiW and Ti film stress vs. deposition pressure for deposition powers of 3kw 6kw.

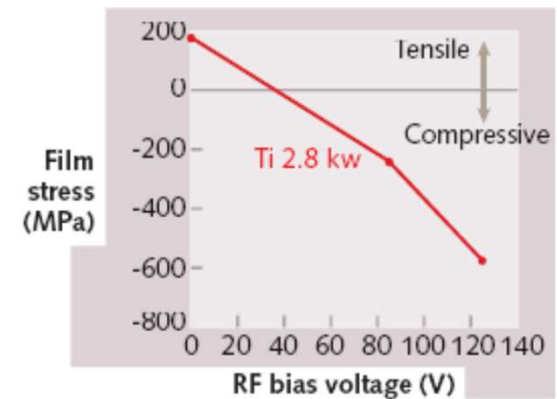
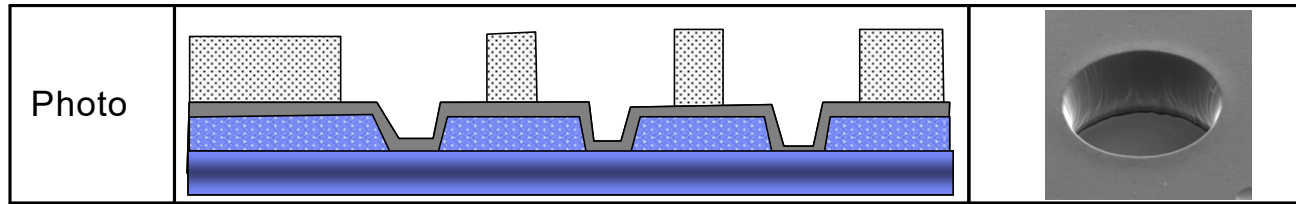


**FIGURE 3.** The dependence of Ti stress on RF bias power for a Ti deposition at 3 mT and 2.8 kW.

PVD Processing for Flip-Chip, Arthur Keigler,  
Advanced Packaging, Vol 16, Issue 7

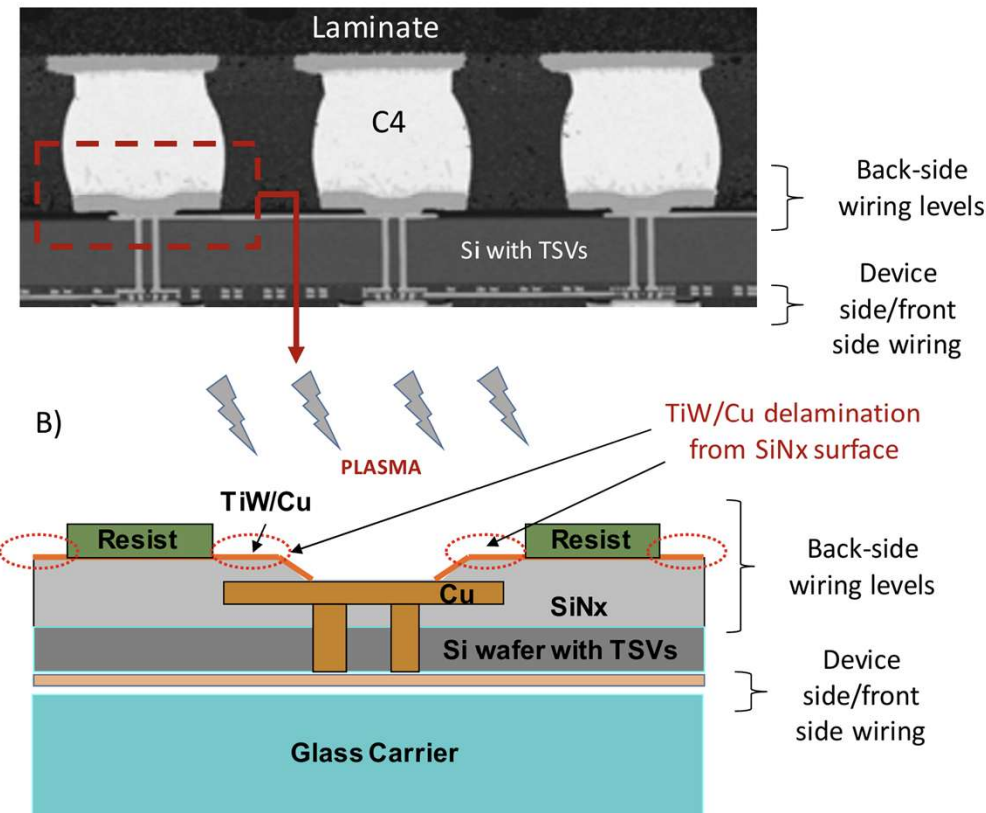
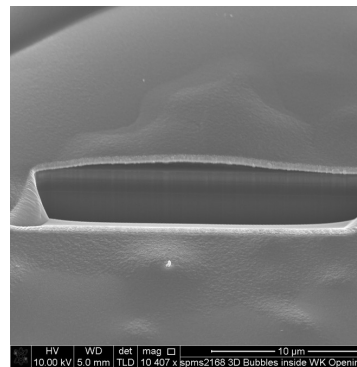
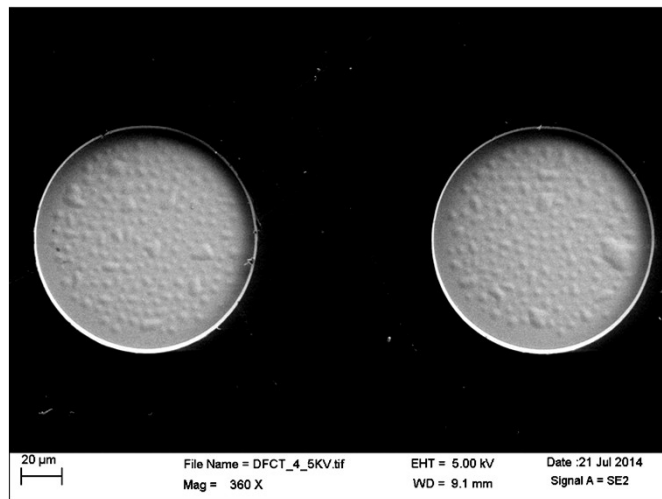
# Thick Photoresist Coating and Lithography



- ✓ **Apply/Bake :**
  - Spin Apply Thick resist
  - or laminate resist (for non circular carriers)
- ✓ **Expose:**
  - Step and Repeat (or Full Field Expose)
- ✓ **Develop:**
  - Selectively removes resist with an aqueous TMAH Alkaline solution
- ✓ **Bake:**
  - Optional – For enhanced adhesion
- ✓ **Inspection**
  - Resist Rework
- ✓ **O2 Plasma clean:**
  - For promoting wetting of plating solution
  - Removes organics (residual resist)
  - Reduces the photoresist foot

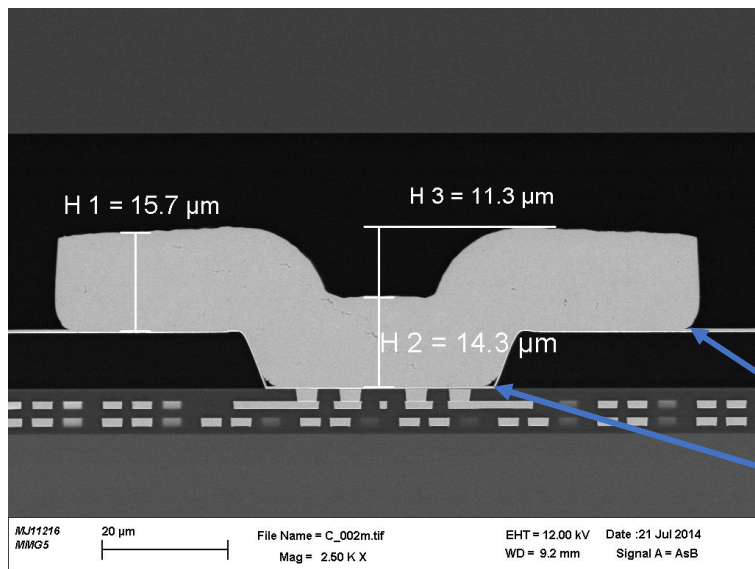
# Plasma Induced Seed Delamination with Glass Carriers

The delamination or blisters of TiW/Cu over the SiNx Surface was observed while using glass carrier.  
The root cause of delamination is identified as the Ar plasma used for clamping the wafers.  
The defect intensity is lowered by reduced Ar plasma power.  
Defects were eliminated by substituting O<sub>2</sub> gas in place of Ar.



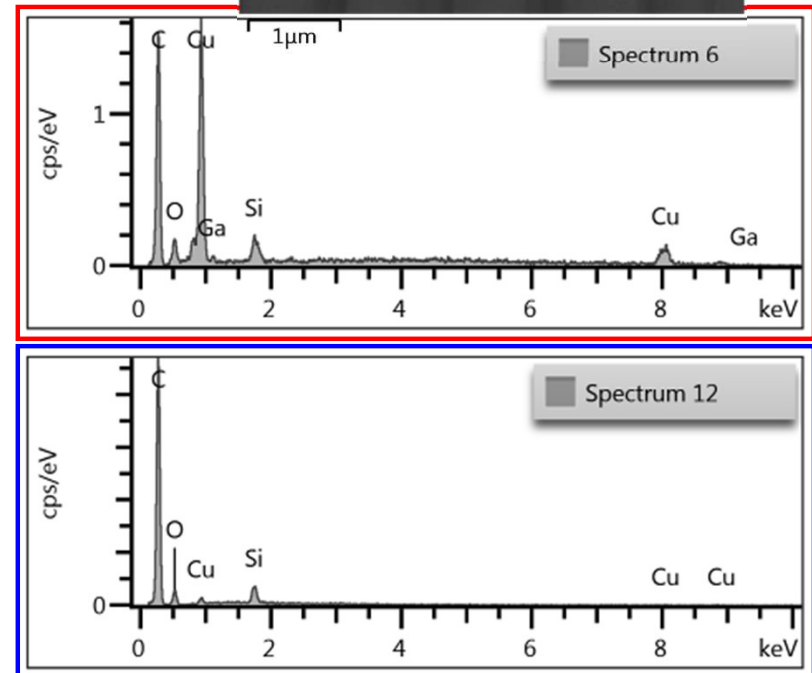
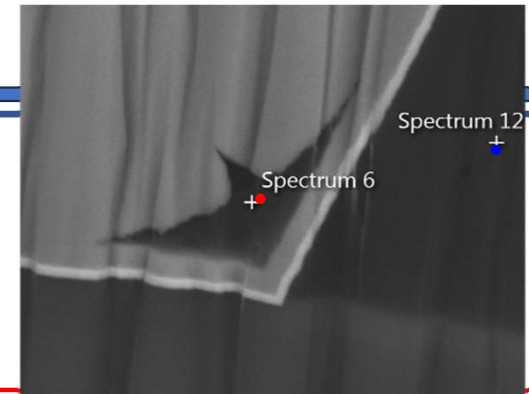
# Residual Resist: At Develop

- Energy-Dispersive X-ray Spectroscopy (EDS) signatures consistent with photoresist.
- Si and Cu signature due to redeposition during FIB processing.

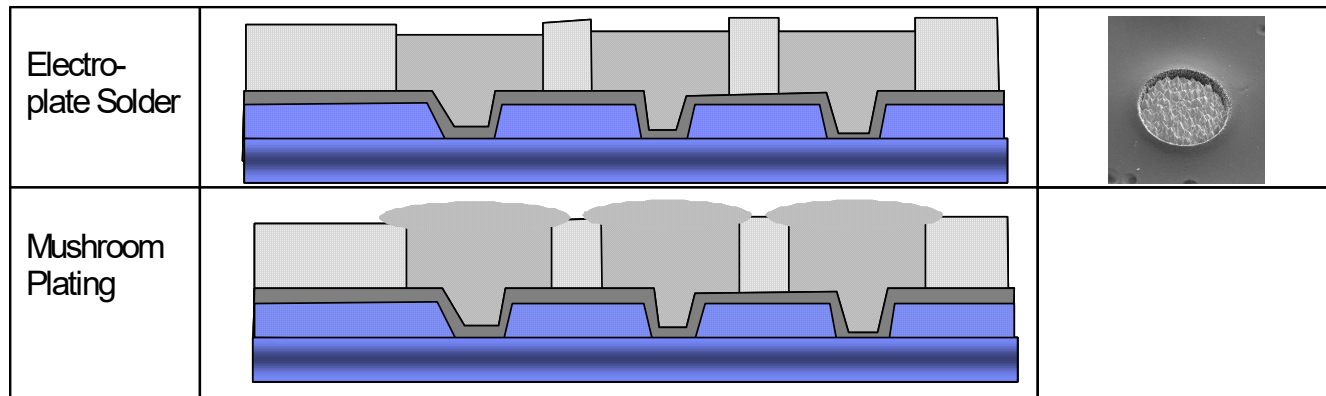


Resist foot

Residual resist

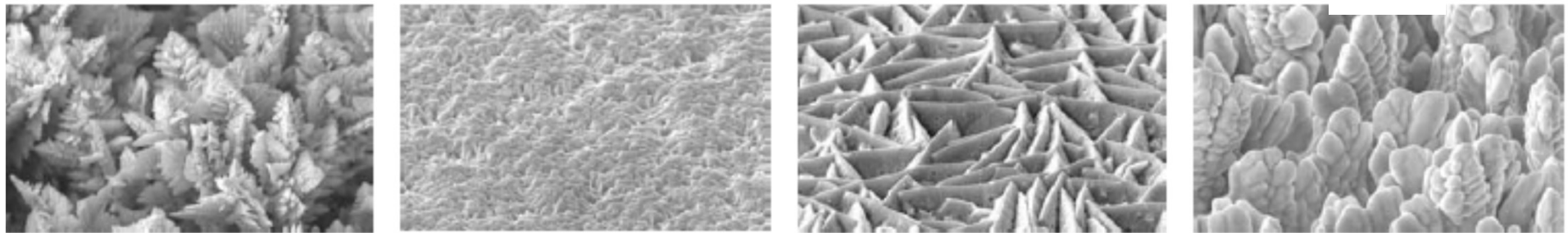


# Solder Deposition: Ni, Cu, Sn, SnAg



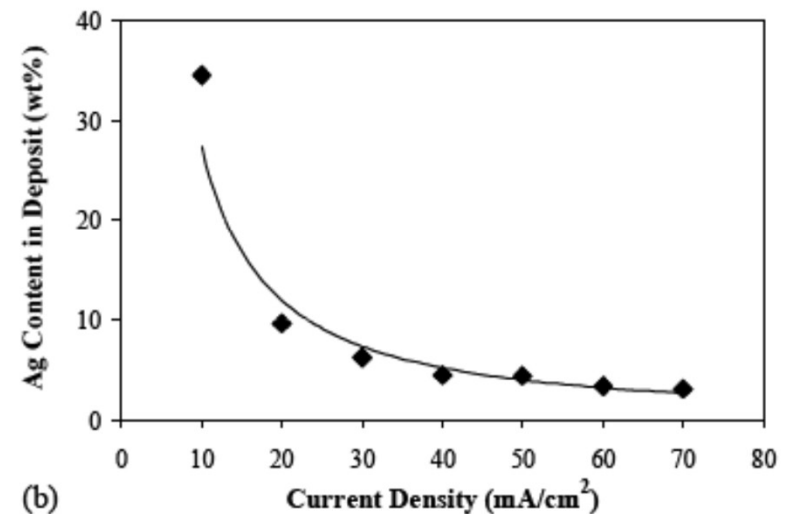
- Resist is developed also at wafer perimeter to allow for electroplating contact.
- When resist thickness is not thick enough, mushroom plating is allowed for increased solder volume.
- Plating chemistry need to be controlled, preferably with auto analyzer and chemistry auto dispenser.
- Sequential electroplating of Cu, Ni and SnAg solder with a water rinse between chemistries.

# Electroplating on SnAg: Effect of Current Density

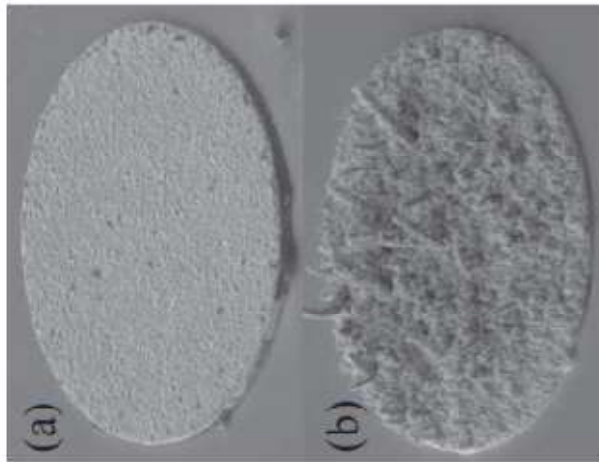


current density  $\uparrow$

SnAg Plating requires tuned chemistry to obtain the desired %Ag at the current density which results in smooth and uniform deposition.



## Effect of Bath Contamination on Solder Bump



SEM Images of plated Ni (a) with no Cu contamination and (b) 500 ppm of Cu.

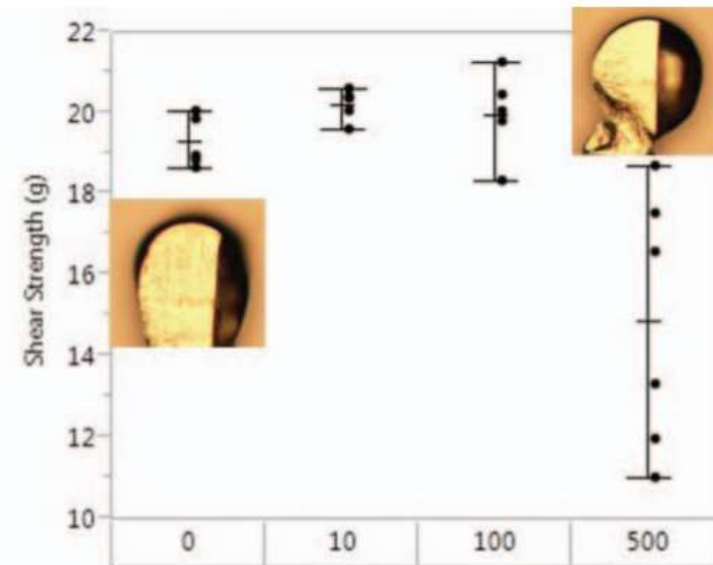


**Figure 13.** Shear strengths and the post-shear images of NiSnAg bumps with Cu-contaminated Ni

Cu contamination in Ni Bath is detrimental to bump integrity specially above 100 ppm. There is little effect of either Cu or Ni contamination on the electroplated SnAg solder.

# Ag<sub>3</sub>Sn Needles Understanding

## Problem statement:

Ag<sub>3</sub>Sn precipitates formed during reflow form a continuous film which could impact assembly yield, electromigration and solder mechanical properties.

## Mechanism:

Increased deposition of Ag in solder coalesce and forms Ag<sub>3</sub>Sn precipitates during reflow, in the form of needles (on top of solder) and/or plates (within the solder).

## Mitigation:

1. Reduce %Ag in Sn to below 2.1%Ag
2. Improve the %Ag distribution across the wafer to reduce high Ag spots.
3. Ensure reflow cooling rate is above 2.5 C/sec

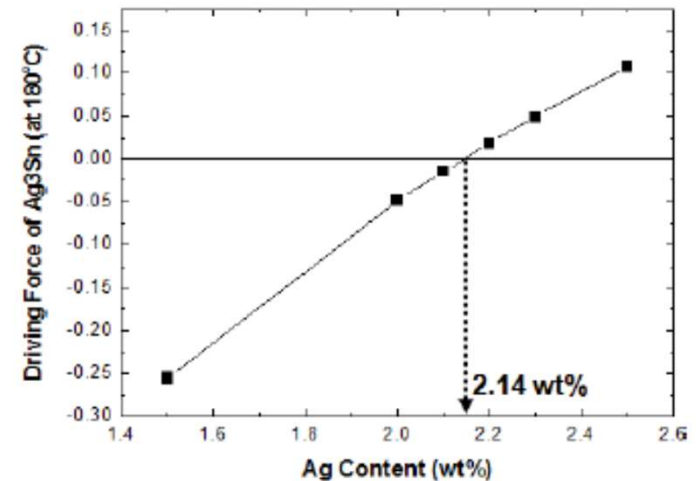
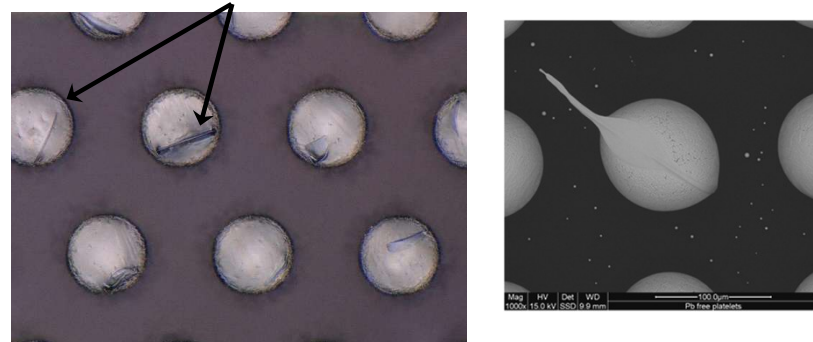
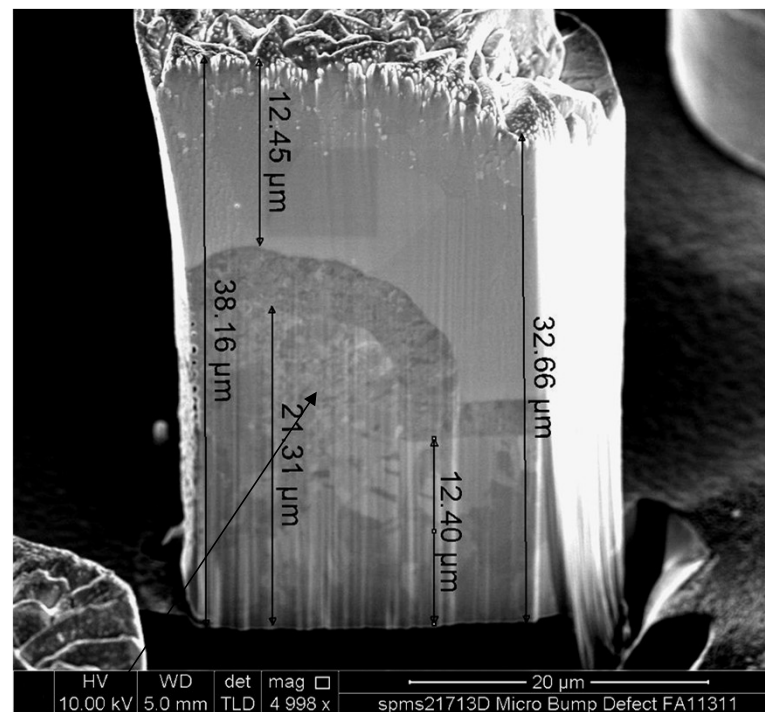
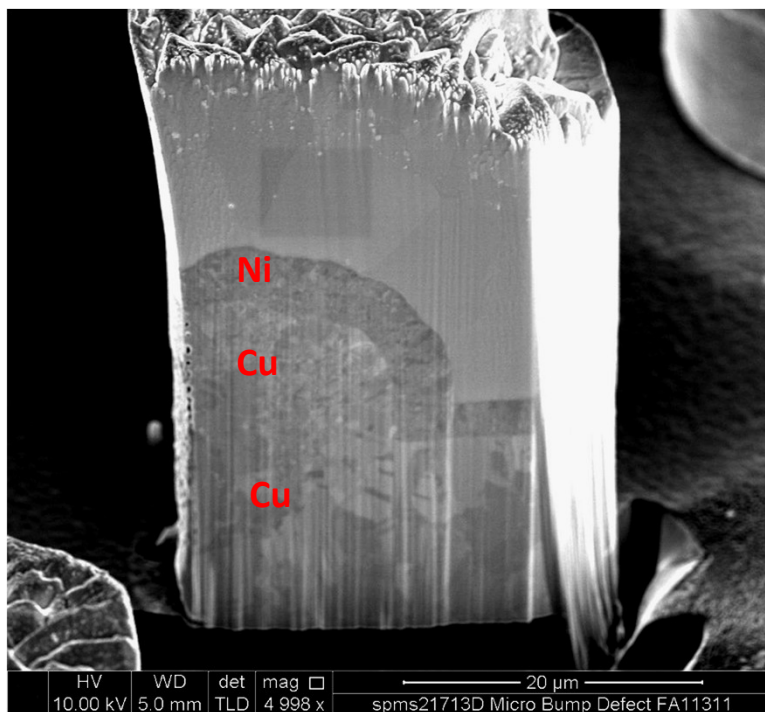


**Figure 6. The calculated driving force of Ag<sub>3</sub>Sn IMCs in the supersaturated liquid at 180°C as a function of the Ag content in the liquid.**

# Plating Defect: Cu Electroplating Nodules

FIB cut view of abnormal Cu-pillar.



Abnormal Cu-pillar deposition significantly affects the solder uniformity.

# Interfacial Voids Understanding

## Problem Statement:

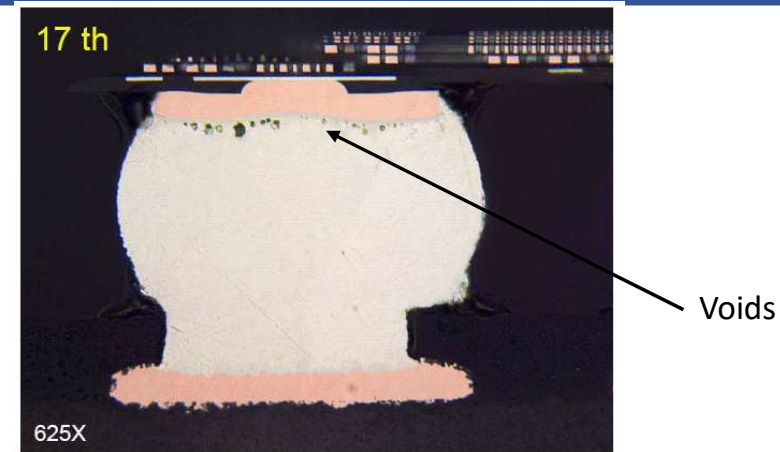
Small voids between the solder and intermetallic affect the mechanical strength of solder bump.

## Mechanism:

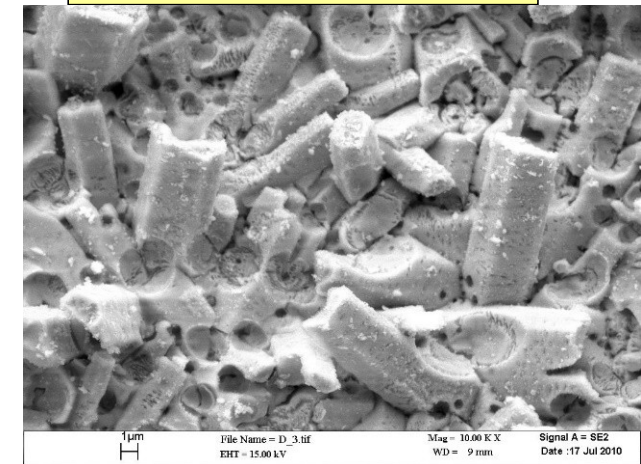
- Deposition of Ag immersion plating and associated organics during the first stage of SnAg plating, prior to current activation.
- At reflow u-voids are formed and get attached to the sides of the intermetallic, or coalesce to form larger voids.

## Three Mitigation Schemes:

1. Start with Sn plating on top of Cu, prior to SnAg plating
2. Eliminate top Cu and deposit SnAg directly on Ni
3. Remove organics byproducts in old SnAg plating bath



Top view SEM on etched solder



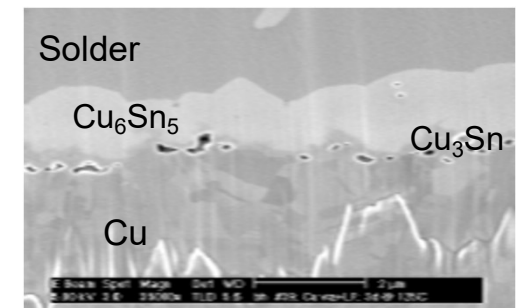
# Kirkendall Voids – Origins in Organic Laminates

## Kirkendell Voids - Mechanism:

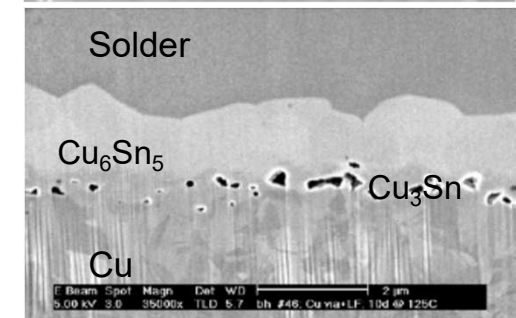
- During Joining of Sn solders with Cu surface the  $\text{Cu}_6\text{Sn}_5$  intermetallic crystallizes, along Cu layer, stopping further dissolution of Cu. Also, a thin intermetallic layer,  $\text{Cu}_3\text{Sn}$ , forms between Cu and  $\text{Cu}_6\text{Sn}_5$ .
- During **thermal aging**, atomic vacancies and impurities are left by Cu atoms migration from the Cu side – which are not filled by the Sn atoms.
- These vacancies coalesce into the so called Kirkendall voids at Cu -  $\text{Cu}_3\text{Sn}$  interface, and in  $\text{Cu}_3\text{Sn}$  compound layer forming discontinuous layer.

## Possible Mitigation:

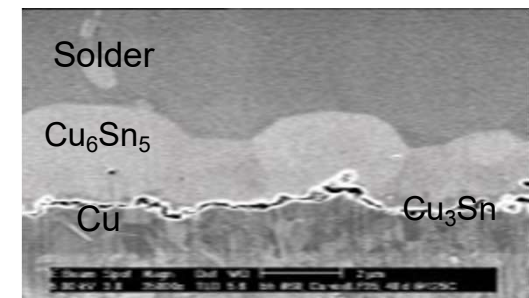
- Replacing the Cu OSP layer with a Ni(P) or Ni(P)/Cu layer.
- Solder additives such as Ni, Bi, Zn (w/Ball drop)
- Increase purity of plated Cu in the substrate
- Change Cu structure to Cu nano twinning



3 days  
of  
125°C  
aging



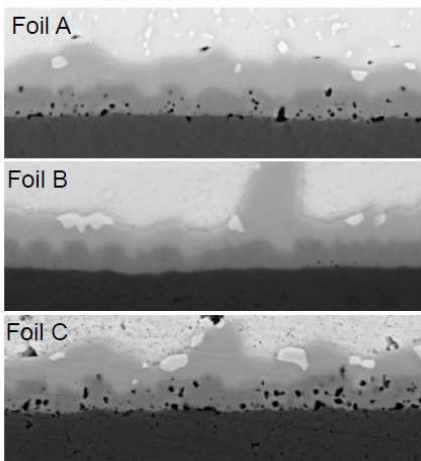
10 days  
of  
125°C  
aging



40 days  
of  
125°C  
aging

# Kirkendall Voids and UBM

Commercial Cu foils for PCB



1 week@175°C

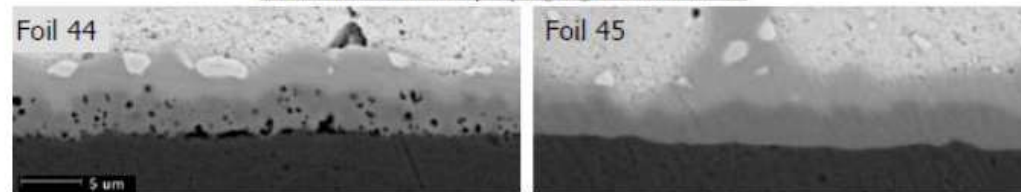
SIMS impurity measurement (ppm)

|    | Foil A | Foil B | Foil C |
|----|--------|--------|--------|
| Cl | 57     | 8      | 59     |
| C  | 28     | 8      | 47     |
| O  | 5      | 1      | 12     |
| S  | 0.5    | 0.02   | 6      |

In the high voiding Cu foils, the impurity levels are in the tens of ppm or less

Incoming foils with high contaminants ppm level had voids in the  $\text{Cu}_3\text{Sn}$  IMC after HTS

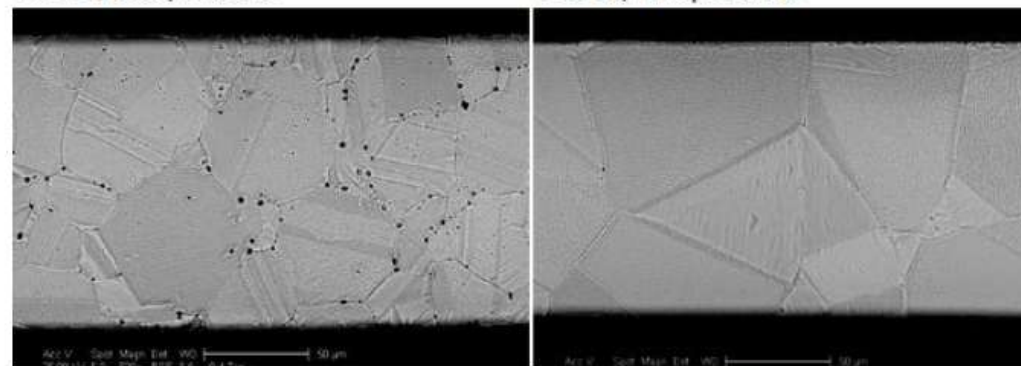
Un-annealed sample, aging 1 wk/175°C



Cu Grain structure of annealed sample

Foil 44, 130 µm thick

Foil 45, 130 µm thick



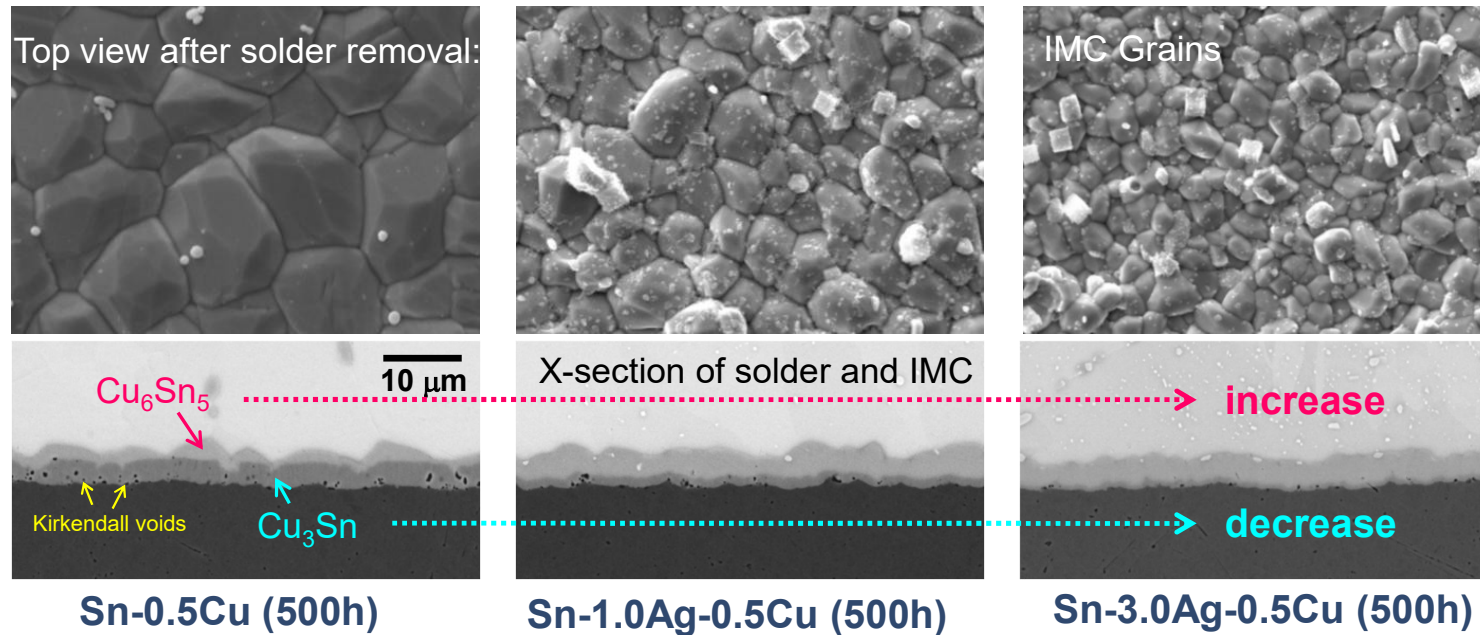
Annealing: 2 hours at 650 °C

Annealing the Cu at 650 C for 2 hours can indicate propensity for the Cu to form KK voids.

Y. Liu, et al, Improving Copper Electrodeposition in the Microelectronics Industry " IEEE Trans. Comp. Pack. Techno. 33, 127 (2010),

L. Yin, et al, "Toward a Better Understanding of the Effect of Cu Electroplating Process Parameters on  $\text{Cu}_3\text{Sn}$  Voiding," Journal of Electronic Materials, vol.41, no.2, pp.302 (2012)

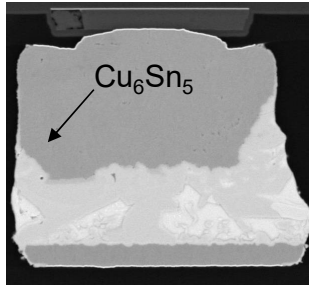
## Effect of %Ag in IMCs Growth



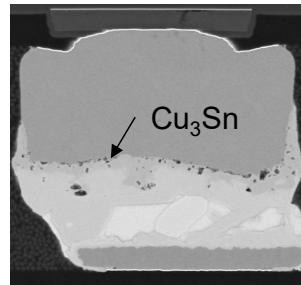
- Kirkendall voids were reduced thru a reduction in the  $\text{Cu}_3\text{Sn}$  layer by increasing Ag%
- After thermal aging at 150C/500hrs, the size of  $\text{Cu}_6\text{Sn}_5$  grains remains stable.

## Kirkendall Void in $\text{Cu}_3\text{Sn}$ IMC      Stack: 14Cu/15SnAg

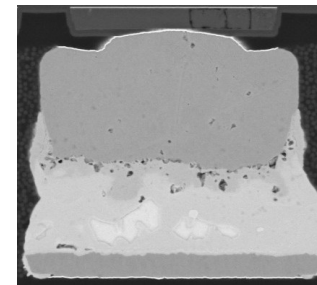
T0, no UF,



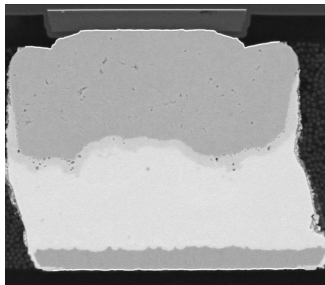
T0+ 500 hrs HTS@150C, UF



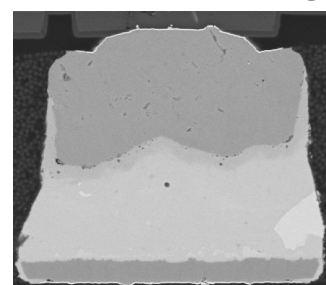
T0+1000 hrs HTS @150C, UF



T0+ 250C, 30 min, UF



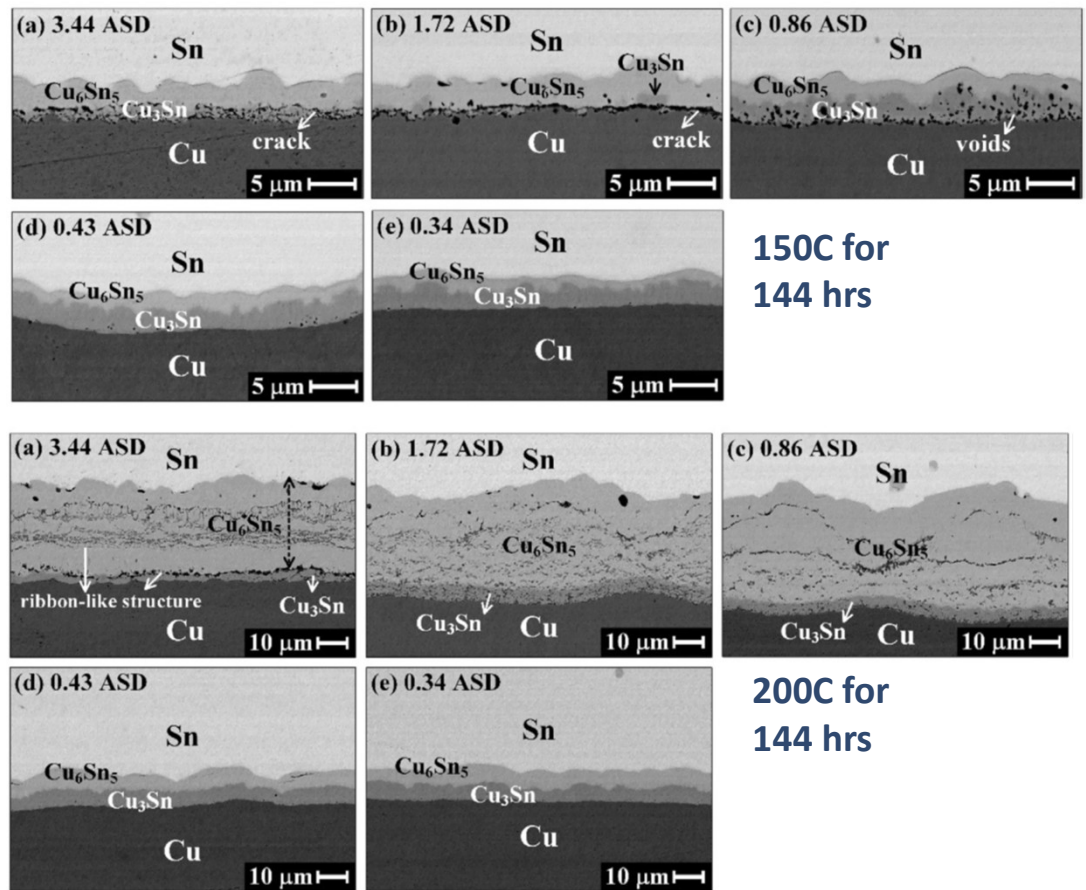
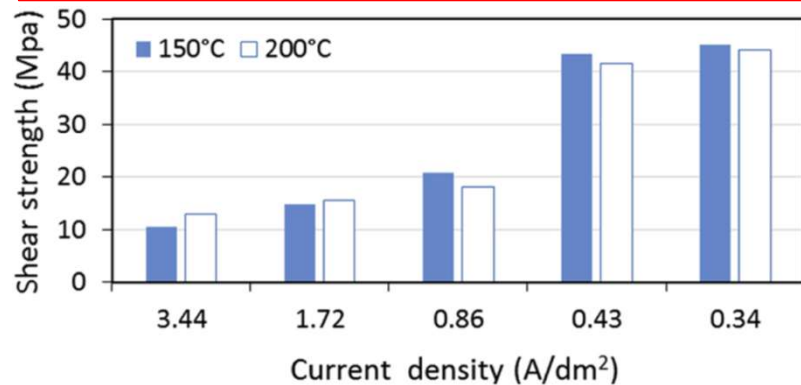
T0+ 250C, 30 min + 1000hrs HTS @150C, UF



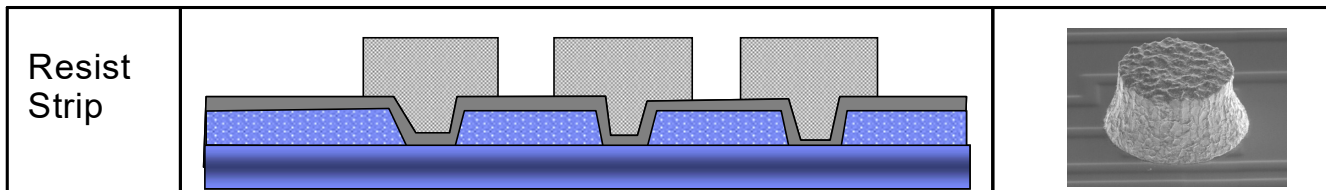
The size and number of Kirkendall voids increased with 500 hrs at 150 C HTS and remained stable at 1000hrs HTS. However, full conversion of intermetallic prior to HTS testing mitigated the  $\text{Cu}_3\text{Sn}$  IMC and the amount of Kirkendall voids at that intermetallic.

# Cu Nanotwin and Void Suppression

Electroplating current density plays an influential role in the evolution of Cu grain microstructure. Reducing the current density to below 0.43 A/dm<sup>2</sup> results in a high fraction of Nano-twinning lamellae in the as-plated Cu film. Nano-twinning structure subdues the impurity incorporation suppressing the void formation.



# Resist Strip



## Strip Chemistries:

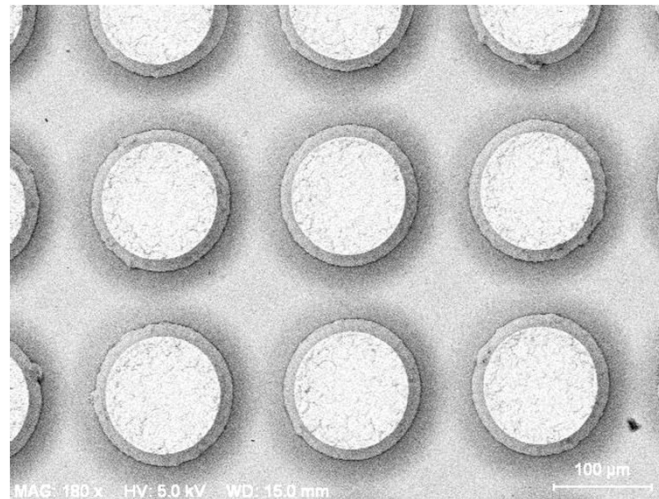
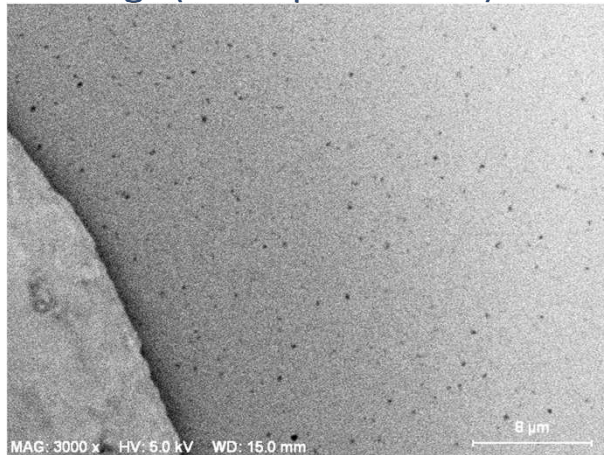
- Organic Solvents with DMSO (w/10% Amines) or NMP w/TMAH or Acetone or KOH can be used; followed by an IPA rinse.
  - Some resists chemistries and laminated resists are more difficult to strip.
- O<sub>2</sub> or O<sub>2</sub>/CF<sub>4</sub> plasma to remove any resist residues.

➔ Requirements: Strip Chemistry can not attack the Cu seed or Sn.

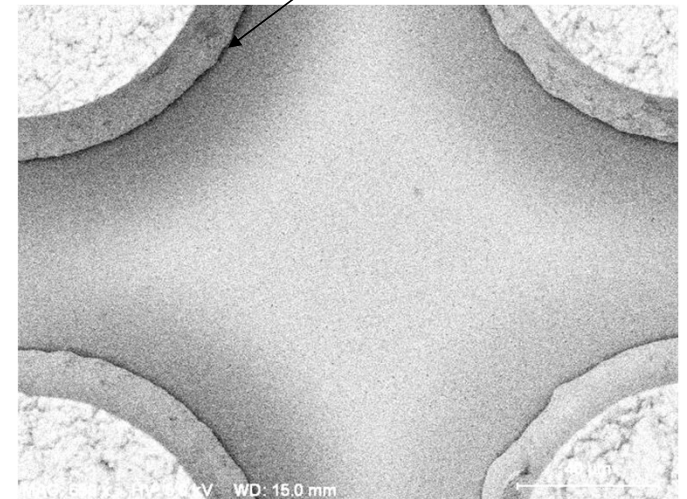
# Post Strip Defects

Top View SEM:

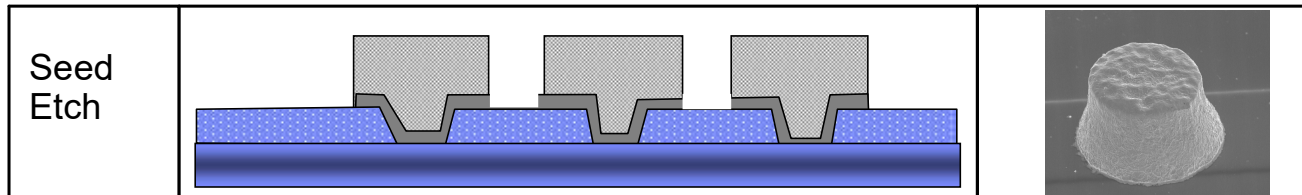
u-Pittings (dark spots on Cu)



Thin carbonaceous residues around C4 bumps.



## Seed (Cu and Ti) Etch



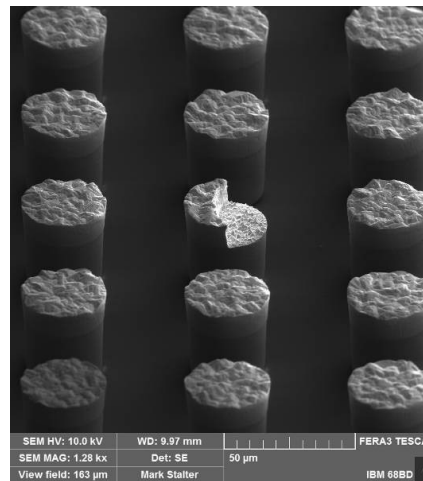
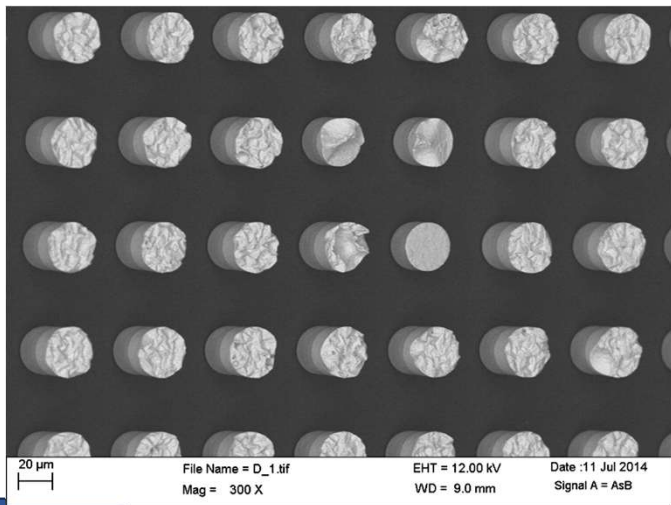
- Cu Etch can be etch at room temperature while Ti Etch needs 45C.
- Minimal undercut of seed under the UBM is obtained by tight etch time control, end point detect system and chemistry control.
- Etch chemistries should have minimal Sn attack/etch.

# Defect: Coplanarity Fails

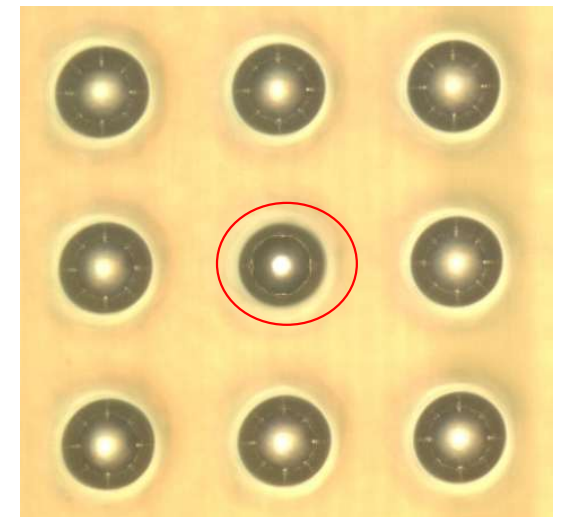
**Coplanarity Fails** – Large height difference between highest to lowest bump within a chip

**Mechanism:** Solder dislodging during the High-Pressure Clean operation.  
Issue more prevalent with smaller solder diameters.

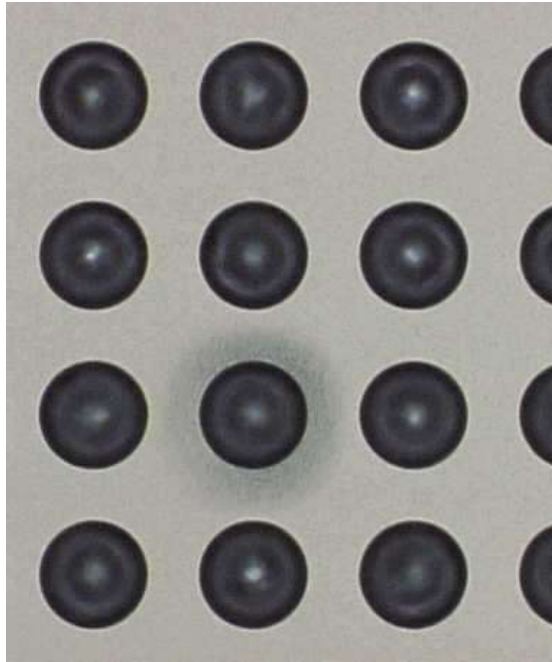
**Mitigation:** Improve cleaning process prior to solder plating.



Post reflow:

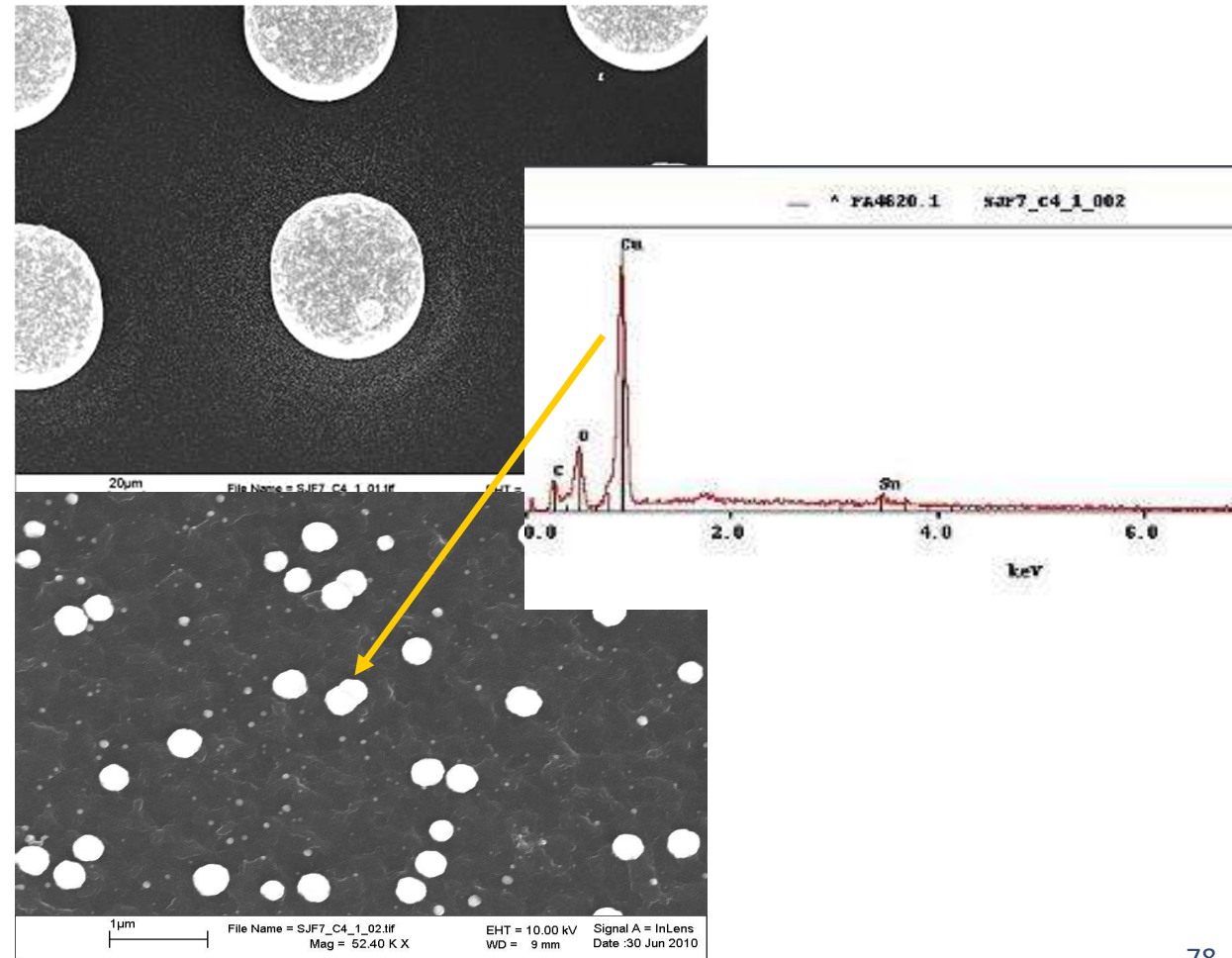


## Defect: CuSn Sphere Halo



### Mitigation:

- Increase Cu over etch to undercut Sn
- Evaluate alternate stripping chemistries

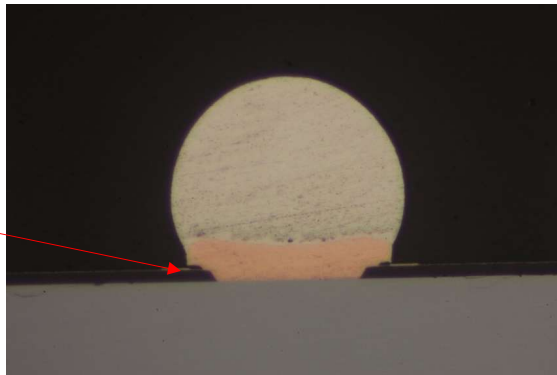


# Large Bump due to Residual Seed Layer

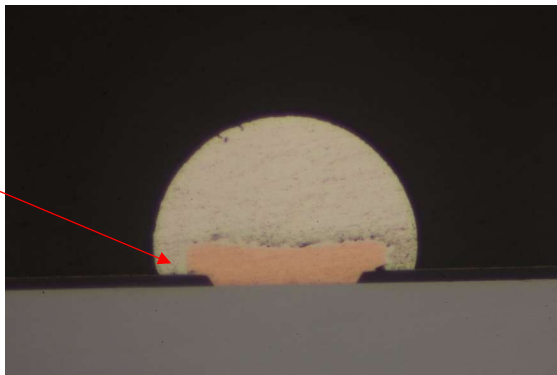
Resist lifting during electroplating.

**Post Reflow:**

Residual /  
Unetched seed

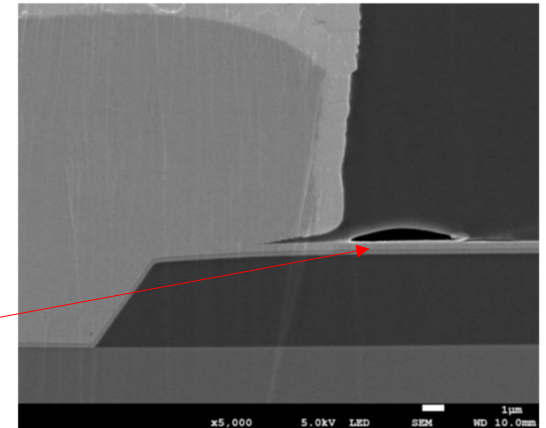


Wetting of  
solder on  
residual seed



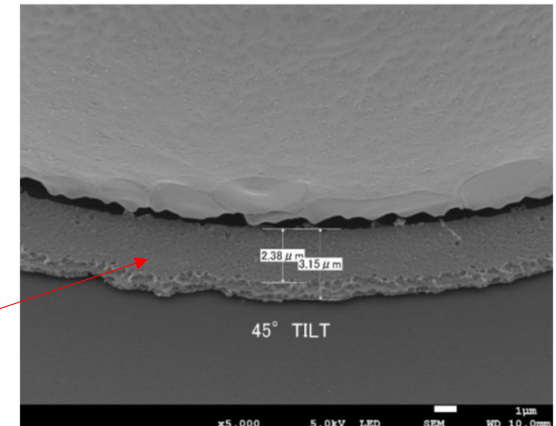
**Post Plating:**

Resist Lifting  
at SnAg  
Plating



**Post Reflow:**

Un-etched seed: Sn  
covered Seed on  
bump perimeter  
(Ribbon)



# Ribbon-Like Defect

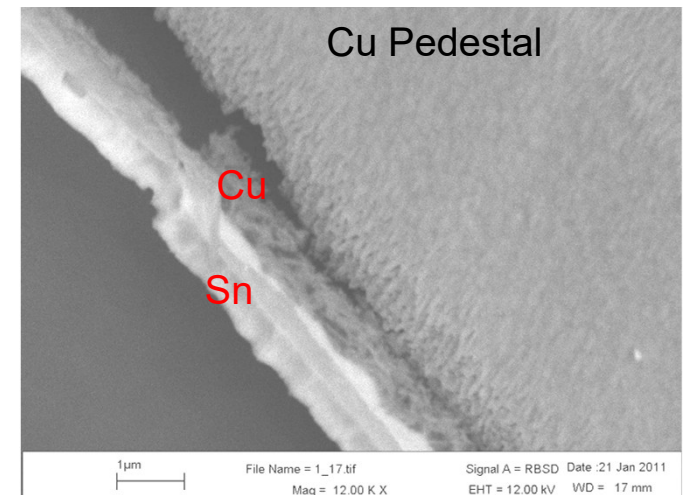
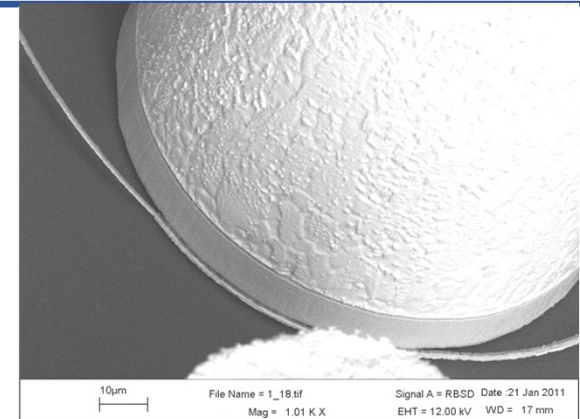
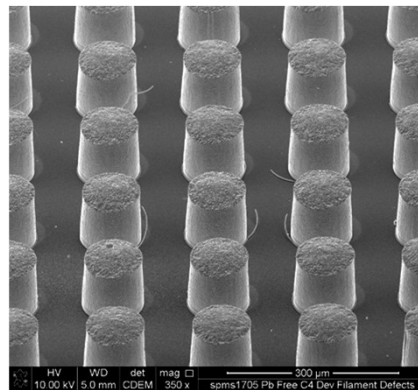
**Problem Statement:** Filament-like defect during seed etch.

**Mechanism:**

- Solder deposition on seed around C4 perimeter resulting smaller solder diameters.

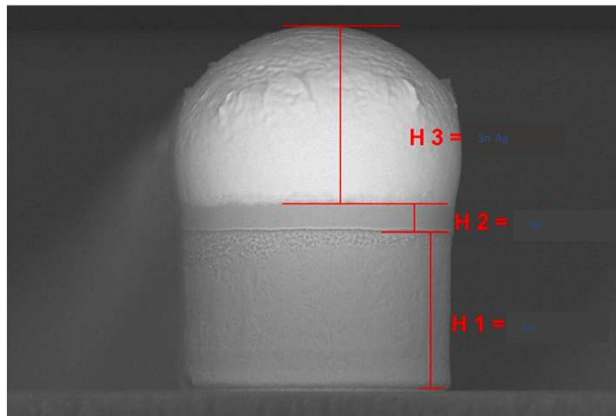
**Mitigation:**

- Improve resist adhesion to seed layer, preventing resist lifting during plating.



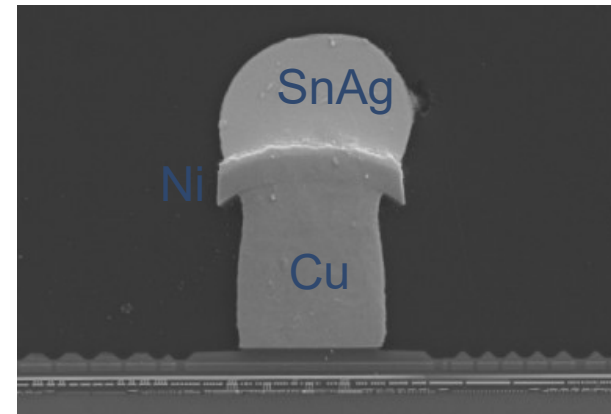
# Seed Over Etch

Ideal u-Pillar



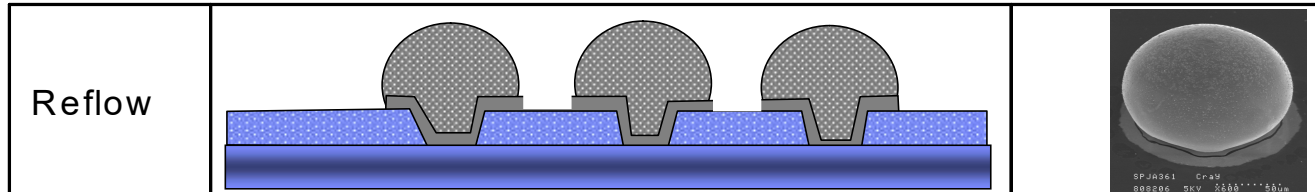
No Cu undercut  
Good solder volume

Marginal u-Pillar



Significant Cu undercut (during seed etching)  
Low solder volume

## C4 Finishing: Clean, Reflow and Inspection



### C4 Finishing:

- ✓ **O2 Plasma:** Removes the polyimide conductive haze
- ✓ **Reflow:**
  - 1) Formic Acid reflow at 245 C, or
  - 2) Flux apply, mass reflow in N2 env., and flux clean
- ✓ **Final Inspection:** Optical inspection of all C4s: Chip Yield
- ✓ **Test:** Identifies good chips
- ✓ **Post test Reflow** Optional- to remove test probe marks

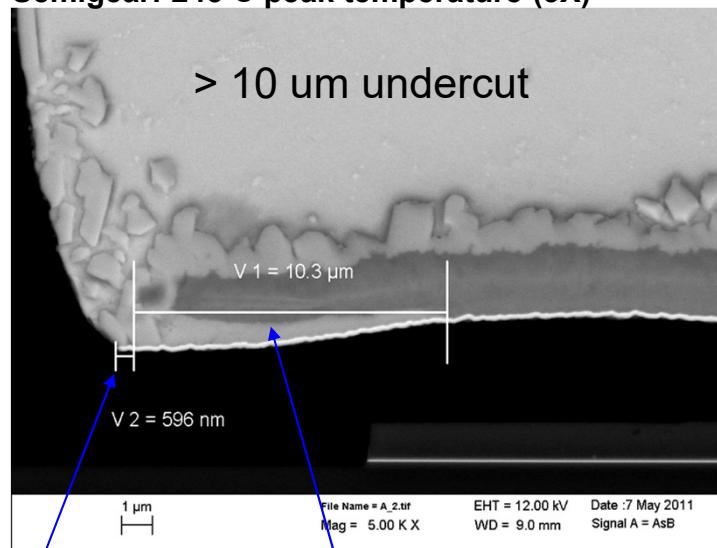
➔ Proceed to Module Assembly

# Thermal Undercut

**Problem:** A combination of reflow parameters (long times and high temperature) and can result in Sn reacting with Cu seed (under the Ni UBM) reducing effective joining area.

**Mitigation:** 1) Introduce Cu in the UBM; 2) Reduce reflow peak temperature and time.

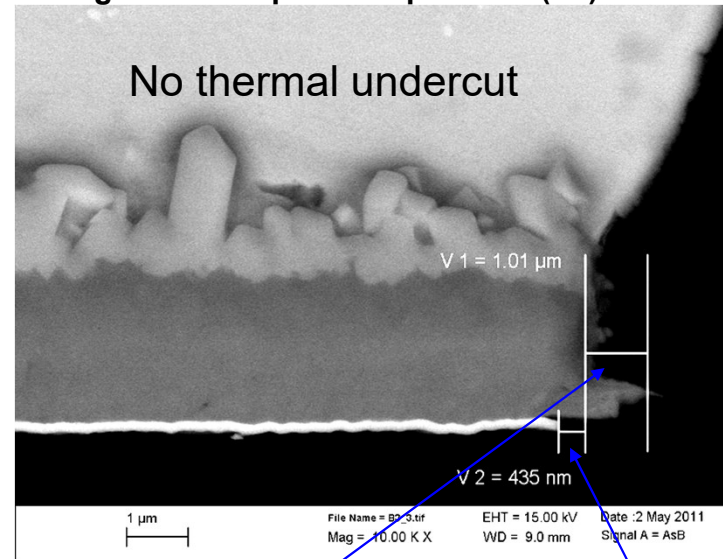
Semigear: 245 C peak temperature (3X)



TiW extension

Thermal Undercut = CuSn IMC

Semigear: 230 C peak temperature (3X)

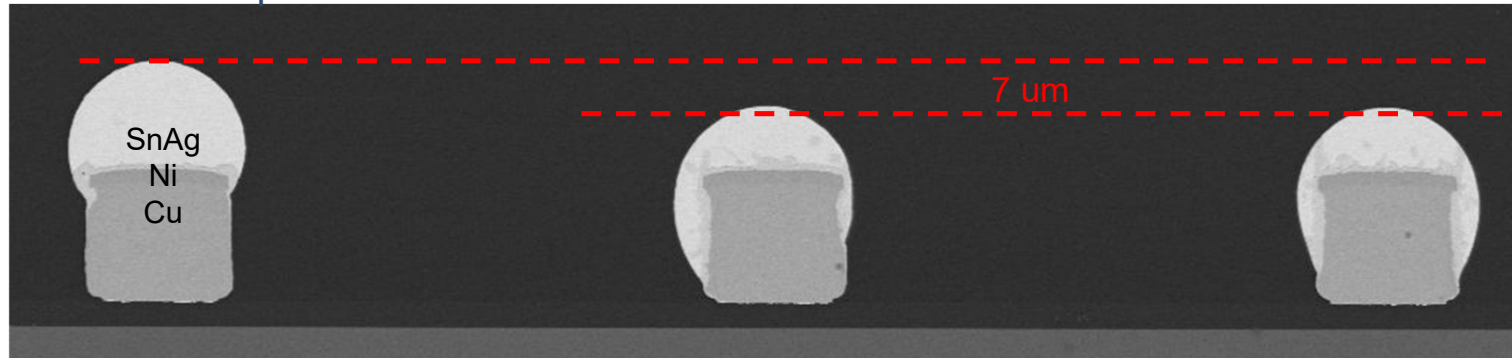


Cu(s) extension

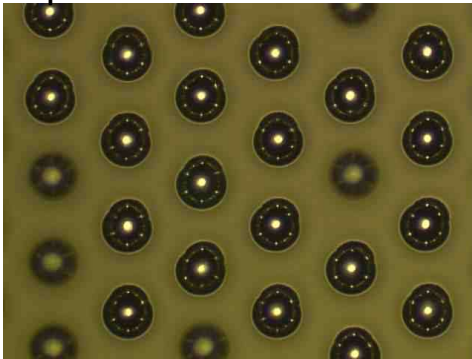
TiW undercut

# Structure/Process Effect on Coplanarity

Post Reflow optical x-section:



Top view:



**Mechanism:** Large solder volume to UBM diameter ratio can cause solder movement at reflow resulting in solder wicking.

- Possible solutions:
- 1) Eliminate top Ni
  - 2) Add top Cu (for IMC to create anchor)
  - 3) Lower solder volume (solder height  $\leq$  UBM diameter)
  - 4) Increase reflow cooling rate
  - 5) Optimize the Formic acid reflow process

# Fluxless Reflow and Solder Wicking

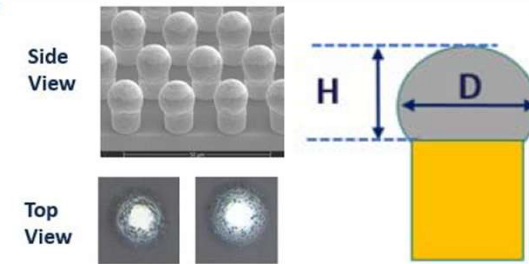
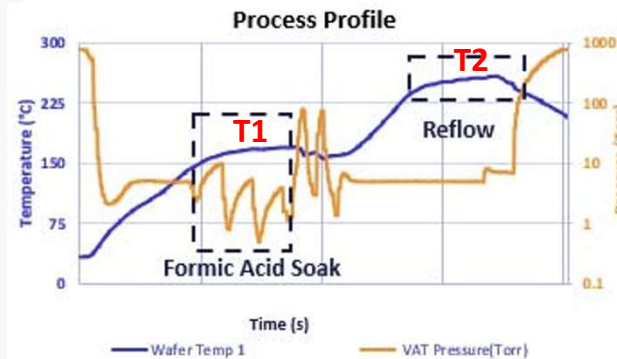
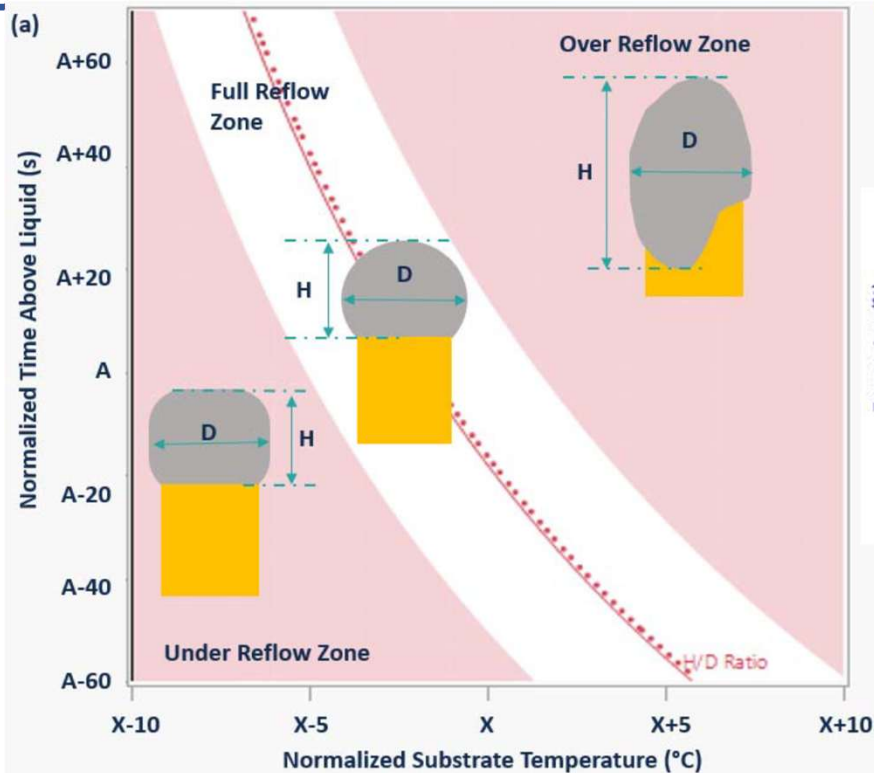


Figure 8B. Full reflow

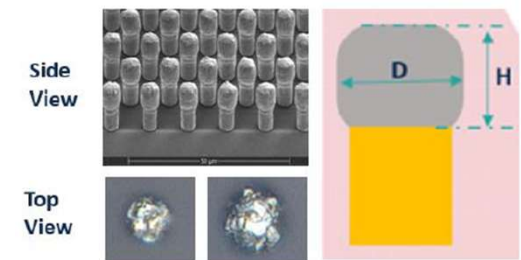


Figure 8C. Under Reflow

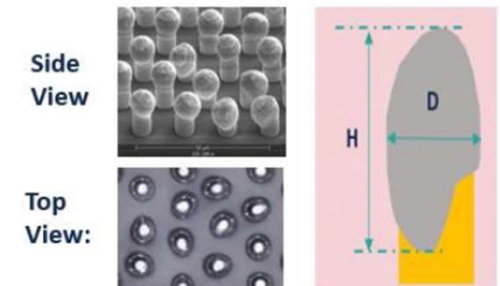


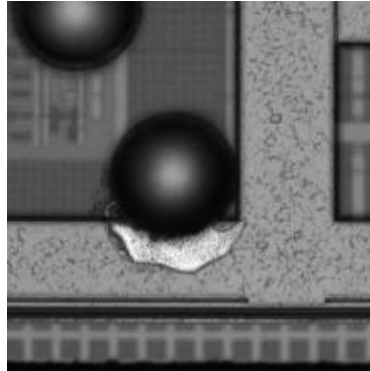
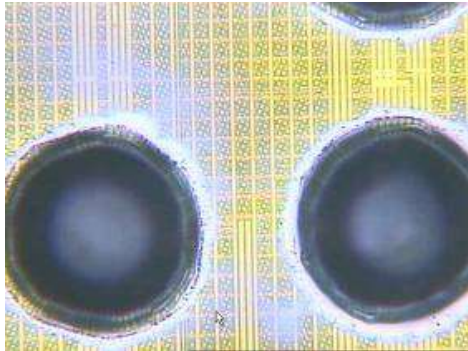
Figure 8D. Over reflow

**Fluxless reflow process:** Heat to T1 → Vacuum Chamber → Introduce Formic Acid → Vacuum Chamber → Backfill with N2 → Heat to T2 → Cool to RT

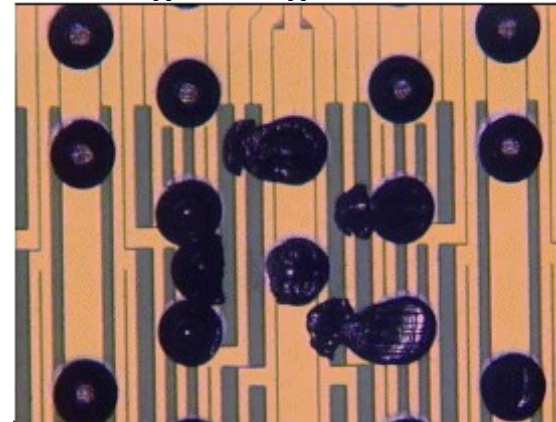
L. Jing, et al, "Impact of Process Parameters on Vacuum Fluxless Solder Reflow," 2023 ECTC

## C4 Fabrication Issues

Residual Seed



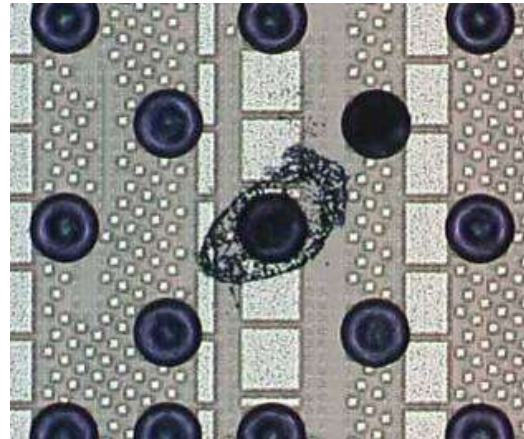
Handling Damage



Plating nodule:

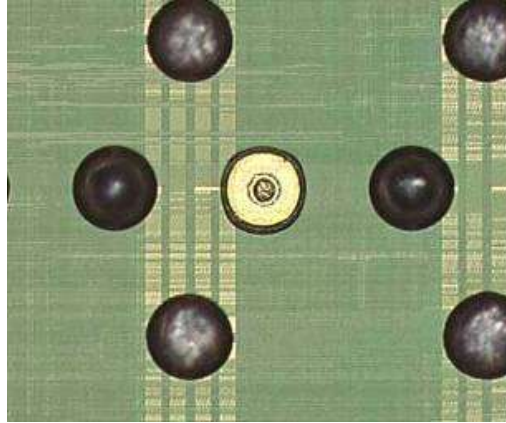


Contamination

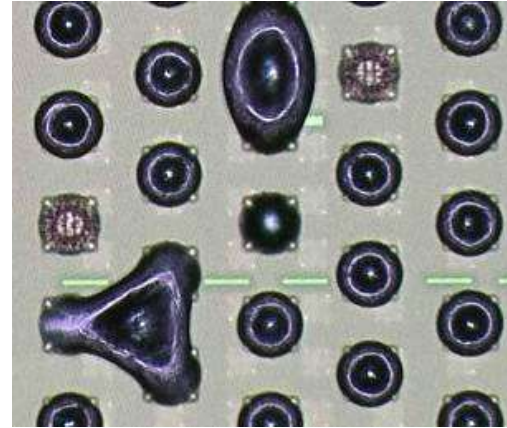


# C4 Fabrication Issues

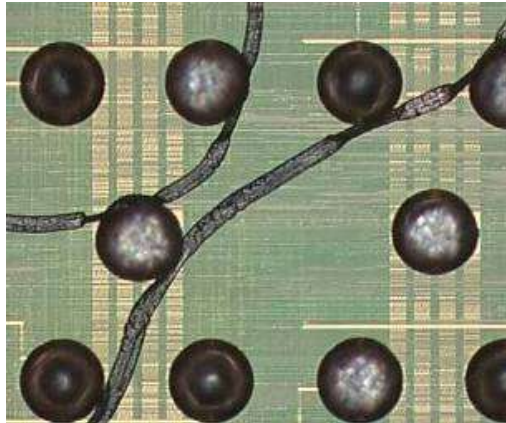
Missing C4:



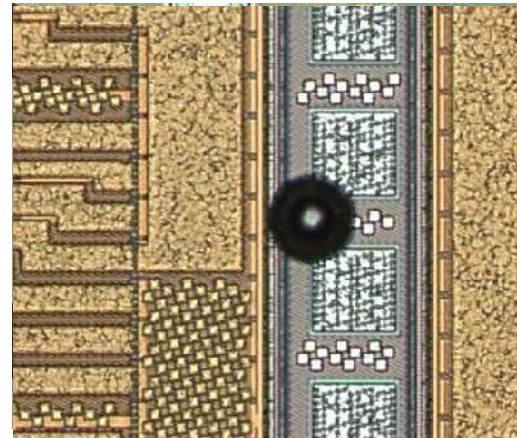
C4 Shorts:



Contamination:



Extra solder:



## Part 3: Pattern Electroplating Summary

### Reviewed the Pattern Electroplating

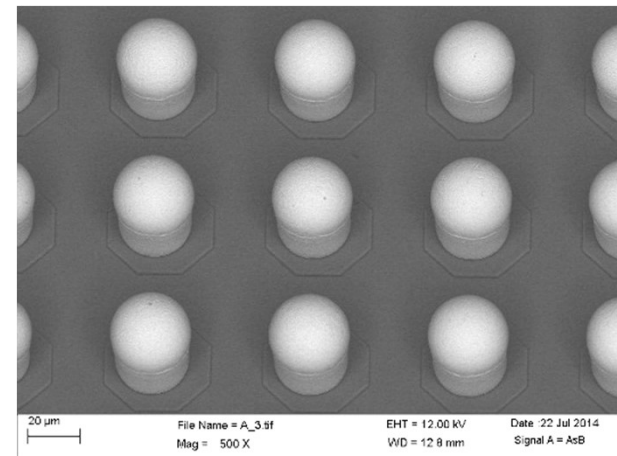
- Passivation: **SiN + SiO<sub>2</sub>** followed by **PSPI** (or PBO, BCB)
- Seed deposition: **Bake, RF clean, Ti + Cu sputter**; Key: film stress control
- Thick resist lithography: **apply → expose → develop → plasma clean**
- Electroplating sequence: **Cu → Ni → Cu → SnAg** (chemistry control critical)
- Final finishing: **O<sub>2</sub> plasma, formic-acid reflow, optical inspection**
- Defects & mechanisms:
  - Ag<sub>3</sub>Sn needles, interfacial voids, Kirkendall voids
  - Thermal undercut, solder wicking, resist lifting, seed undercut

# Flip-Chip Interconnect

## Part 4: Cu-Pillar Fabrication and Applications

Part 4 provides the understanding how Cu-pillar bumps enabled fine-pitch interconnects, customizable geometries, and advanced assembly methods such as mass-reflow and TCB/NCP. It covers key fabrication parameters, bump-on-trace joining modes, HBM introduction and process options for high-density packaging.

- Key Topics:
- Why Cu-Pillar?
  - Implementation in Assembly
    - Cu-Pillar Joining to Laminate
    - Cu-Pillar Joining to Si Interposer
  - HBM Driving u-Pillar Implementation



# Cu-Pillar Technology

## Lead Free Solder Bump Assembly

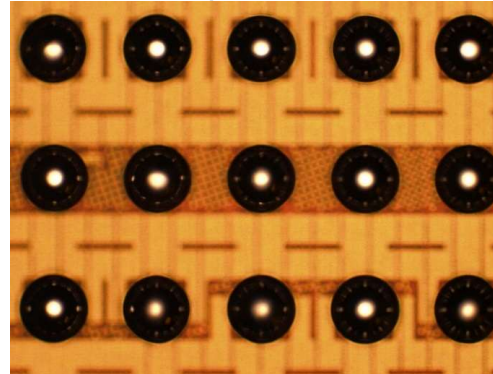
- Large Pitch ( $> 110\mu\text{m}$  with exceptions)
- Historically Large Die, now all sizes
- Bump Shape is not Customized
- Use Mass Reflow Assembly
- All application



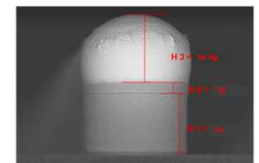
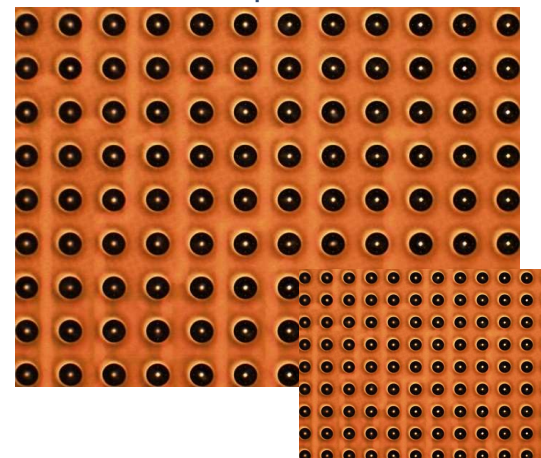
## Cu-Pillar Bump Assembly

- Very high-density bump / pitch (20 - 100 $\mu\text{m}$ )
- Mostly smaller die but no limit to it
- Highly customized bump shape (some oval)
- Mass reflow or thermal compression assembly
- On High-end with Si-on-Si or WLFO or Bridge
- Large pitch: Capillary underfill
- Fine pitch w/low solder volume: NCP with TCB

C4: 150  $\mu\text{m}$  pitch

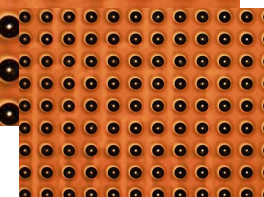


u-Pillar: 60  $\mu\text{m}$  pitch

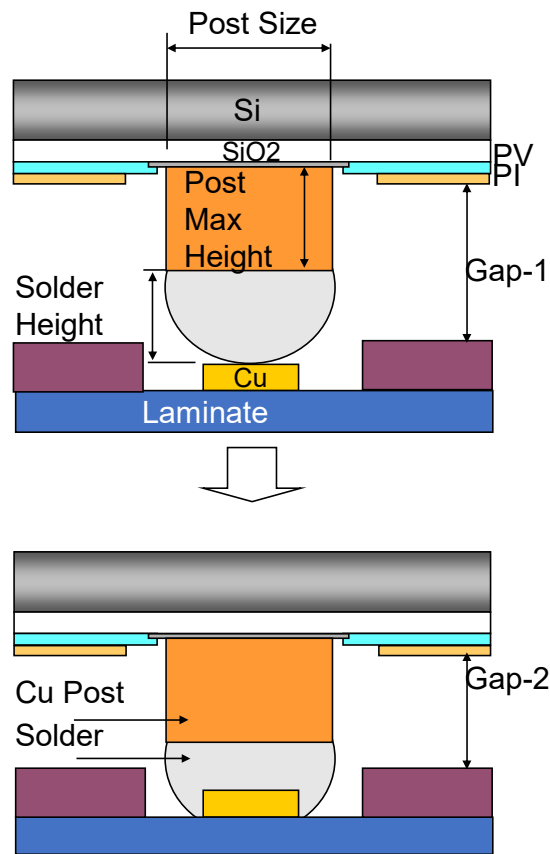


u-Pillar: 2011 → Future

u-Pillar: 30  $\mu\text{m}$  pitch



# Metal Post Solder-Chip Connection (MPS-C2)

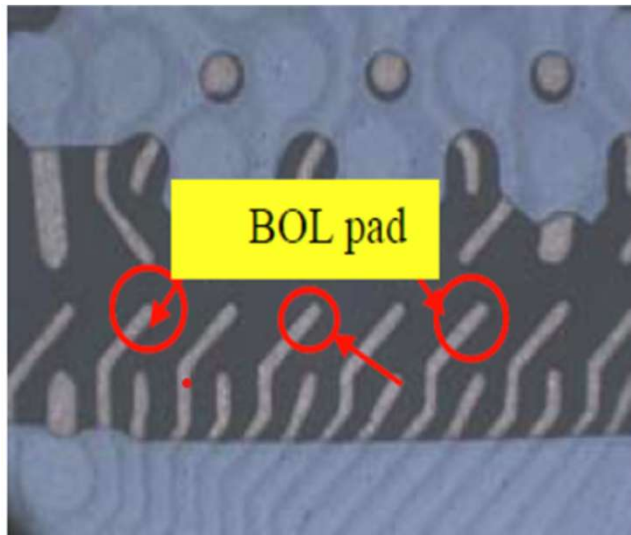


| Post Size (um) | Post Max Height (um) | Solder Max Height (um) | Bump Max Height (um) | Min Gap (Gap-2) |
|----------------|----------------------|------------------------|----------------------|-----------------|
| 45 x 45        | 26                   | 20                     | 46                   | 14              |
| 50 x 50        | 63                   | 25                     | 88                   | 53.5            |
| 55 x 55        | 61                   | 27.5                   | 88.5                 | 52.8            |
| 60 x 60        | 59                   | 30                     | 89                   | 52              |

## Elements:

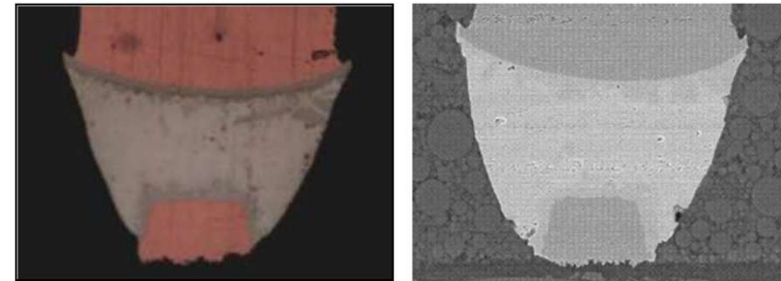
- Fine pitch connection: < 70 um
- No solder on Laminate side required
- Limited solder composition by electroplating
- Chip joining utilizes Mass Reflow (MR)

# Bond-on-Line (BoL) and Bond-on-Pad (BoP)

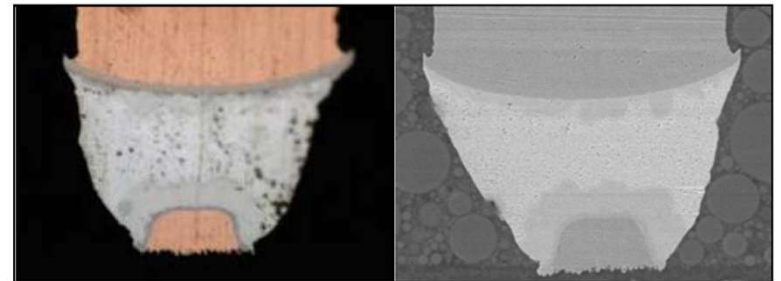


BoL process occurs when the chip is joined to the laminate Cu wiring directly followed by underfill.

It is the first Implementation of u-pillars with molded underfill.



(a) Cross-section image after HTST 1500hrs

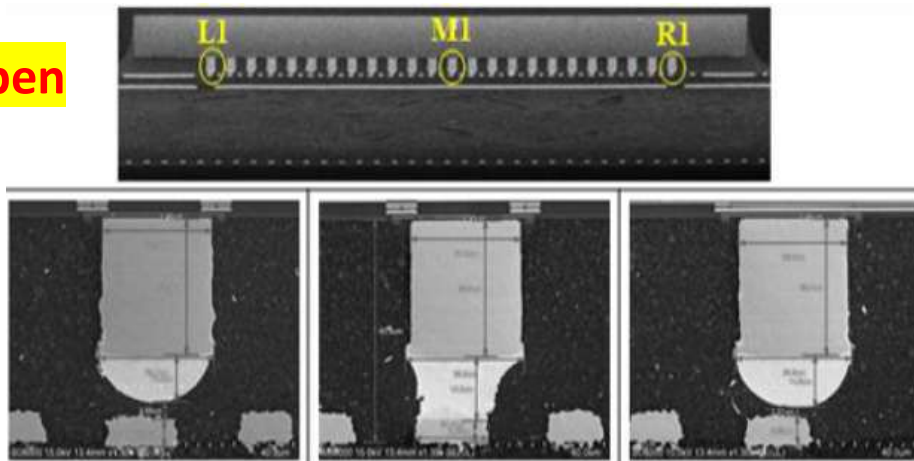


(b) Cross-section image after TC 1500 cycles

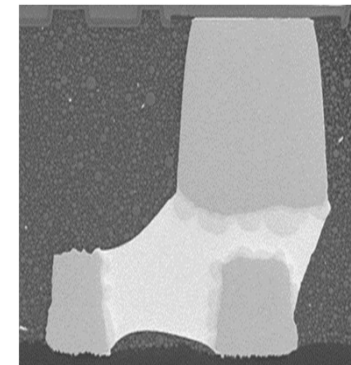
# Mass Reflow Process Abnormalities

Effect of Substrate Warpage (and differential CTE) at Joining:

Open



Short



Pitch and Bump Size

For large dies TCB is needed to minimize laminate warpage.

# TC/NCP Flip-Chip Qualification and Reliability

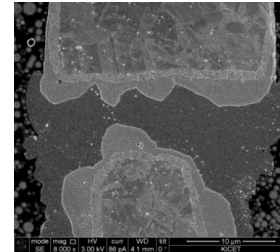
## Conditions

| Test Items | Precon                           | Condition   | Read points |
|------------|----------------------------------|-------------|-------------|
| T & H      | MSL3                             | 85°C/85%RH  | 1000hrs     |
| uHAST      | 30°C/60%<br>RH-192hrs<br>260°C3X | 130°C/85%RH | 96hrs       |
| TCB        |                                  | -55°C/125°C | 1000X       |
| HTS        |                                  | 150°C       | 1000hrs     |

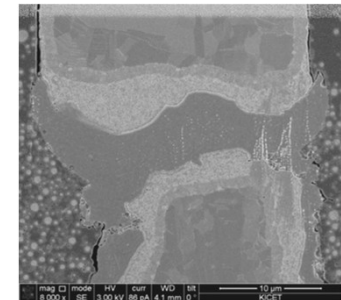
## Results

| Lot#          | Precon      | T & H       | uHAST       | TCB         | HTS         |
|---------------|-------------|-------------|-------------|-------------|-------------|
| 1             | 0 / 308     | 0 / 77      | 0 / 77      | 0 / 77      | 0 / 77      |
| 2             | 0 / 308     | 0 / 77      | 0 / 77      | 0 / 77      | 0 / 77      |
| 3             | 0 / 308     | 0 / 77      | 0 / 77      | 0 / 77      | 0 / 77      |
| Total         | 0 / 924     | 0 / 231     | 0 / 231     | 0 / 231     | 0 / 231     |
| <b>Result</b> | <b>Pass</b> | <b>Pass</b> | <b>Pass</b> | <b>Pass</b> | <b>Pass</b> |

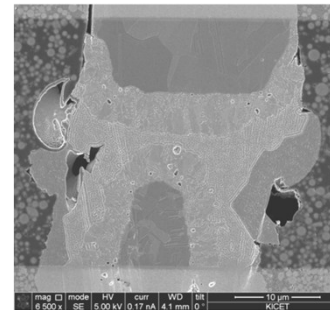
Superior board level drop performance.



uHAST 168 hours



TC 1000x



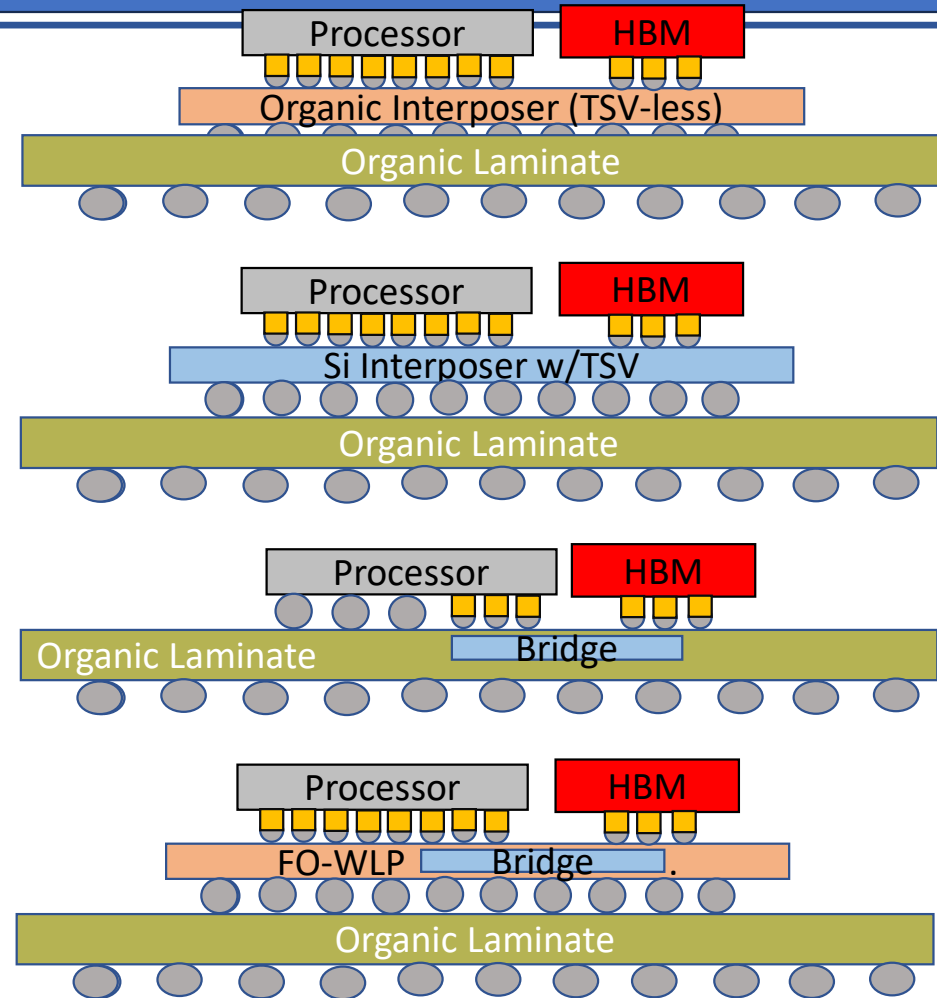
HTS 2000 hours

# HBM Interconnect Options w/Chip Last Approach

The introduction of HBMs with 55um Pitch / 30 um diameter Cu-pillar required advanced packaging:

- 1) High-performance laminate with organic RDL  
- iThop or Organic Interposer (RDL first FO-WLP)
- 2) Chip to Si interposer or to processor  
- 2.5D, 3D, CoWoS, Memory
- 3) Bridge technology  
- Intel EMIB, TSMC InFO-L

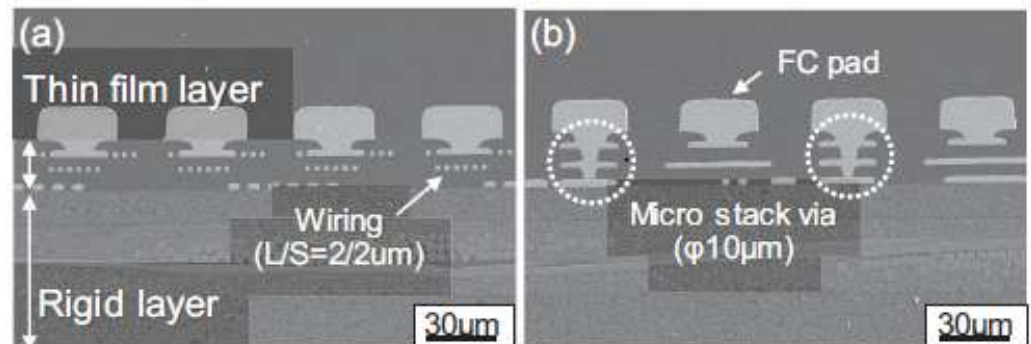
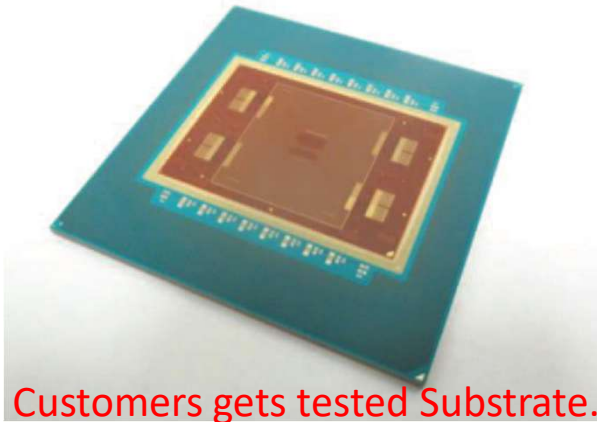
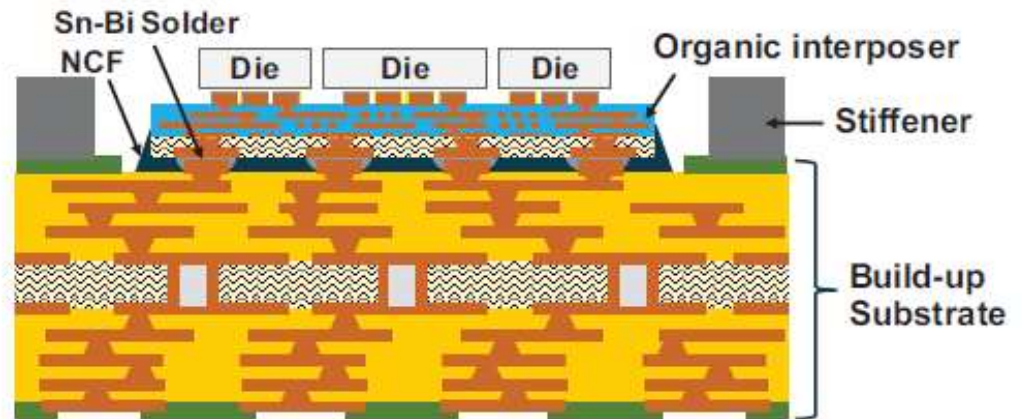
Note: Minimum laminate pitch limit is 90 um



## 2.3D Hybrid Laminate

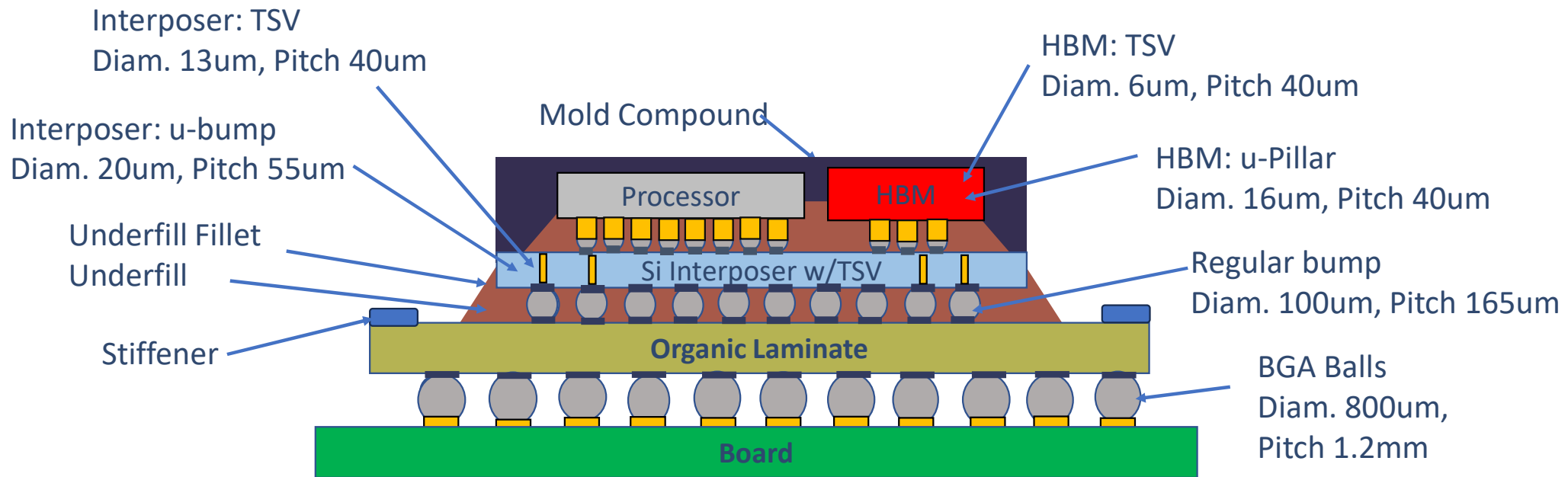
### Shinko's Integrated-Thin film High density Organic Package (i-THOP<sup>®</sup>)

To support 40um u-Pillar pitch HBM, a highly dense organic (2/2, L/S) RDL interposer was developed by Shinko. The Cu-Polyimide RDL is fabricated on rigid carrier, then diced and joined on to the laminate using SnBi solder.



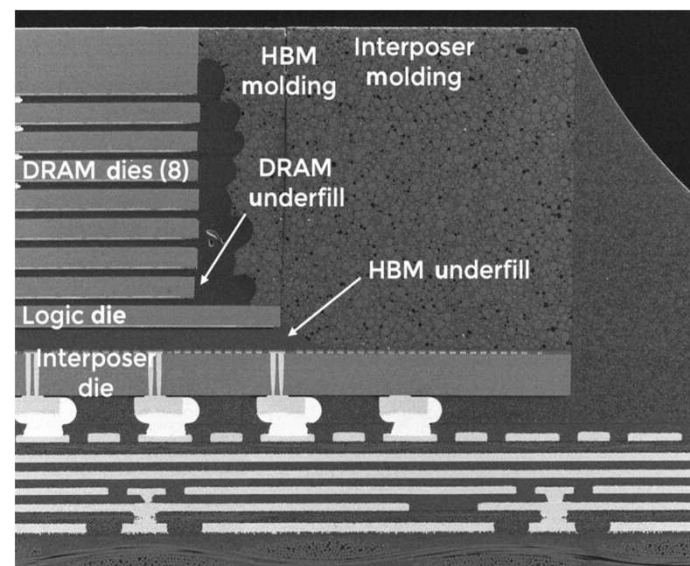
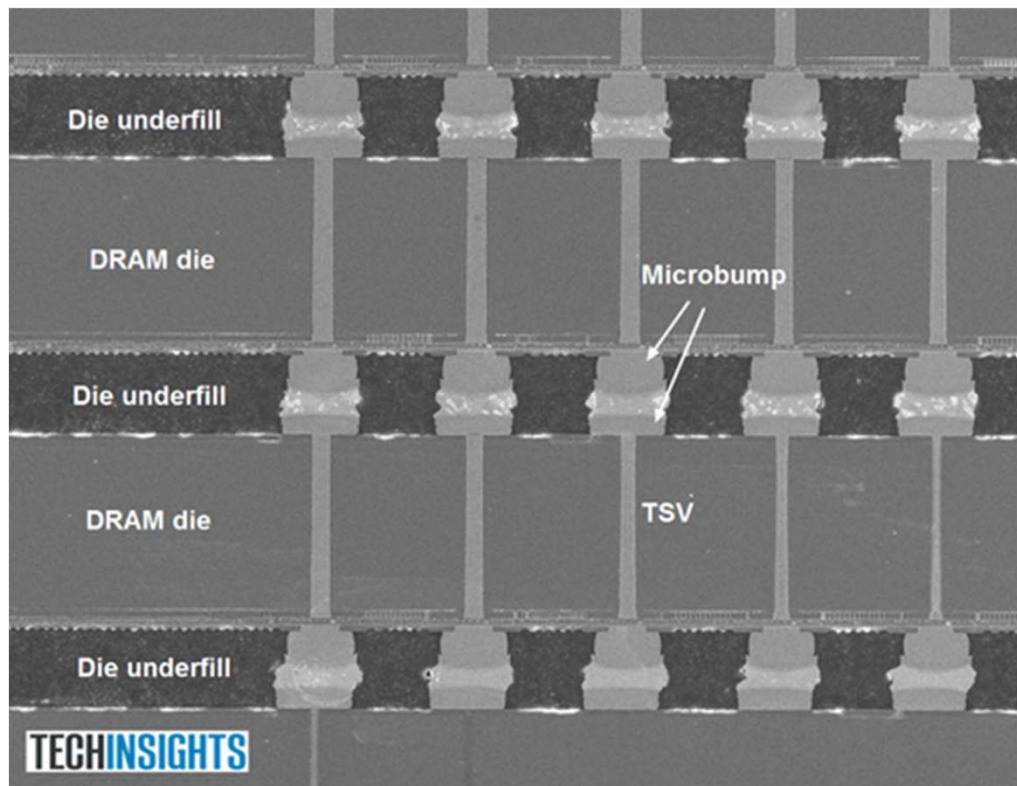
Y. Kobayashi, et al, "Reliability and Warpage of High Density Package using Organic Interposer for Heterogeneous Integration," ICEP-IAA 2025

# Applications Today: Si Interposer

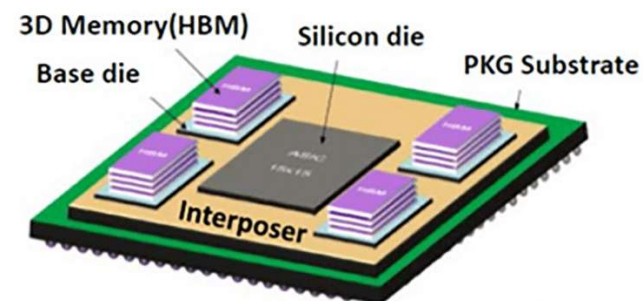


Flip-Chip Interconnection: 4 Solder Bump Pitches; 2 TSV Pitches; 3 Carriers; 2 Underfills  
(not to scale)

# HBM: TCB/NCP with Cu u-Pillar



YOLE  
SystemPlus



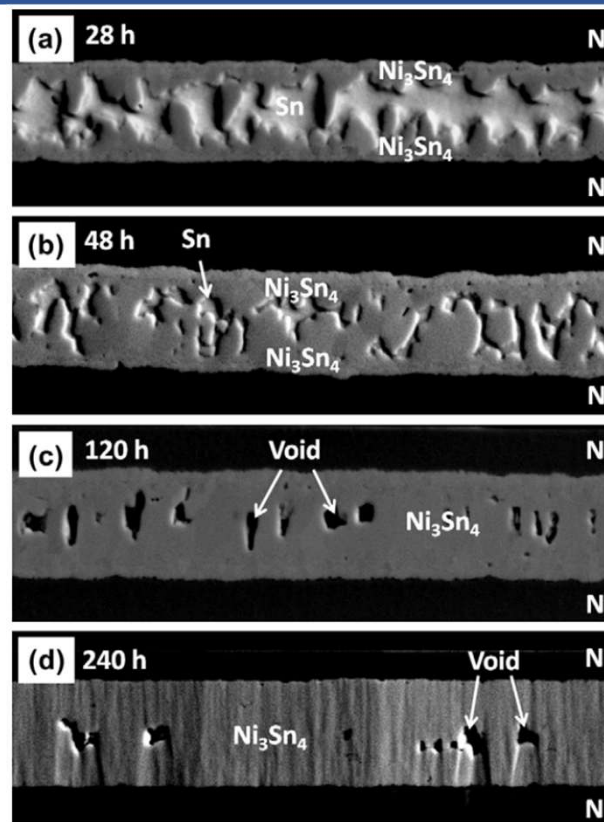
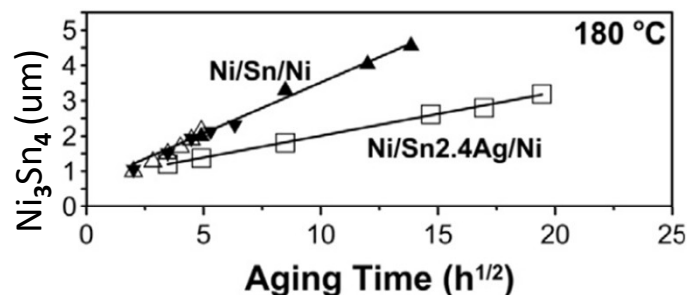
# Elimination of Voids in Ni / Sn / Ni System

## Mechanism:

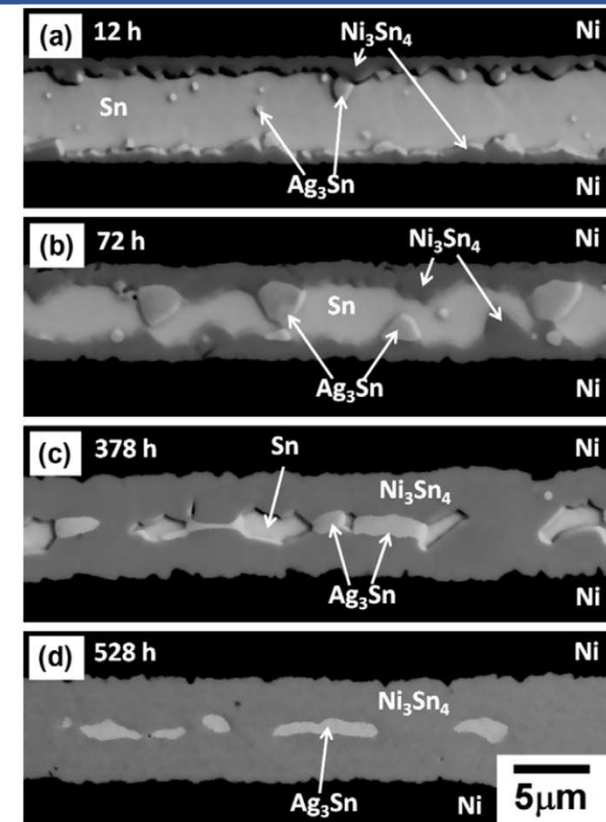
- Volume reduction voids during the  $\text{Ni}_3\text{Sn}_4$  IMC formation concentrate at the bonding interface.

## Solution:

- Incorporating 2.4% Ag in the solder slows the IMC formation allowing  $\text{Ag}_3\text{Sn}$  to aggregate at the bonding interface.



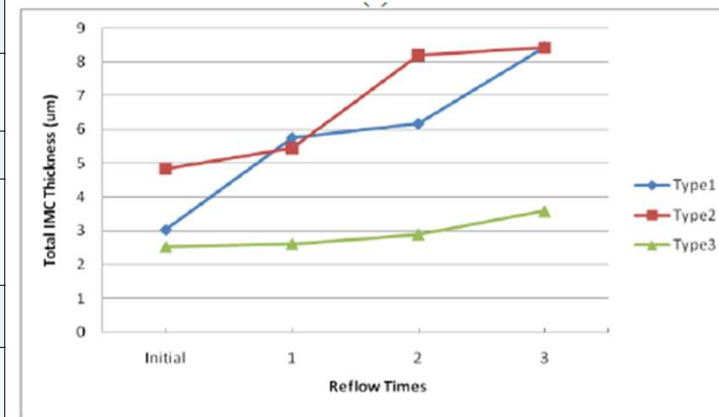
Ni/Sn(7  $\mu\text{m}$ )/Ni



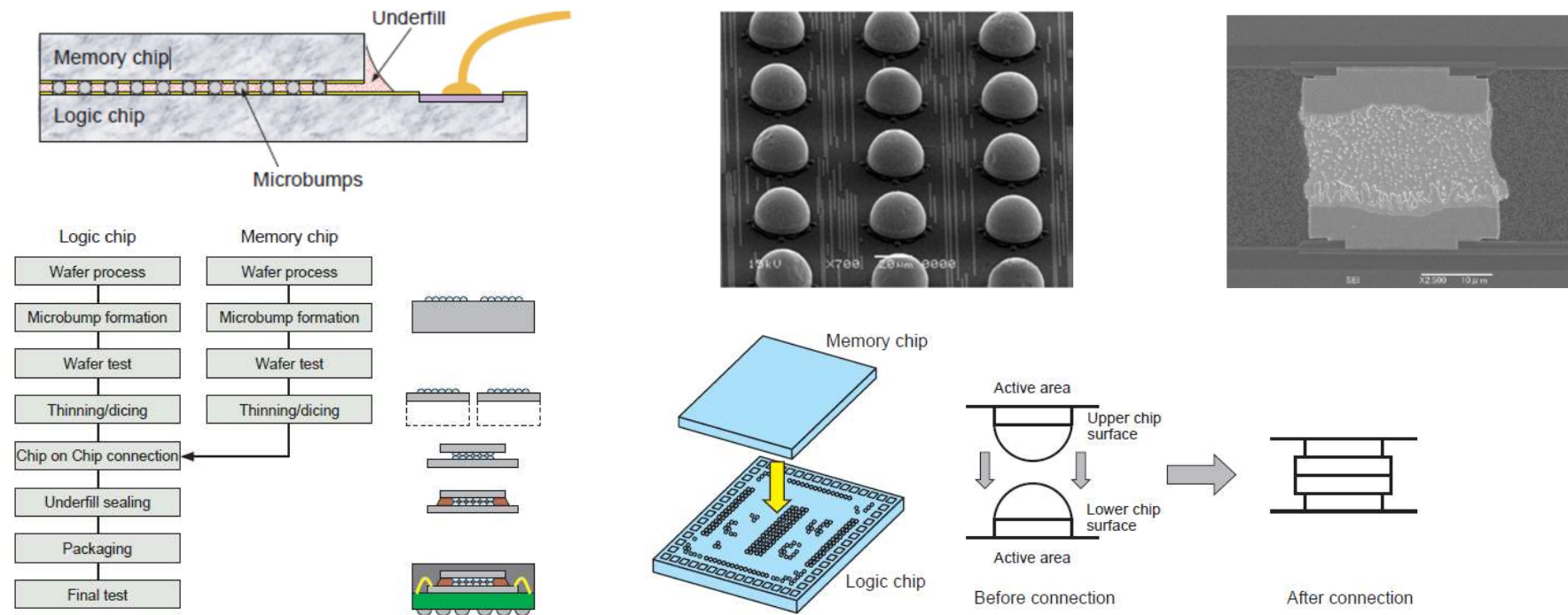
Ni/Sn2.4Ag(7  $\mu\text{m}$ )/Ni

# Memory Stack UBM Assessment: 180C HTS

|                 | Type1                                           | Type2                                         | Type3               | Type4                |
|-----------------|-------------------------------------------------|-----------------------------------------------|---------------------|----------------------|
| Front side bump | Cu /SnAg                                        | Cu/Ni/SnAg                                    | Cu/Ni/SnAg          | Cu/Ni/SnAg           |
| Back side bump  | Cu/thin Ni/Au                                   | Cu/thin Ni/Au                                 | Cu/thick Ni/Au      | Cu                   |
| Test results    | Failed after 504hr                              | Failed after 1400hr                           | Passed until 2016hr | Failed after 672hr   |
| Failure site    | Front bump                                      | Back bump                                     | -                   | Back bump            |
| Failure mode    | Pop-up failure                                  | Interface delamination                        | -                   | IMC crack            |
| Root cause      | Excessive IMC growth by solder sidewall wetting | Sn diffusion due to insufficient Ni thickness | -                   | Excessive IMC growth |

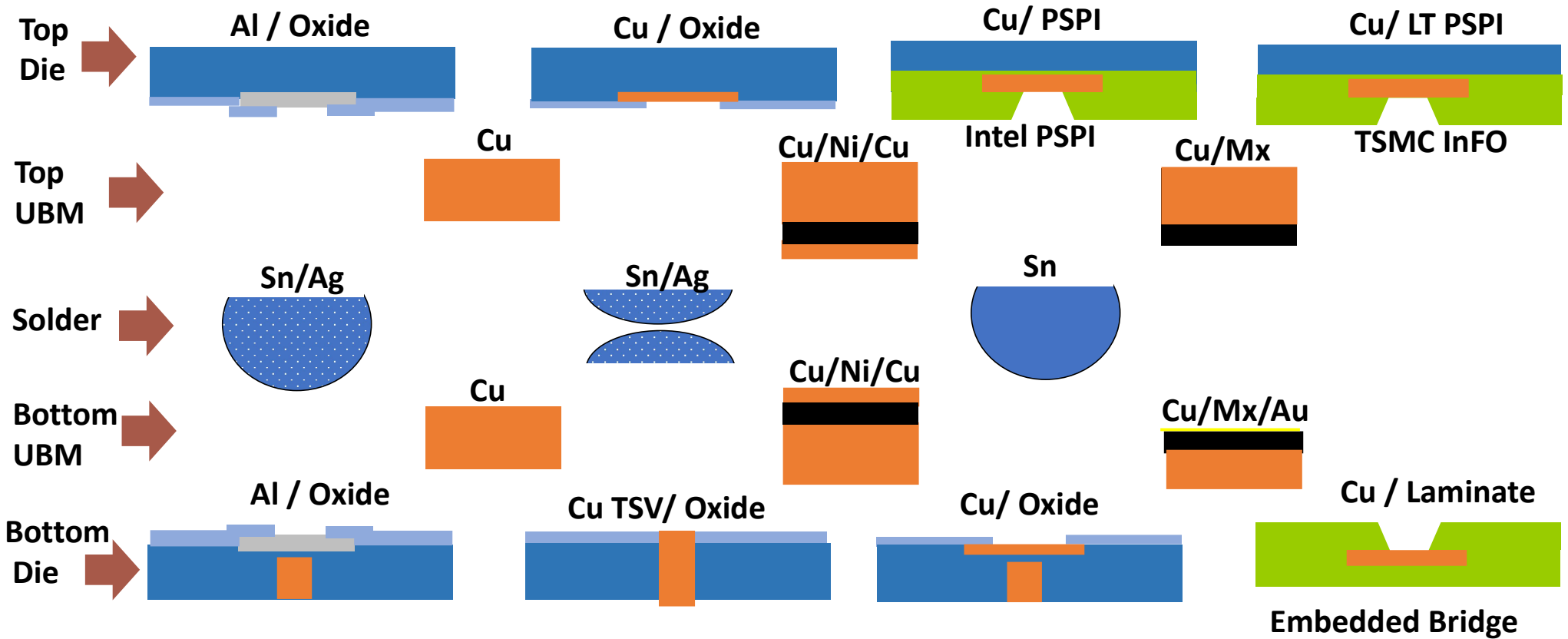


# First D2D interconnect: Sony with Solder-to-Solder Connection



Multi-Chip LSI (MCL) used in the early assembly of the CPU of Sony PlayStations. SnAg solder bump for both the logic and memory are 30 μm C4s with 60 μm pitch. Thermal compression bonding is used, having a misalignment of less than 3 μm (average + 3σ).

# Si-to-Si Interconnect: UBM / Solder Options



Mx = Ni, NiFe, Co, CoFe, NiCo - Goal is to minimize the IMC thickness

# 15 um Pitch: 5Cu / 5Sn / 2Ni(P)/Au

## Consideration for 15um Pitch, 8um Cu/Sn:

- IMC is 1.5 um so minimum solder height set to 5um.
- Ti adhesion layer undercut was too large resulting in pad lifting during seed wet etching. 1000A Ta layer etched by RIE replaced Ti seed layer; Cu seed thickness: reduced to 500A.
- TCB with excellent alignment tolerance is required: 20 MPa force and 350 C for 60 sec, with bottom substrate heated to 300C for Ni/Au UBM and 25C for Cu/Sn UBM.
- 5Cu/5Sn to itself - the TCB was 10 MPa and 350C for 30 sec, followed by mass reflow @265C.
- Fine particle filler was required in the underfill.

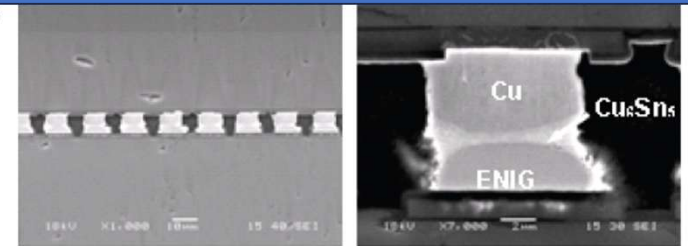


Fig. 8 Cross-section of micro joints with CuSn solder micro bump joined to ENIG

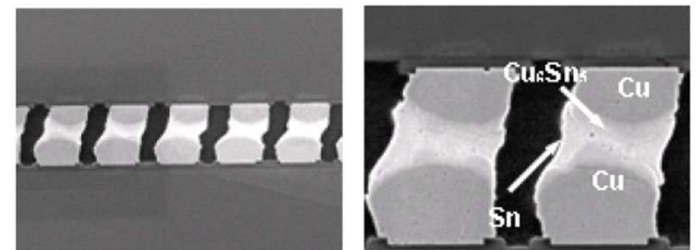
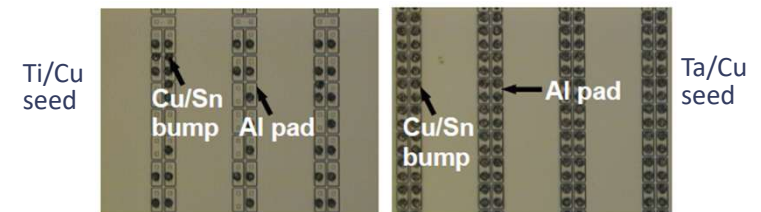


Fig. 10 Cross-section of micro joints with Cu/Sn solder micro bump joined to Cu/Sn solder micro bump



A. Yu, et al, "Study of 15μm Pitch Solder Microbumps for 3D IC Integration," 2009 ECTC

# Ni vs Ni/Pd/Au on u-Pillar System

## Microstructure :

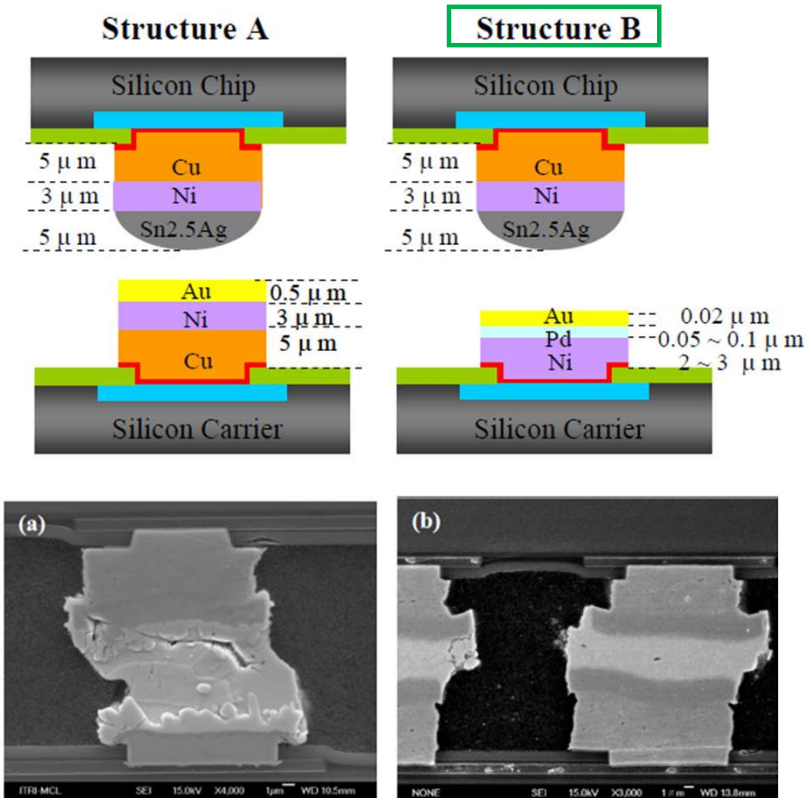
- Cu/Ni/SnAg/Au/Ni/Cu joint structure almost transformed into  $(\text{Au},\text{Ni})_x\text{Sn}_y$ -based IMC-like joint after bonding.
- Cu/Ni/SnAg/Au/Pd/Ni u-joint showed a very complicated morphology in IMCs distribution: large  $(\text{Pd},\text{Ni})\text{Sn}_4$  IMCs formed within the joined layer

## Thermal Cycle Test:

- Electrical failure occurred in the chip stack with Cu/Ni/SnAg/Au/Pd/Ni u-joints just after 250 cycles with crack forming in the interface of  $\text{Ni}_3\text{Sn}_4/(\text{Pd},\text{Ni})\text{Sn}_4$
- Cu/Ni/Sn/Au/Ni/Cu u-joints survived pass 1000 cycles.

## Electromigration:

- Cu/Ni/SnAg/Au/Ni/Cu and Cu/Ni/SnAg/Au/Pd/Ni u-joints showed excellent endurance during electromigration possibly due to IMC joint.

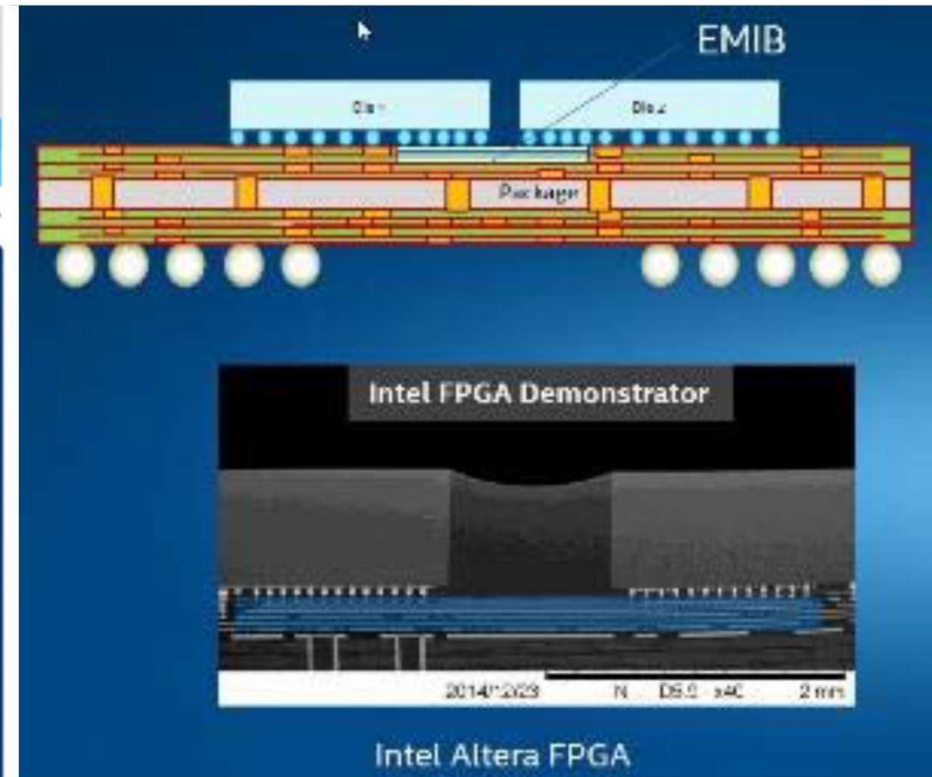
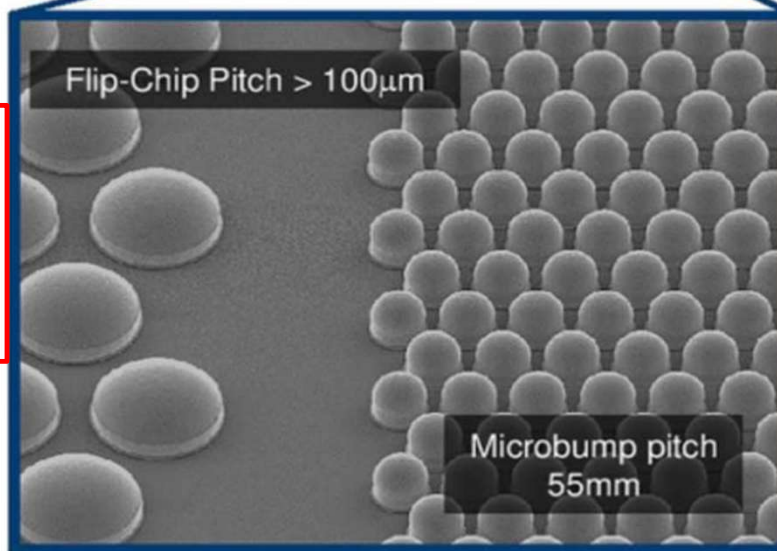


# Application: Si Bridge Technology

## Intel's Embedded Multi-die Interconnected Bridge (EMIB)

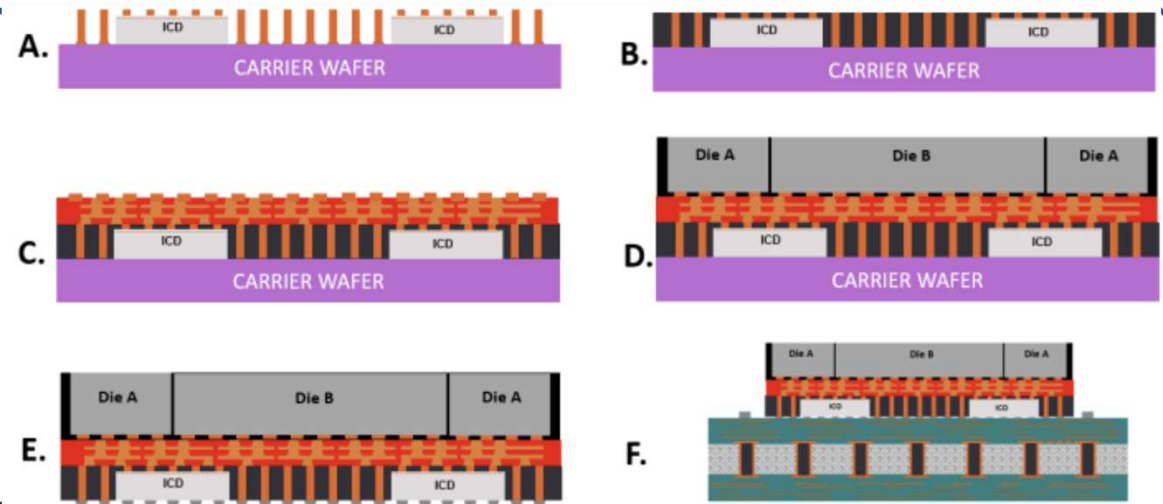
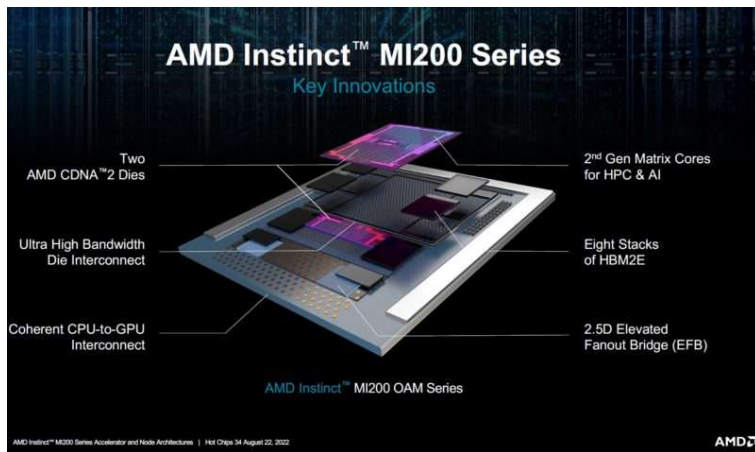


EMIB Bridge:  
75um thick Si  
BEOL metal process  
2um/2um L/S  
2um via size

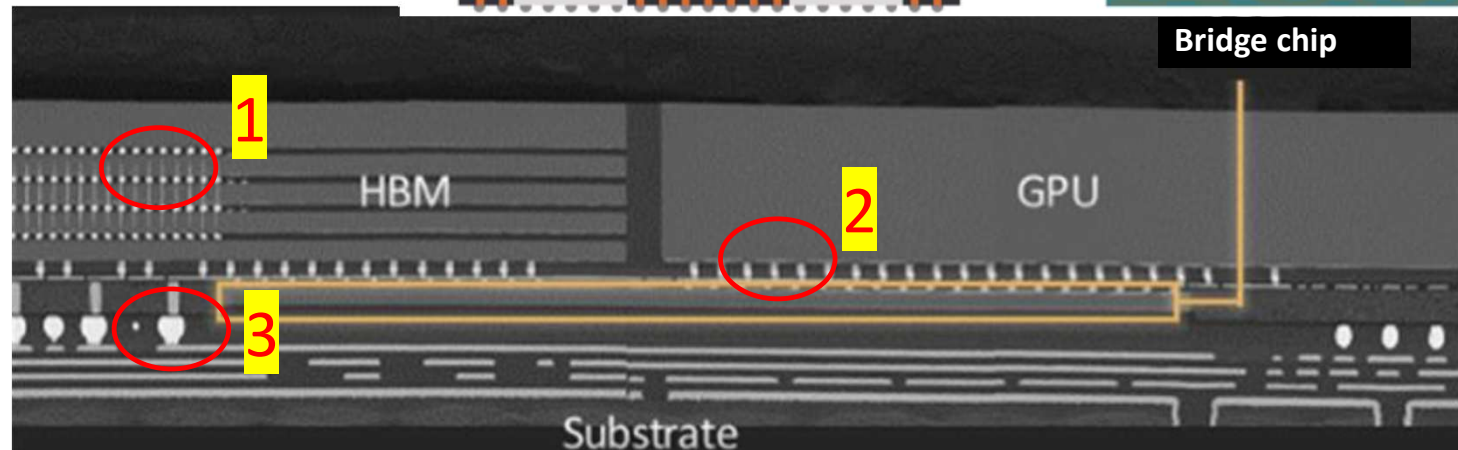


Dual flip-chip pitch is required, with 2 lithography and plating steps

# AMD MI200 w/Embedded Fan-Out Bridge



3 Flip Chip Levels:



# Flip-Chip C4 Pitch Evolution

| Theme                    | 2010–2015                            | 2016–2019                      | 2020–2023                      | 2024–2026                                                    |
|--------------------------|--------------------------------------|--------------------------------|--------------------------------|--------------------------------------------------------------|
| <b>Pitch scaling</b>     | 150–80 $\mu\text{m}$<br>C4 - Pillars | 40–55 $\mu\text{m}$<br>pillars | 30–20 $\mu\text{m}$<br>u-bumps | 20–10 $\mu\text{m}$ u-pillars (HBM, chiplets)                |
| <b>Reliability focus</b> | White bump                           | Solder fatigue                 | EM + IMC formation             | Substrate-dependent reliability; ultra-fine pitch EM studies |
| <b>Bonding methods</b>   | Reflow                               | Reflow + TCB                   | TCB optimization               | Copper paste dip-bonding; hybrid bonding integration         |
| <b>Electroplating</b>    | PbSn → SnAg                          | Basic Cu and SnAg              | Additive control               | Accelerator–suppressor–leveler systems for u-pillar arrays   |
| <b>Applications</b>      | Flip-chip                            | Flip-chip                      | HBM, 2.5D interposers          | Chiplets, HBM, 3D stacking, UCle ecosystems                  |
| <b>Industry drivers</b>  | Servers                              | Mobile SoCs                    | AI accelerators                | Chiplet architectures, HBM4, 3D logic stacking               |

# Part 4: Cu-Pillar Fabrication and Applications Summary

## Part 4: Cu-Pillar Fabrication and Applications

### Cu-Pillar: Why It Matters

- Enabled **fine-pitch interconnects (20–100  $\mu\text{m}$ )** beyond LF solder limits
- **Customizable bump geometry** for electrical + mechanical optimization
- Enabled the introduction of HBM at 55um pitch

### Key Technology Elements

- **Cu post + Ni + Cu + SnAg solder cap** is the preferred structure for Cu-pillar
- **Cu post + Ni + SnAg solder cap** is the preferred structure for u-pillar
- Joining modes: **Bump-on-Trace, Bump-on-Line, Si-to-Si interconnect, Si to Laminate**

### HBM Implementation Options

- Advance substrates: iTHOP and Organic interposers
- Interposer: **organic vs Si interposer**
- Bridge technology on Laminate
- Bridge technology on FO-WLP

# Flip-Chip Interconnect

## Part 5: Solders, Electromigration and Reliability

Part 5 provides an understanding on how solder composition, microstructure, and additives influence wetting, undercooling, fatigue, and long-term reliability. It describes chip-package Interaction failure modes, white-bump mechanisms, and electromigration physics needed to evaluate and design robust flip-chip interconnects.

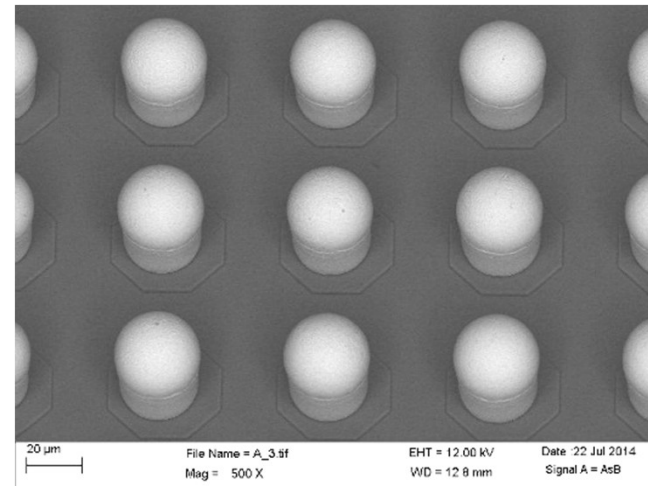
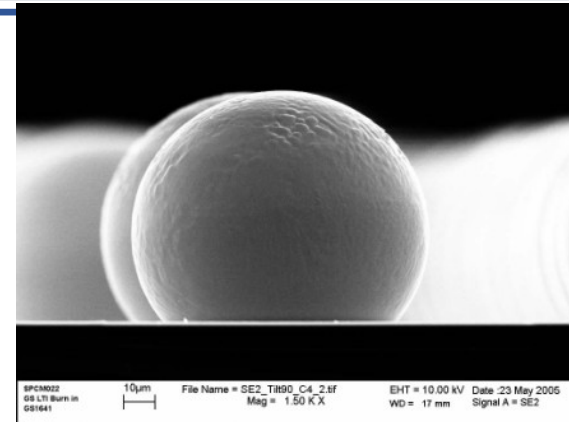
### Key Topics:

- Solder Selection
- Chip-Package Interaction
- White Bump
- Flip-Chip Reliability Assessment, Failure Modes
- Flip-Chip Electromigration consideration

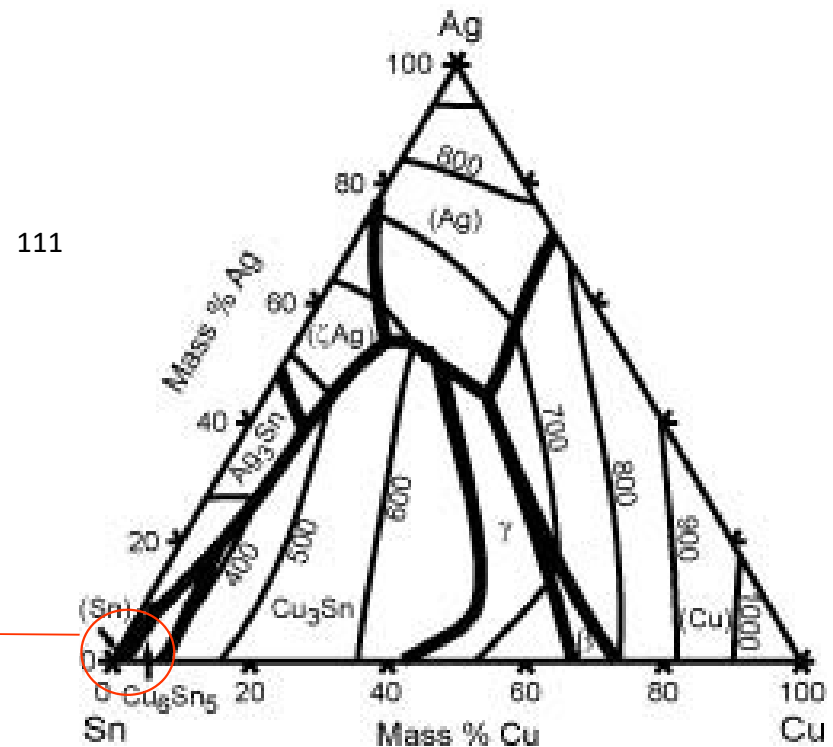
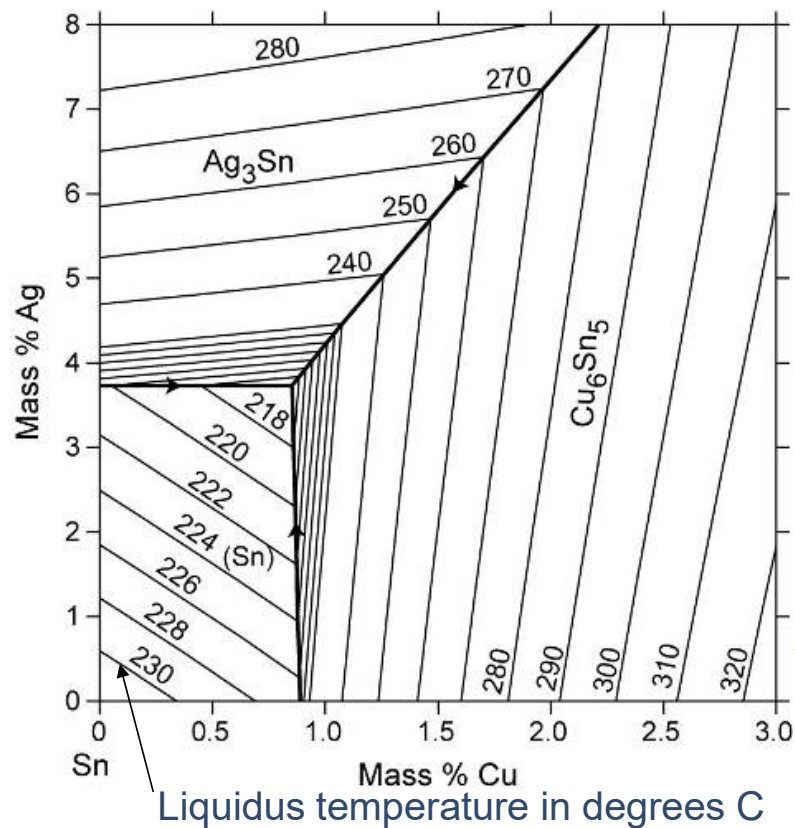
# Solder Selection and Other Considerations

- Wetting & Spreading
- Surface Tension
- Oxidation Resistance
- Micro-Hardness
- Tensile Properties
- Undercooling
- Melting Temperature
- Electrical Conductivity
- Thermal Conductivity
- Alpha Emission Rate
- Reliability
- Electromigration
- Corrosion Resistant
- Fatigue Performance

SAC = SnAgCu solder



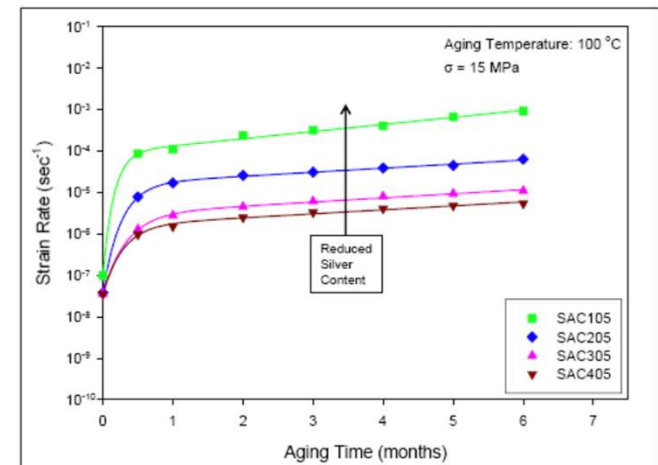
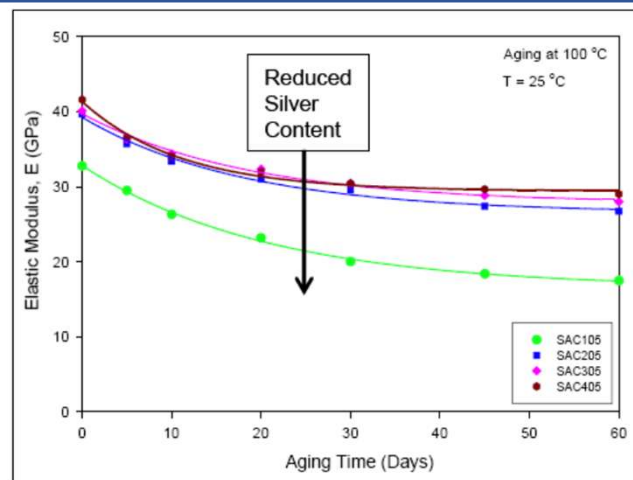
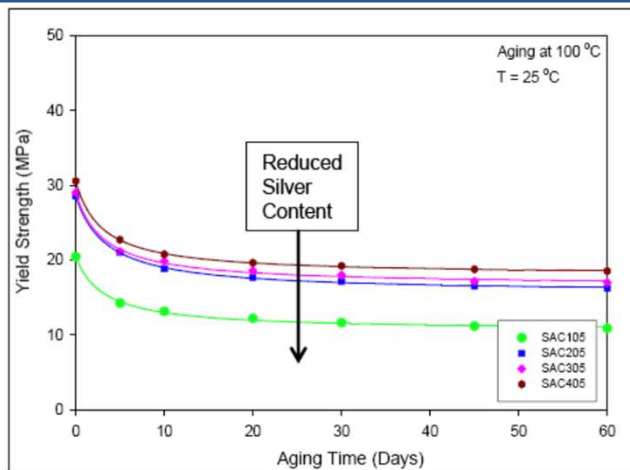
# Sn-Ag-Cu Solder Ternary Phase Diagram



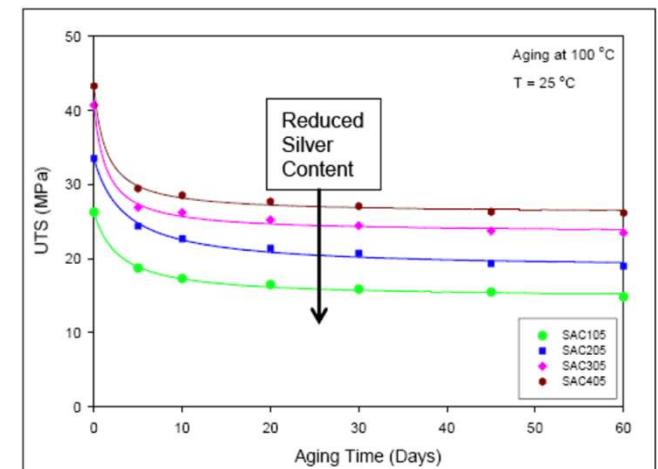
➔ Reflow temperature should be 15 C higher than the liquidus temperature

<http://www.metallurgy.nist.gov/phase/solder/agcusn.html>

# BGA: Lead Free Solder Aging Effects



- Mechanical Properties of SAC solder changes significantly with time. This aging effect can affect the values used for modeling the interconnect.
- Bi addition to the solder stabilizes the Sn grain structure reducing aging issues.



Z. Cai, et al, "Reduction of Lead-Free Solder Aging Effects Using Doped SAC Alloy," 2010 ECTC, and Jeff Suhling, 2018 EPTC Invited paper

# Solder Additives for Various Applications

Solders additives can moderate the solder properties and enhance the solder performance for specific applications:

- Reduced liquidus temperature: Bi, In
- Reduced undercooling: Al, Bi, Co, Sb, Zn
- Reduce Kirkendall voids: Ni, Co, Zn
- Increase drop resistance: Pt, Ni, Co, Zn, Ce
- Increase creep resistance: Bi, Ce, La, Sb, Ni
- Increase of shear strength: Co, Ni, Zn

However, solders additives, such as Zn, Ni, and Fe tend to oxidize reducing the solder wetting properties.

Some solder additives tend to migrate to the solder surface, at reflow, resulting in poor wetting characteristics.

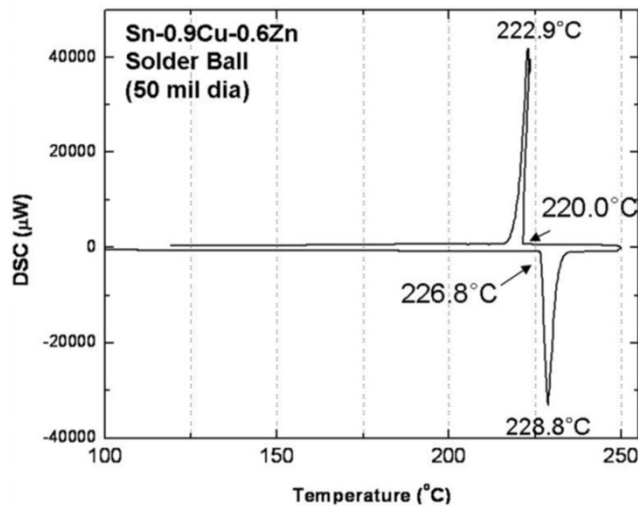
*Lead-free Electronic Solders: A Special Issue of the Journal of Materials Science:  
Materials in Electronics* By K. N. Subramanian, Springer (2007)

# Solder Additives and Undercooling

Solder undercooling is the temperature difference between the solder's equilibrium melting point and the actual temperature at which solidification begins.

$$\Delta T = T_{\text{liquidus}} - T_{\text{nucleation}}$$

A solder can be cooled below its melting point and still remain liquid until a solid nucleus forms.



| Solder composition (wt.%) | Melting temp. during heating, T1 (°C) | Peak temp. during cooling, T2 (°C) | Required undercooling, $\Delta T$ (T1 - T2) (°C) |
|---------------------------|---------------------------------------|------------------------------------|--------------------------------------------------|
| Sn-3.8Ag-0.7Cu (SAC)      | 217.0                                 | 187.2                              | 29.8                                             |
| SAC + 0.1Zn               | 217.7                                 | 213.3                              | 4.4                                              |
| SAC + 0.7Zn               | 217.2                                 | 213.6                              | 3.6                                              |
| Sn0.9Cu-0.6Zn             | 226.8                                 | 220.0                              | 6.8                                              |
| Sn0.9Cu-0.3Fe             | 228.7                                 | 208.5                              | 20.2                                             |
| Sn0.9Cu-0.2Co             | 229.4                                 | 224.7                              | 4.7                                              |
| Sn-8Zn-3Bi                | 193.7                                 | 191.8                              | 1.9                                              |
| 100Sn                     | 232.6                                 | 217.5                              | 15.1                                             |
| 95Pb-5Sn                  | 305.6                                 | 302.4                              | 3.2                                              |
| 100Pb                     | 328.5                                 | 324.1                              | 4.4                                              |

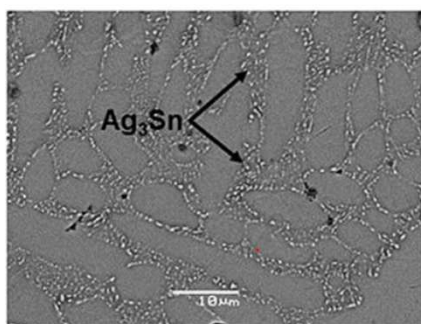
Bi and Zn additives significantly reduce the undercooling.

# Bumping for High Reliability Application

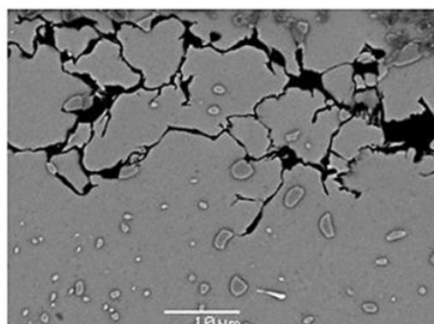
3<sup>rd</sup> Generation Pb-free solder for Auto and Aerospace applications requires TC -40 to +150C. Under this conditions recrystallization and crack propagation failure mode occurs on traditional 305 SAC solders.

Solder providers are developing a new generation of solders with additives (such as Bi, Sb, In) in conjunction with dopants (such as Ni, Co, Zn) for these harsh environments.

Ag<sub>3</sub>Sn intermetallic precipitate coarsening that precedes recrystallization and crack propagation during thermal cycling.



SAC305 as solidified



SAC305 after thermal cycling

J. W. J. Liu, "High-Reliability Pb-Free Solder Alloys for Automotive and Aerospace Electronics," J. Mater. Sci.: Mater. Electron., vol. 29, 2018.

Tradenames and Nominal Composition (wt. %) of High Reliability Solder Alloys

| Alloy           | Developer | Sn    | Ag   | Cu  | Bi  | Sb  | In  | other         |
|-----------------|-----------|-------|------|-----|-----|-----|-----|---------------|
| 405Y            | Inventec  | 95.5  | 4.0  | 0.5 |     |     |     | 0.05 Ni; Zn   |
| Cyclomax (SACQ) | Accurus   | 92.8  | 3.4  | 0.5 | 3.3 |     |     |               |
| Ecalloy         | Accurus   | 97.3  |      | 0.7 | 2.0 |     |     | 0.05 Ni       |
| HT1             | Heraeus   | 95.0  | 2.5  | 0.5 |     |     | 2.0 | Nd            |
| Indalloy 272    | Indium    | 90.0  | 3.8  | 1.2 | 1.5 | 3.5 |     |               |
| Indalloy 277    | Indium    | 89.0  | 3.8  | 0.7 | 0.5 | 3.5 | 2.5 |               |
| Indalloy 279    | Indium    | 89.3  | 3.8  | 0.9 |     | 5.5 | 0.5 |               |
| Innotot         | Heraeus   | 91.3  | 3.8  | 0.7 | 3.0 | 1.5 |     | 0.12 Ni       |
| LF-C2           | Nihon     | 92.5  | 3.5  | 1.0 | 3.0 |     |     |               |
| M794            | Senju     | 89.7  | 3.4  | 0.7 | 3.2 | 3.0 |     | Ni            |
| M758            | Senju     | 93.2  | 3.0  | 0.8 | 3.0 |     |     | Ni            |
| MaxRel Plus     | Alpha     | 91.9  | 4.0  | 0.6 | 3.5 |     |     |               |
| PS48BR*         | Harima    | Bal.  | 3.2  | 0.5 | 4.0 | 3.5 |     | Ni, Co        |
| REL22*          | AIM       | Bal.  | 3.0  | 0.7 | 3.0 | 0.6 |     | 0.05Ni; other |
| REL61*          | AIM       | Bal.  | 0.6  | 0.7 | 2.0 |     |     |               |
| SB6NX           | Koki      | 89.2  | 3.5  | 0.8 | 0.5 |     | 6.0 |               |
| SN100CV         | Nihon     | 97.8  |      | 0.7 | 1.5 |     |     | 0.05Ni        |
| SN100CW1        | Nihon     | 95.8  |      | 0.7 | 1.5 | 2.0 |     |               |
| Violet          | Indium    | 91.25 | 2.25 | 0.5 | 6.0 |     |     |               |
| Viromet 347     | Asahi     | 88.4  | 4.1  | 0.5 |     |     | 7.0 |               |
| Viromet 349     | Asahi     | 91.4  | 4.1  | 0.5 |     |     | 4.0 |               |

\*Nominal values; actual composition proprietary

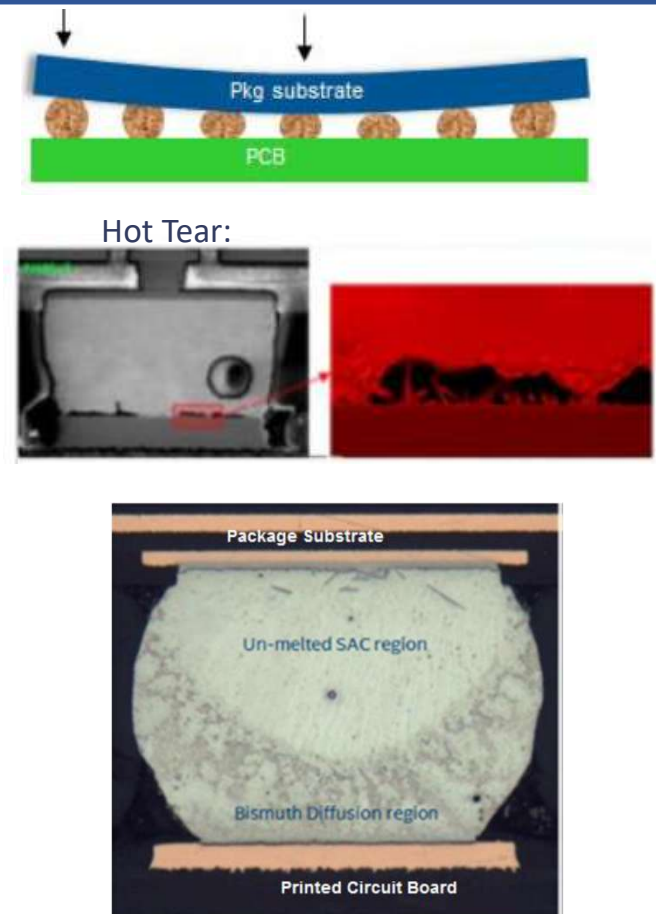
# Solid Liquid Inter-Diffusion (SLID) Interconnects

**Problem:** SnAg solder reflow temperatures of  $>240^{\circ}\text{C}$  result in high warpage during FO-WLP joining to BPC boards limiting package size. Increased FO-WLP size not only affects T0 joining, but package reliability.

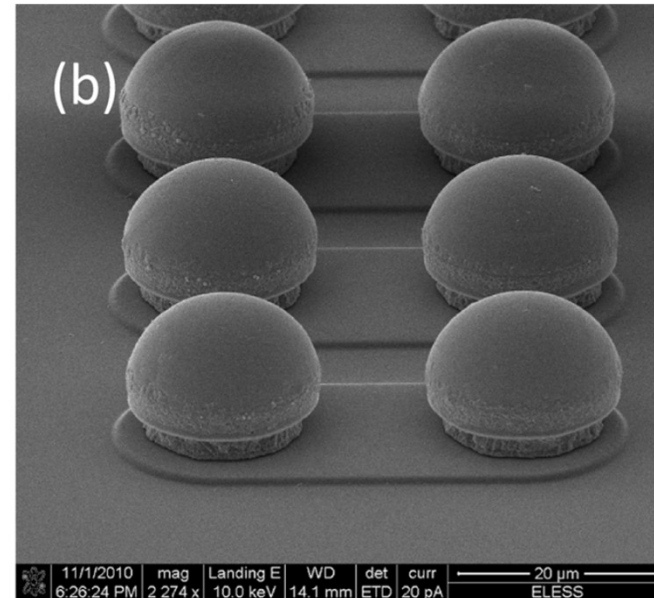
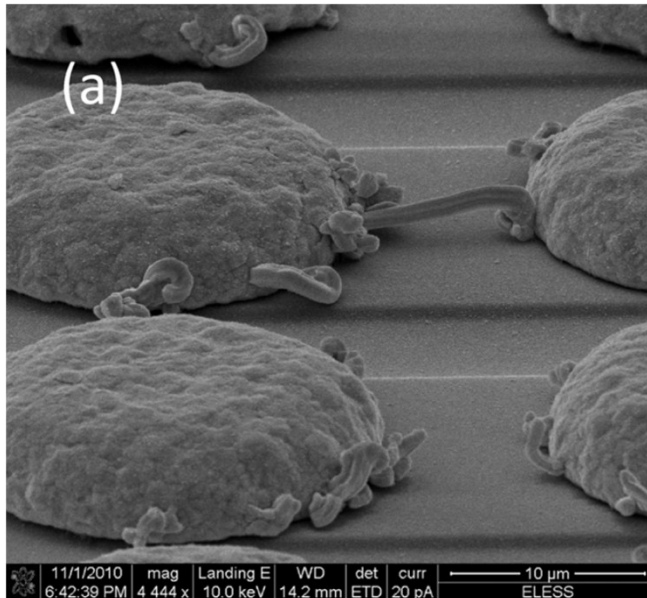
**Mitigation:** Industry is moving towards low temperature solder joining, in particular eutectic Sn58%Bi solders. This can be accomplished by:

- 1) Replacing SAC solders with SnBi (EM issues)
- 2) Depositing SnBi solder on the board and to enable low temperature joining ( $<180^{\circ}\text{C}$ ).

By selecting proper joining temperature/time the SnBi ratio can be optimized for best mechanical properties.



## No Sn Whiskers in Cu/Ni System



- (a) SEM image of a Sn whisker between two Cu bumps having a top layer of Sn, the whisker is a short.
- (b) Shows no Sn whisker when a Ni layer was added between the Cu bump and the top layer of Sn.

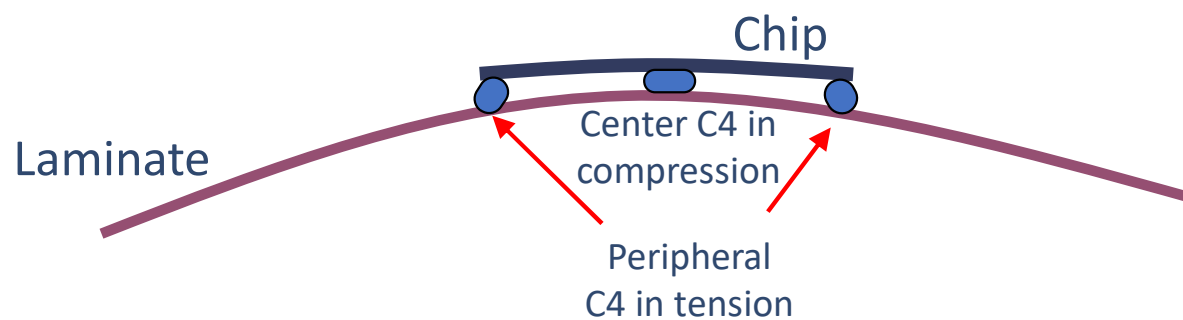
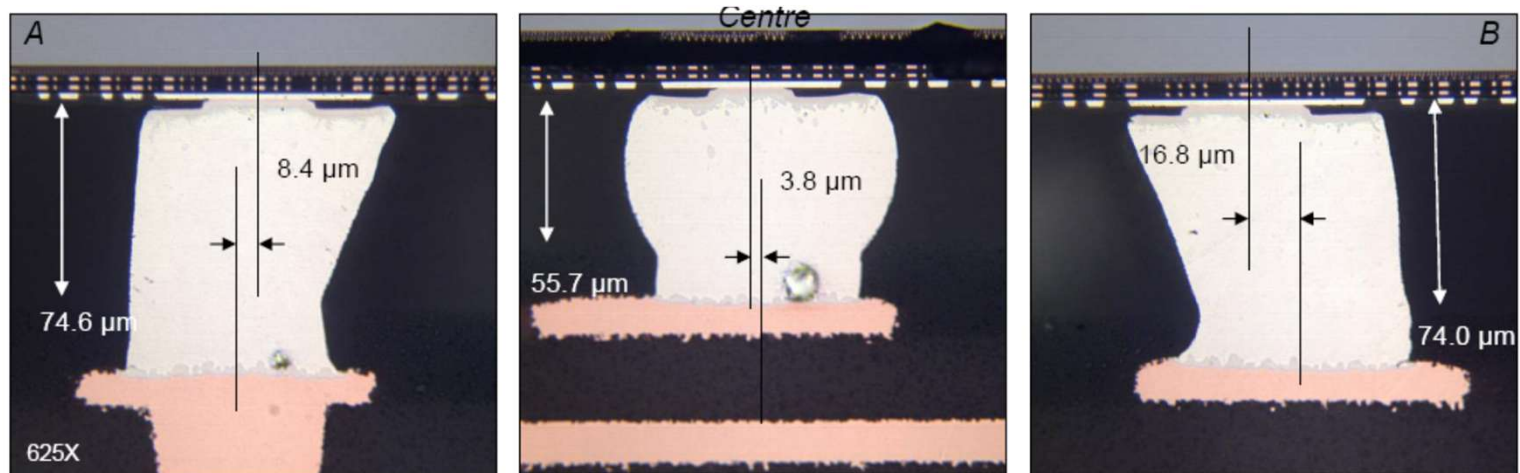
# Chip-Package Interaction (CPI)

Chip-package interaction is the interaction of stresses between the chip and the package that alters the strain state of solder joints, underfill, and BEOL layers, often leading to early failures such as cracking, delamination, or electrical opens.

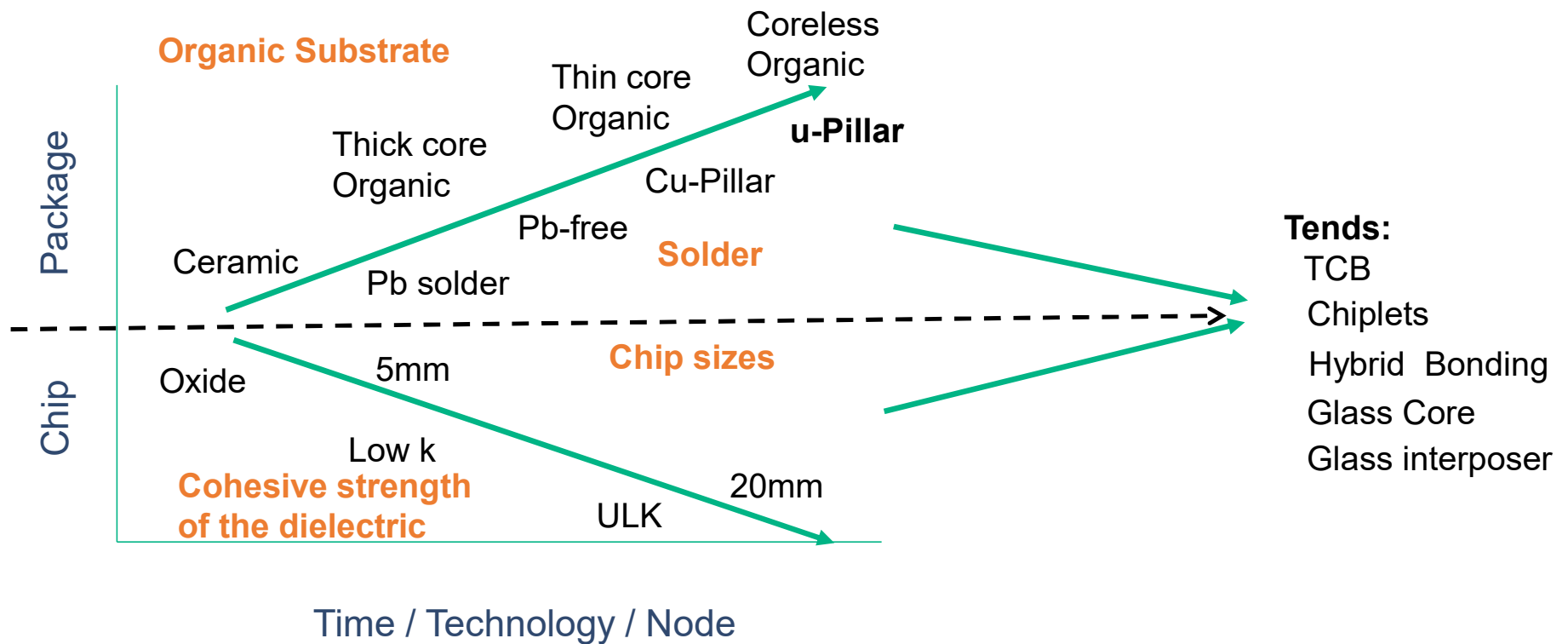
| CPI Stress Test               | What It Reveals                                |
|-------------------------------|------------------------------------------------|
| <b>Thermal Cycling (TC)</b>   | CTE mismatch, solder fatigue, IMC cracking     |
| <b>HTS</b>                    | IMC growth, UBM/passivation cracking           |
| <b>uHAST</b>                  | Moisture-driven delamination, PI/PSPI failures |
| <b>Power Cycling</b>          | Die warpage, RDL cracking, bump fatigue        |
| <b>Mechanical Bend / Flex</b> | BEOL cracking, die-package-board interaction   |
| <b>Drop/Shock</b>             | Die-edge stress, underfill adhesion            |
| <b>Warpage Measurement</b>    | Assembly-induced opens/shorts                  |
| <b>Electromigration (EM)</b>  | IMC voiding, current crowding failures         |

Today Modeling plays a critical role in evaluating CPI weakness prior to fabrication and testing.

# Effect of Laminate Warpage



# Flip-Chip Package Trend Summary



# Reliability Concerns on FC-BGA

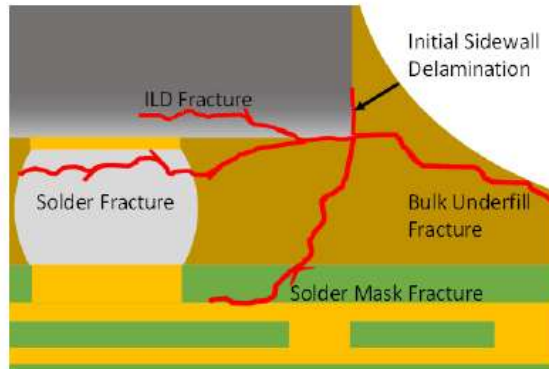
## White Bump:

Low-k Dielectric materials crack during chip joining (cooling) before underfill apply. Cracks observed by ultrasound show as white spot, known as white bump. Defect driven by CTE mismatch between laminate (18ppm) and Chip (2.7ppm), mainly on large area chips.

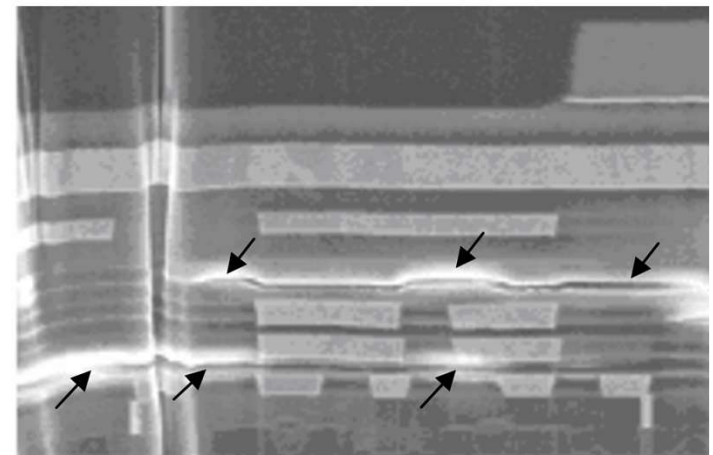
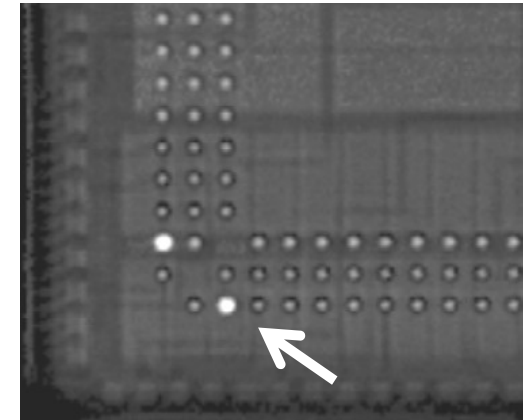
## Underfill Delamination:

Corner or edge Crack in underfill propagate to the C4 joints or to the laminate

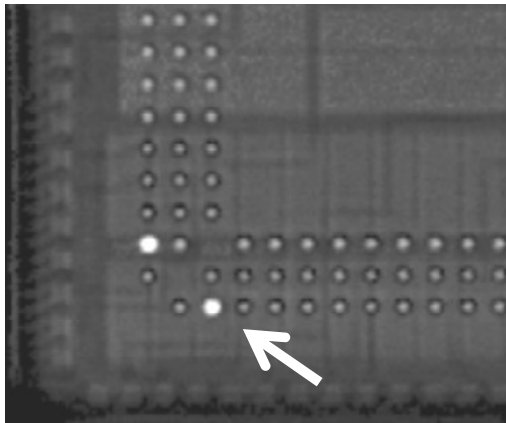
### Solder Cracks: Underfill Delamination



## Post Join CSAM:

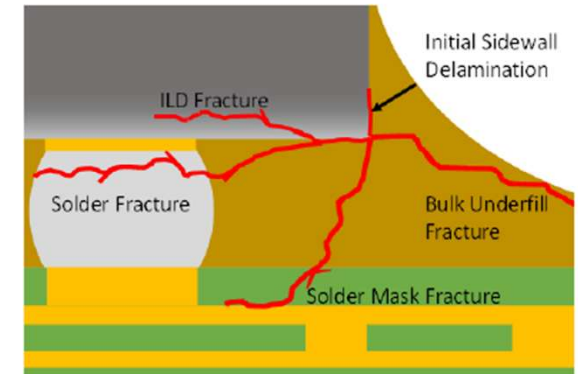
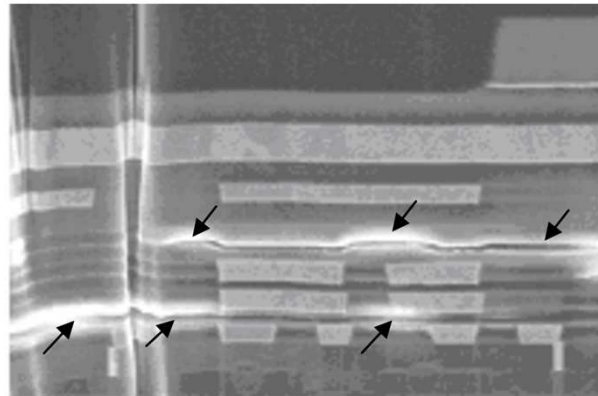


# ELK ILD Crack – White Bump



CSAM image – white spots

Cross-section of white bump:



J. Cremaldi, 2014 ECTC, p255.

## Problem:

BEOL dielectric stack under the u-bump caused by stress and warpage during initial joining reflow due to the chip and laminate CTE mismatch. Other source could be underfill fillet delamination during stress testing.

## Solution:

- TCB significantly reduced the CTE effects between the laminate and the chip through its differential heating and cooling. The laminate is kept at 100C which the chip in the TCB head is heated and cooled fast, minimizing the temperature delta.

# Bond and Assembly Variables Affecting White Bump

## F-BEOL Variables

- PSPI thickness
- PSPI via diameter
- Al pad thickness
- Al pad size
- PSPI via location
- Cu-Al layer via

## Laminate Variables

- Substrate CTE
- Wiring metal loading and distribution
- Solder mask opening
- Metallurgy: Cu OSP vs Ni/Au
- Solder composition (%Ag,%Cu)
- Low melting solders

## UBM Variables

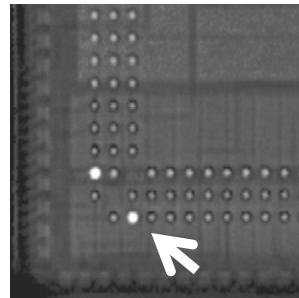
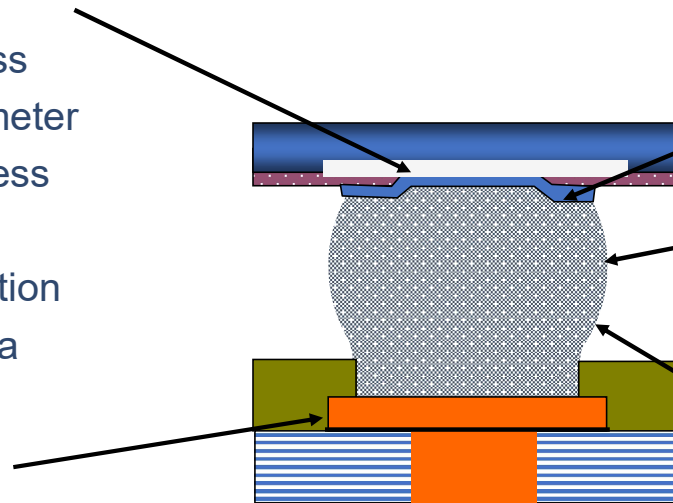
- UBM undercut
- Chip size and DNP
- Ni and/or Cu thickness
- Ni deposition (stress)

## C4 Bump

- %Ag, % Cu, additives
- Volume and height
- Solder microstructure
- Thermal undercut

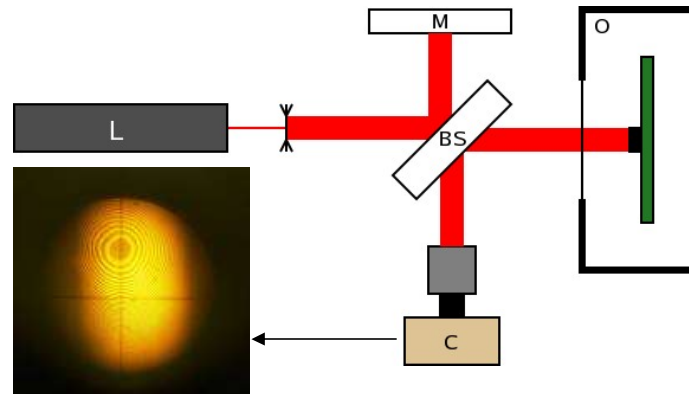
## Joining

- Die thickness
- Cooling rate
- Reflow temp / profile
- Solder microstructure
- TCB: Differential heating /cooling
- NCP at joining



**White Bump is a T0 Problem.**

# Dynamic Chip Warpage Measurements

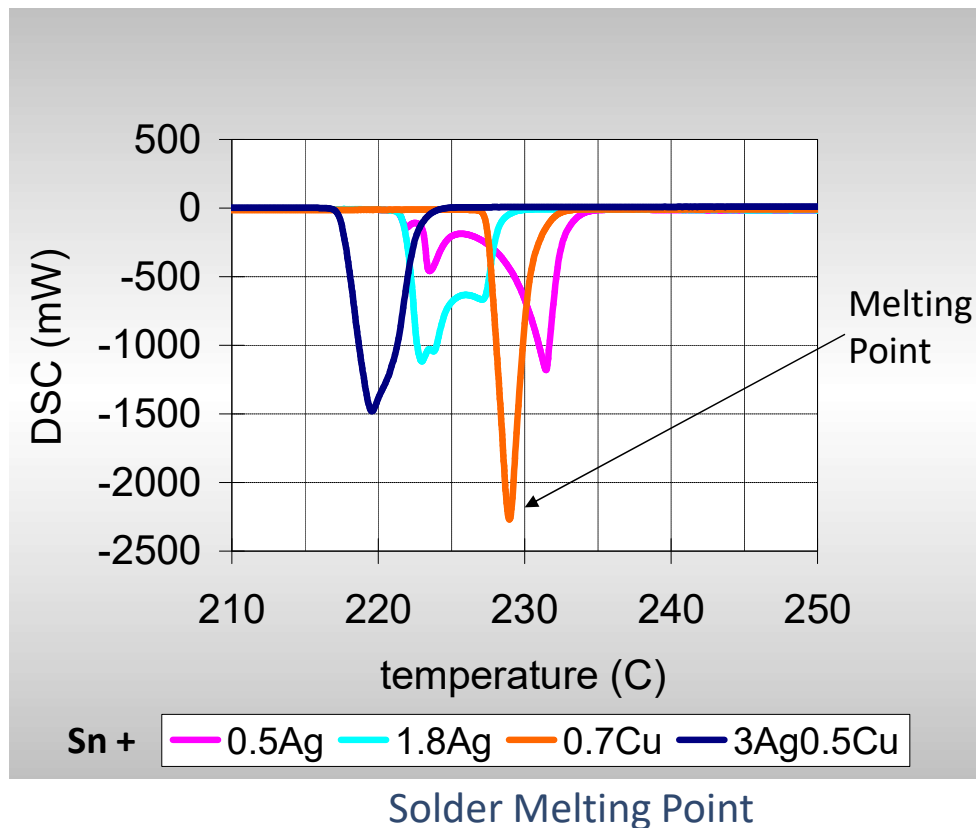


Interferometric measurements of the backside of the chip are precise (rms ~ 100 nm), fast (10 Hz) and non-contact.

DCWM adds a flexible heating/cooling system for reflow simulations ( $\pm 5^{\circ}\text{C/s}$ ,  $\pm 0.1^{\circ}\text{C}$ )

Hypothesis: Chip warpage correlates linearly with stress in joint.

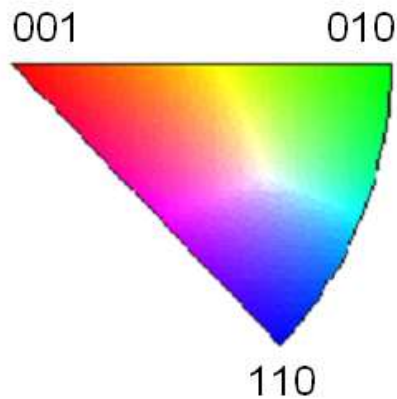
# Differential Scanning Calorimetry (DSC)



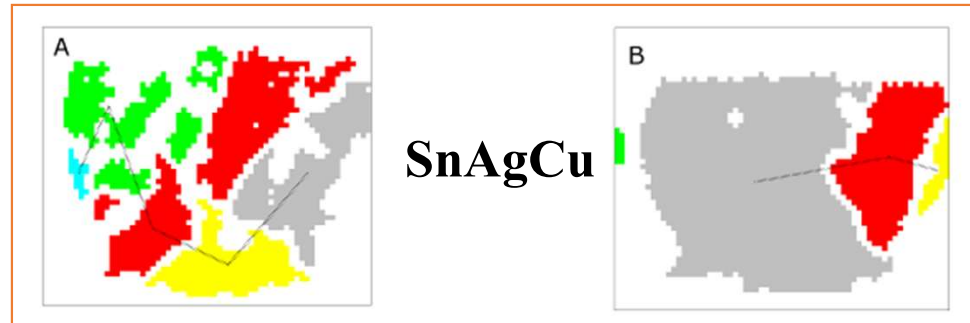
Sample wt : 10 – 15 mg, heating rate : 5 C / min

DSC is a low-cost method of monitoring the solder plating composition.

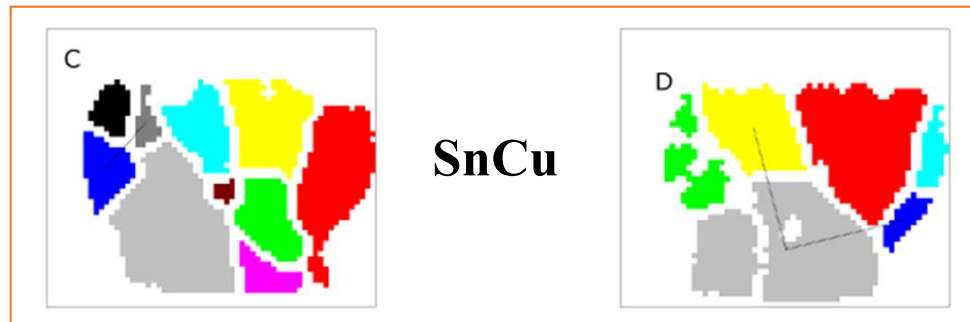
# Electron Backscatter Diffraction (EBSD) Imaging



EBSD provide the solder grain orientation mapping. It can be used to identify cracks as intergranular or transgranular.



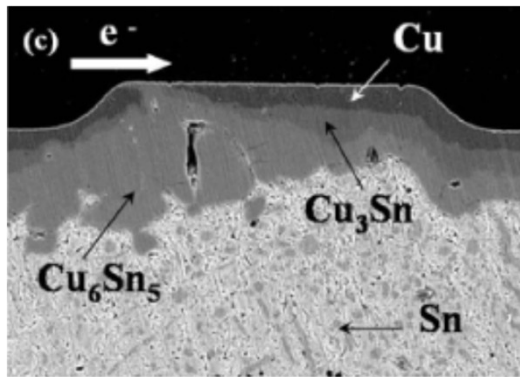
SnAgCu joints have fewer grains, and more 60° twins than SnCu grains.



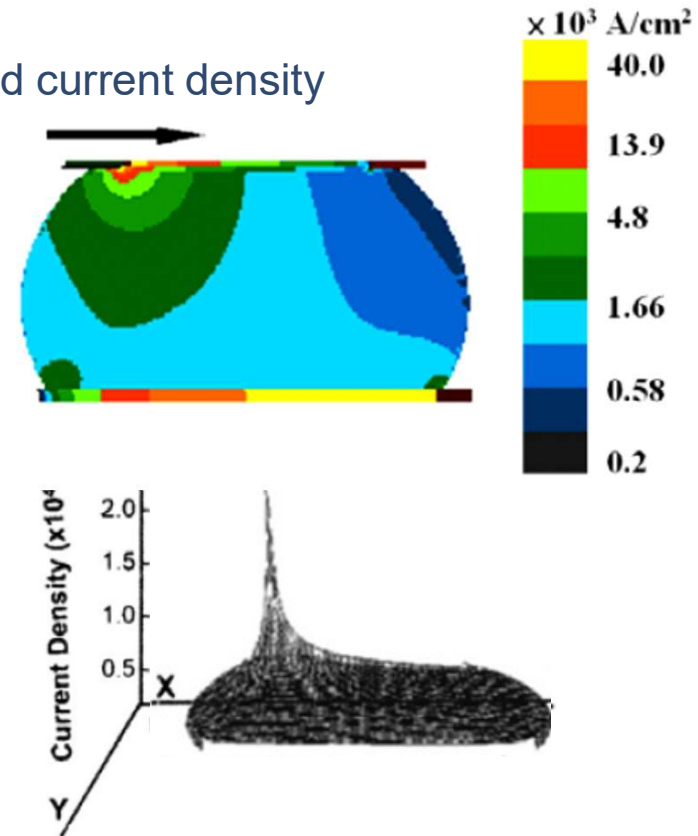
Colors show independent grains; dotted lines identify 60° twins

# Electromigration (EM) Fails

- Sn diffusion at operating conditions
  - Driven by increases of junction temperature and current density



Current crowding:  
Highest current density occurs at the point  
where the UBM meets the BEOL wiring.



# Black's Equation and Effect of Sn Grain Orientation

Black's EM Equation:

$$MTTF = A j^{-n} e^{\left(\frac{Q}{kT}\right)}$$

$A$  is a constant

$j$  is the current density

$n$  is a model parameter

$Q$  is the activation energy in eV (electron volts)

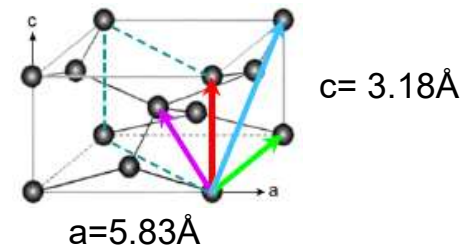
$k$  is Boltzmann constant

$T$  is the absolute temperature in K

| Diffusion element in Sn |        | Diffusivity (cm <sup>2</sup> /sec) |                          |
|-------------------------|--------|------------------------------------|--------------------------|
|                         |        | 150°C                              | 25°C                     |
| Ag<br>(in Solder)       | a-axis | 5.60 x 10 <sup>-11</sup>           | 5.75 x 10 <sup>-15</sup> |
|                         | c-axis | 3.13 x 10 <sup>-9</sup>            | 6.76 x 10 <sup>-12</sup> |
| Cu<br>(in Laminate)     | a-axis | 1.99 x 10 <sup>-7</sup>            | 3.85 x 10 <sup>-9</sup>  |
|                         | c-axis | 8.57x 10 <sup>-6</sup>             | 1.16 x 10 <sup>-6</sup>  |
| Ni<br>(in Chip side)    | a-axis | 3.85 x 10 <sup>-9</sup>            | 6.04 x 10 <sup>-12</sup> |
|                         | c-axis | 1.17 x 10 <sup>-4</sup>            | 1.35 x 10 <sup>-5</sup>  |
| Sn<br>(in Solder)       | a-axis | 1.24 x 10 <sup>-12</sup>           | 4.85 x 10 <sup>-18</sup> |
|                         | c-axis | 4.92 x 10 <sup>-13</sup>           | 1.50 x 10 <sup>-18</sup> |

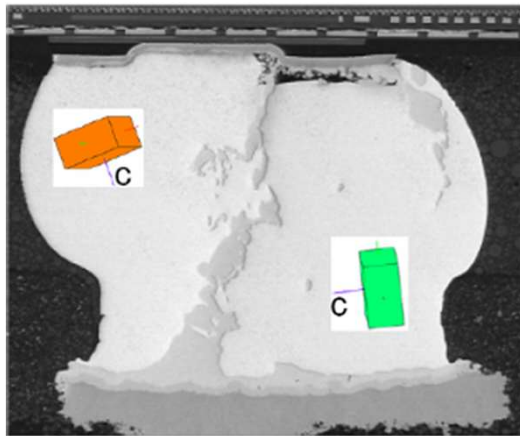
Sn grain orientation plays a role in the likelihood of EM failure.

Body Centered Tetragonal

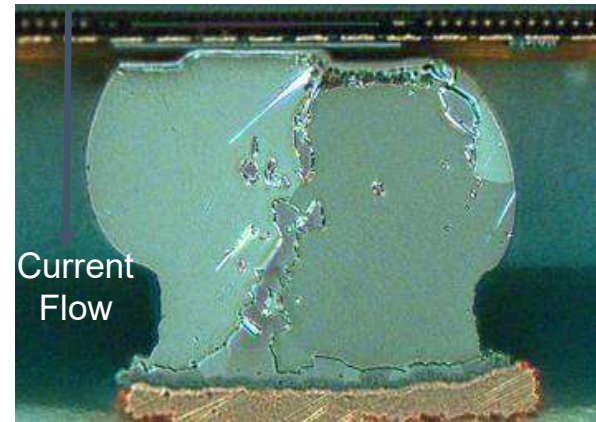
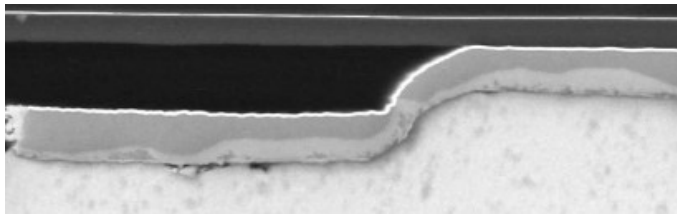


# Example of Bi-Crystal C4 with SnCu Solder

SEM x-section

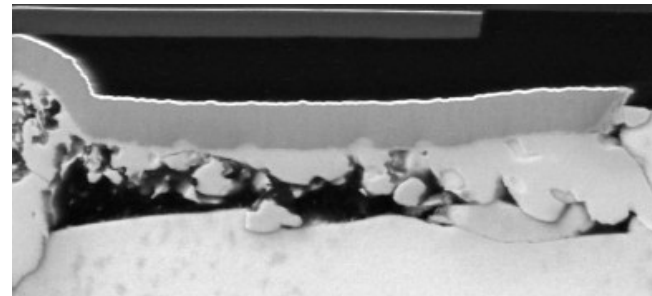


- **Mode-II: Fast diffusion, IMC movement and barrier layer consumption, c-axis of Sn grain along current direction, common in SnCu**



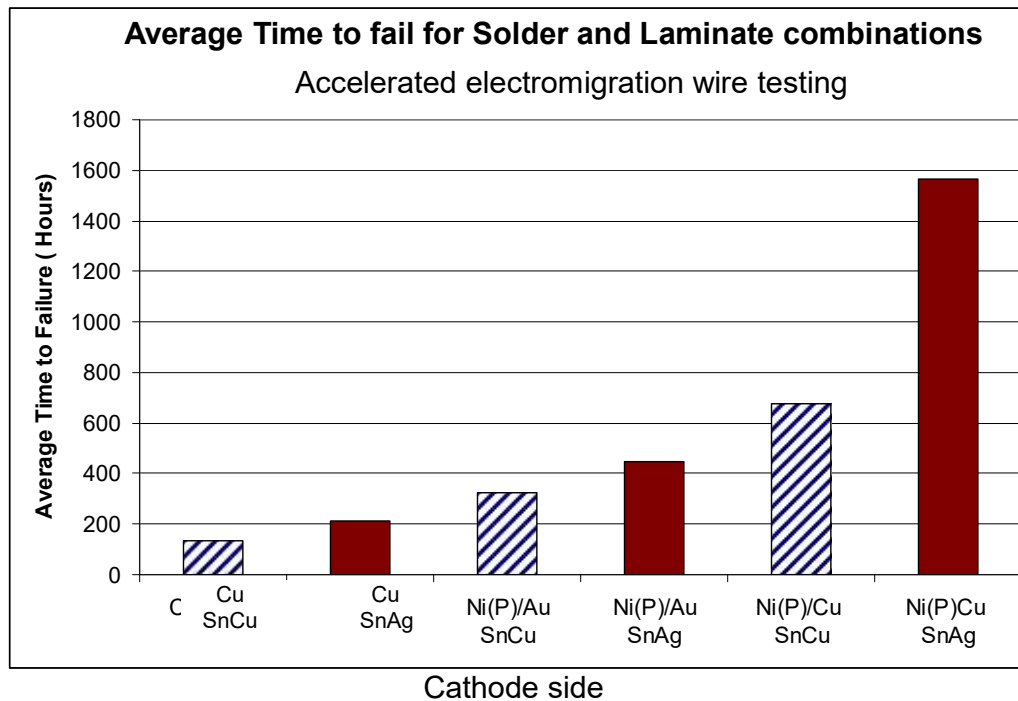
Optical microscopy:  
Polarized image

- **Mode-I: Sn self diffusion, voids between IMC and solder, c-axis of Sn grain not align to current, more common in SnAg**



M. Lu, et al, "Comparison of Electromigration Performance for Pb-free Solders and Surface Finishes," 2008 ECTC

# Comparison of Average Time to Failure: Wire Testing



Anode side is  
Chip side:  
TiW/Ni/Cu

← Lamine / Chip UBM  
← Solder composition

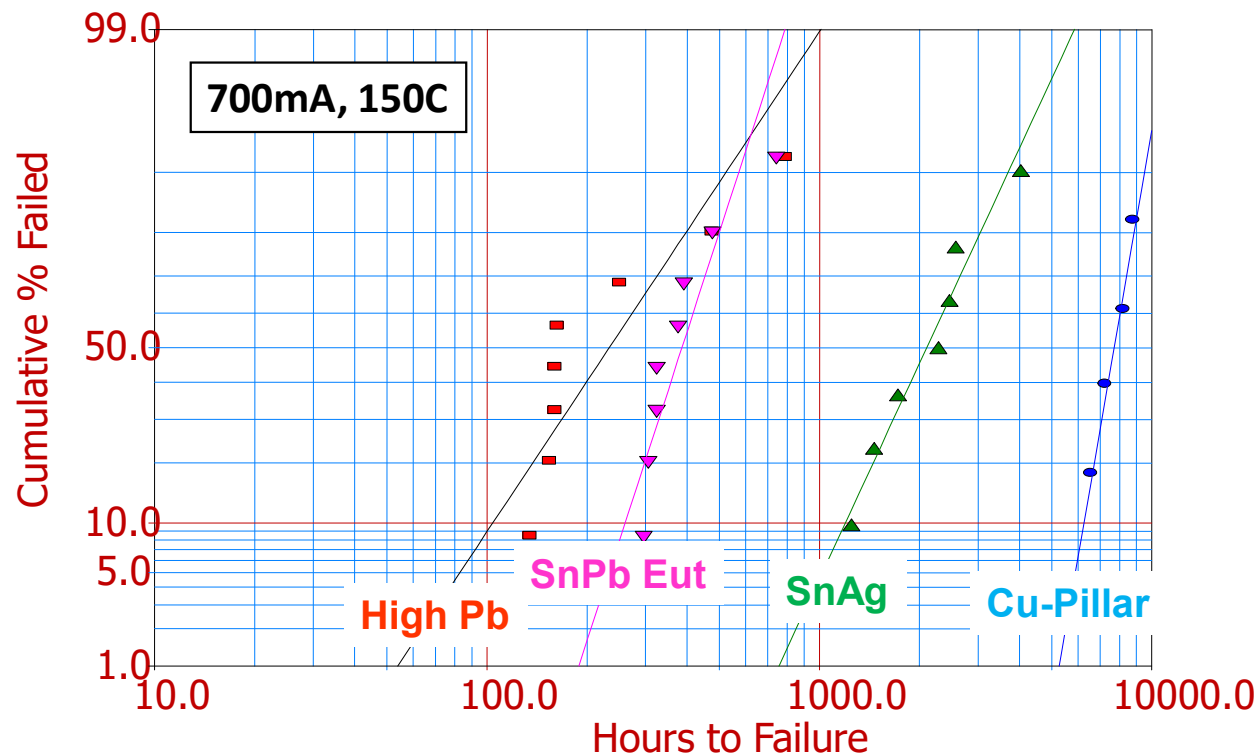
SnAg > SnCu

Ni(P)/Cu > Ni(P)/Au > Cu

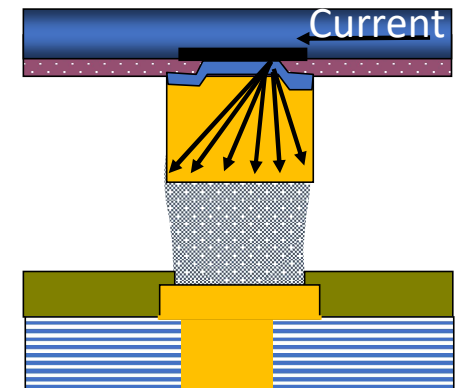
→ Cu on UBM and formation of  $\text{Cu}_6\text{Sn}_5$  intermetallic is important in improving EM lifetime

# Electromigration Comparison

Cu-Pillar > SnAg > SnPb eutectic > High Pb  
Cu-Pillar 3.35X better life than SnAg



Cu-Pillar redistribute the current over a large area , reducing the current density.



# Bond and Assembly Variables Affecting Electromigration

## F-BEOL Variables

- PSPI via diameter
- PSPI via shape
- Al pad thickness
- Al pad size/shape
- PSPI via location
- Cu-Al layer via

## Laminate Variables

- Substrate CTE
- Solder mask opening
- Metallurgy: Cu OSP vs **Ni/Au**
- Solder composition (%Ag,%Cu)

## UBM Variables

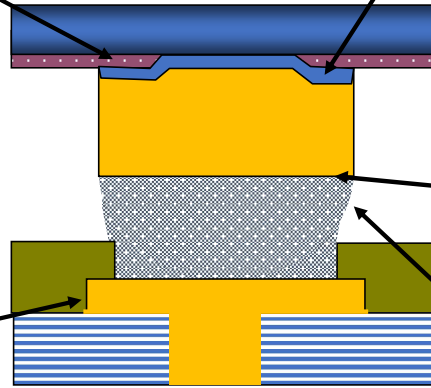
- UBM Thickness: Std or Cu-pillar
- UBM size/shape
- Terminal metal: Ni or Cu
- Ni and/or **Cu thickness**
- Ni deposition (stress)

## C4 Bump

- **%Ag, % Cu, %Sn**
- Volume and height
- Solder grain orientation

## EM Test

- Temperature
- Current density
- Stress at test temperature
- Test duration



## Part 5: Solders, CPI and EM Summary

### Core Reliability Themes

- **Solder composition & microstructure** govern wetting, undercooling, fatigue, and EM lifetime
- **Chip-Package Interaction (CPI)** is the dominant source of early failures
- **White bump / ELK cracking** driven by die warpage during T0 reflow
- **Electromigration physics** controlled by current crowding, IMC behavior, and Sn grain orientation

### Reliability Enablers

- **Solder additives:** Bi, Sb, In, Ni, Co, Zn for aging control, undercooling reduction, creep resistance
- **Low-temperature SnBi joining** to reduce warpage (SLID / FO-WLP)
- **Ni barrier UBM** can suppress Sn whiskers
- **Cu-pillar with thin solder cap** → 3.35× EM lifetime improvement
- **TCB joining** → minimizes laminate–chip temperature delta, reduces white bump
- **Metrology & modeling:** DSC (melting point), EBSD (grain orientation), DCWM (warpage)

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*Thank You*

# Flip-Chip Characterization Techniques

| Characterization Technique                   | Destructive?    | Comments                                             |
|----------------------------------------------|-----------------|------------------------------------------------------|
| X-Ray                                        | Non-Destructive | Used for defects, such as void inspection in solder  |
| Focused Ion Beam                             | Destructive     | Designed to x-section a small area without polishing |
| Scanning Electron Microscope                 | Either          | High resolution Inspection                           |
| Energy Dispersive X-ray Spectroscopy EDS     | Either          | Elemental composition of a small area                |
| Electron Backscatter Diffraction EBSD        | Destructive     | Provides grain mapping and orientation               |
| Differential Scanning Calorimetry DSC        | Destructive     | Provides solder melting point                        |
| Solder Shear or Chip pull                    | Destructive     | Assess bump mechanical integrity                     |
| Confocal Scanning Acoustic Microscopy (CSAM) | Non-Destructive | Assesses interconnection voids, cracks, delamination |

# Advanced Package Reliability Failure Modes

| Interconnect          | Reliability Failure Mode                   | Cause of Failure                                   | Driving Force/Challenge                                                                 |
|-----------------------|--------------------------------------------|----------------------------------------------------|-----------------------------------------------------------------------------------------|
| BGA Solder Joint      | Cracking/Voiding                           | Fatigue and Electromigration                       | CTE mismatch, Package size, die/package ratio, warpage, current density, marginal joint |
| RDL/D2D/Sub Cu Traces | Cracking/Voiding/short                     | Fatigue; EM and Stress migration, electro-chemical | Die/interposer size and current density, electrical field                               |
| Underfill             | Underfill cracking/delamination            | Fatigue/bend stress                                | Large die/interposer size, new materials, D2D gap                                       |
| U bump/C4 bump Joints | Cracking/Voiding induced electrical open   | Fatigue; EM and Stress migration                   | Large die/interposer, high current density, Bump size/height, thermal gradient          |
| 3D Cu/Cu Hybrid Bond  | Voiding                                    | EM and stress migration                            | Increased chip temperature, bond current density                                        |
| TSV(Through Si Via)   | Cracking/voiding and Dielectric Failure    | Electromigration and Dielectric Breakdown          | Increased die temp and current density                                                  |
| BEOL                  | Cracking/Voiding                           | Fatigue, EM and Stress migration                   | Increased current density, SHE and JHE, Local thermal cycling                           |
| Cu/ELK (CPI)          | ELK cracking                               | Thermal and mech stress                            | Large die size, Cu-pillar bumps, Cu/ELK metal density and density gradient              |
| HBM Stack             | Failures within HBM stack                  | Thermal and mech stress                            | Large interposer size, package level stress                                             |
| Photonics             | Coupling loss, optical performance degrade | Thermal and mech and optical power                 | Increased warpage, material degradation, thermal gradient induced local stresses        |

# Bumping Technologies Challenges

| Architecture Type                        | Interconnect Technologies                          | Tightest Pitch           | Typical Interconnection Process        | Typical Equipment        | Typical Applications                                      | Key Concerns and Challenges (Partial List)                                                                                       | Advantages (Partial List)                                                      |
|------------------------------------------|----------------------------------------------------|--------------------------|----------------------------------------|--------------------------|-----------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------|
| 2D                                       | Wire-Bonding                                       | 25 $\mu\text{m}$         | Wire-bonding                           | Wire-Bonder              | Automotive, LCD drivers, Sensors, ASICs, Controllers      | - <b>Oxidation of Cu bonds</b> - Wire-bond lift-off due to CTE mismatch                                                          | - Low cost-of-ownership - Flexible process - Easy to test / re-work wire-bonds |
| 2D & 2D Enhanced                         | u-bumps, C4s, TSVs, and passive Si Interposer      | 20 $\mu\text{m}$<br>(55) | TCB or Mass reflow                     | TCB<br>(Mass Reflow)     | CPUs, GPUs, FPGA, Network servers, Gaming Console Servers | - <b>Warpage issues</b> due to large package size - Interposer testing<br>- Handling thinned wafers<br>- <b>Electromigration</b> | Packaging enables High performance HI e.g., ASIC + HBM                         |
| 2D Enhanced, 3D die-to-die, die-to-wafer | Cu-pillars, passive and active Si coupons & wafers | < 10 $\mu\text{m}$       | Solderless Cu-Cu TCB                   | TCB                      | AI, High-Performance Computing (HPC)                      | - <b>Ensuring KGD</b> - Test coverage - Die handling - No re-workability<br>- Misalignment during Die placement                  | Already established TCB tooling with improvements - Pitch scaling - HI         |
| 3D Die-to-Die, Die-to-Wafer              | Cu-Cu Bonding                                      | 5 $\mu\text{m}$          | F2F or F2B Cu-Cu Hybrid Bonding - TCB  | Custom bonding equipment | AI, High-Performance Computing (HPC)                      | - Ensuring KGD - <b>Test coverage</b> - High cost of ownership - Misalignment / <b>Foreign Materials</b> (FM) particles          | Pitch scalability                                                              |
| 3D Wafer-to-Wafer                        | Cu-Cu Bonding                                      | 0.9 $\mu\text{m}$        | F2F or F2B Direct Cu-Cu Hybrid Bonding | Custom bonding equipment | AI, High-Performance Computing (HPC)                      | - Ensuring KGD/stacks - Test coverage - High cost of ownership - <b>Misalignment</b>                                             | High 3D interconnect density with ultra-low bonding latency                    |

# Acronyms

|       |                                         |          |                                                    |         |                                                 |
|-------|-----------------------------------------|----------|----------------------------------------------------|---------|-------------------------------------------------|
| ABF   | Ajinomoto Build-up Film                 | EMC      | Epoxy Molding Compound                             | NCP     | Nonconductive Paste                             |
| ACA   | Anisotropic Conductive Adhesives        | EMIB     | Embedded Multi-die Interconnect Bridge             | NSMD    | Non-Solder Mask Defined                         |
| AI    | Artificial Intelligence                 | ENEC/OSP | Electroless Ni(P) + Electroless Copper + OSP       | OSP     | Organic Solderability Preservative              |
| AP    | Mobile Application Processor            | ENEPIG   | Electroless Ni(P) + Electroless Palladium + Imm Au | PBO     | Polybenzoxazoles                                |
| ASIC  | Application Specific Integrated Circuit | ENIG     | Electroless Ni(P) + Immersion Au                   | PCB/PWB | Printed Circuit/Wiring Board                    |
| BCB   | Benzocyclobutene                        | eWLB     | embedded Wafer Level Ball Grid Array               | PMICS   | Package-on-Package<br>Micro-Interconnect System |
| BCP   | Build-Panel Carrier boards              | FEOL     | Front End Of Line                                  | PR      | Photoresist                                     |
| BEOL  | Back End Of Line, Refer to metal layers | FL       | Flip-Chip                                          | PSPI    | Photosensitive Polyimide                        |
| BGA   | Ball Grid Array                         | FLBGA    | Flip-Chip Ball Grid Array                          | RDL     | Redistribution Layer                            |
| BH    | Bond Head (of TCB)                      | FO-WLP   | Fanout Wafer Level Package                         | RF      | Radio Frequency                                 |
| BoL   | Bump on Lead                            | GPU      | Graphics Processing Unit                           | SAC     | Tin-Silver-Copper                               |
| BoP   | Bump on Pad                             | HAST     | Highly Accelerated Stress Test                     | SAP     | Semi-Additive Process                           |
| C4    | Controlled Collapse Chip Connection     | HBM      | High Bandwidth Memory                              | SEM     | Scanning Electron Microscope                    |
| CoWoS | Chip on Wafer on Substrate              | HTS      | High Temperature Solder                            | SLID    | Solid-Liquid Inter-Diffusion                    |
| CPI   | Chip-Package Interaction                | I/O      | Input / Output                                     | SMD     | Solder Mask Defined                             |
| CPU   | Central Processing Unit                 | ILD      | Inter Layer Dielectric                             | SoC     | System on Chip                                  |
| CSAM  | Confocal Scanning Acoustic Microscopy   | IMC      | Intermetallic Compound                             | SoP     | Solder on Pad                                   |
| CSP   | Chip Scale Package                      | IMS      | Immersion Molded Solder                            | TCB     | Thermal Compression Bonding                     |
| CTE   | Coefficient of Thermal Expansion        | InFO-L   | Integrated Fan-Out – Local Interconnect            | Tg      | Glass Transition Temperature                    |
| CUF   | Capillary Underfill                     | JEDEC    | Joint Electron Device Engineering Council          | TIM     | Thermal Interface Material                      |
| DCWM  | Dynamic Chip Warpage Measurement        | LAP      | Laser Assisted Packaging                           | TMV     | Through Mold Vias                               |
| DSC   | Differential Scanning Calorimetry       | MCU      | u Controller Unit                                  | TSV     | Through Si Vias                                 |
| EBS   | Electron Backscatter Diffraction        | MR       | Mass Reflow                                        | UBM     | Under Bump Metal                                |
| EDS   | Energy Dispersive X-ray Spectroscopy    | MU       | Mold Underfill                                     | UCLe    | Ultra-Clean Interposer Environment              |
| ELK   | Extreme Low-K                           | NCF      | Nonconductive Film                                 | ULK     | Ultra Low-k                                     |
| EM    | Electromigration                        | NCP      | Nonconductive Paste                                | WLCSP   | Wafer Level Chip Scale Packaging                |